PRELIMINARY SPECIFICATION

GoldStar
GOLD STAR CO.,LTD.

GM71C4256
262,144 WORDS × 4 BIT CMOS DYNAMIC RAM

T-46-23-17

Description

The GM71C4256 is the new generation dynamic RAM organized 262,144×4 Bit. The GM71C4256 utilizes GoldStar's silicon Gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the GM71C4256 to be packaged in a standard 20 pin DIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

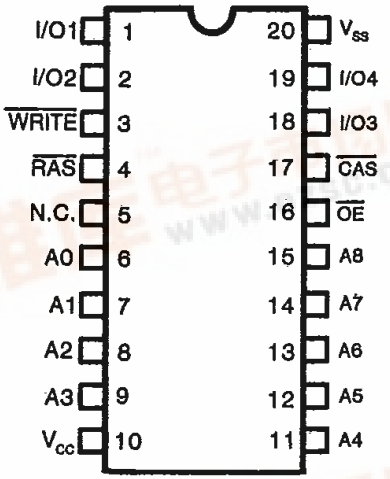
Features

- **262,144 × 4 Bit organization**
- **Fast access time and cycle time: 85/100/120(Max)**

PARAMETER		GM71C4256(ns)		
		−85	−10	−12
t_{RAC}	$\overline{RAS}$ Access Time	85	100	120
t_{AA}	Column Adress Access Time	45	50	60
t_{CAC}	$\overline{CAS}$ Access Time	30	30	35
t_{RC}	Cycle Time	165	190	220
t_{PC}	Fast Page Mode Cycle Time	50	55	70

- **Single Power Supply of 5V±10% with a built-in V_{BB} generator**
- **Low Power**
  - **330mW MAX. Operating (GM71C4256-85)**
  - **274mW MAX. Operating (GM71C4256-12)**
  - **16.5mW MAX. Standby**
- **Output unlatched at cycle end allows two-dimensional chip selection**
- **Read-Modify-Write, $\overline{RAS}$-only refresh, and Fast Page Mode Capability**
- **All input and output TTL compatible**
- **512 refresh cycles/8ms**
- **Industry standard 20 pin Plastic DIP**

Pin Configuration



A_0–A_8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

Absolute Maximum Ratings

Input Voltage	V_{IN}	−1∼7V
Output Voltage	V_{OUT}	−1∼7V
Power Supply Voltage	V_{CC}	−1∼7V
Operating Temperature	T_{OPR}	0∼70°C
Storage Temperature	T_{STG}	−55∼150°C
Short Circuit Output Current	I_{OUT}	50mA

(Note 1)

Recommended DC Operating Conditions

(T_A=0°C to +70°C)

V_{CC}	Supply Voltage	4.5∼5.5V
V_{IH}	Input High Voltage	2.4∼6.5V
V_{IL}	Input Low Voltage	−1.0∼0.8V

(Note 2)

Functional Block Diagram

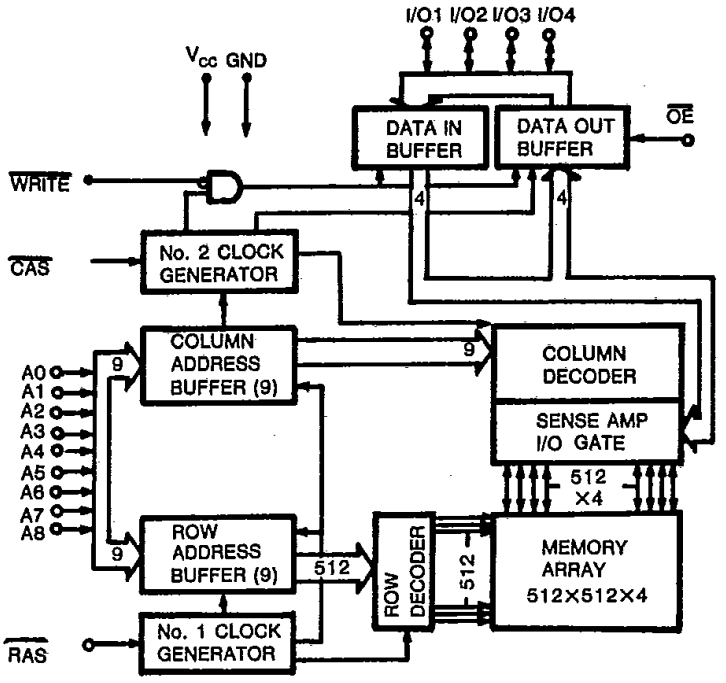


Figure 1

DC Electrical Characteristics: (V_{CC}=5±10%, T_A=0 ~70°C) T-46-23-17

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTES
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT}=−5mA)		2.4	—	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT}=4.2mA)		—	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN)	85	—	70	mA	3,4
		100	—	65		
		120	—	55		
I_{CC2}	Standby Current Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		—	3	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN)	85	—	75	mA	3
		100	—	65		
		120	—	55		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=t_{PC} MIN)	85	—	55	mA	3,4
		100	—	45		
		120	—	35		
I_{CC5}	Standby Current Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)		—	1	mA	
$I_{I(L)}$	Input Leakage Current Any Input (0V≤V_{IN}≤6.5V, All other Pins Not Under Test = 0V)		−10	10	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is is Disabled, 0V≤V_{OUT}≤V_{CC}		−10	10	μA	

Capacitance (V_{CC}=5V±10%, f=1MHz, T_A=0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
CI_1	Input Capacitance (A0—A8)	—	5	pF
CI_2	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	—	7	pF
C_O	Output Capacitance (I/O_1–I/O_4)	—	7	pF

Electrical Characteristics And Recommended AC Operating Conditions (V_{CC}=5V±10%, T_A=0~70°C)
(Note 5,6,7)

SYMBOL	PARAMETER	GM71C4256-85		GM71C4256-10		GM71C4256-12		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read/Write Cycle Time	165	—	190	—	220	—	ns	
t_{RMW}	Read-Modify-Write Cycle Time	225	—	225	—	295	—	ns	
t_{PC}	Fast Page Mode Cycle Time	50	—	55	—	70	—	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	110	—	115	—	140	—	ns	
t_{RAC}	Access Time from $\overline{RAS}$	—	85	—	100	—	120	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	—	30	—	30	—	35	ns	8, 13
t_{AA}	Access Time from Column Address	—	45	—	50	—	60	ns	8, 14
t_{CPA}	Access Time from CAS Precharge	—	45	—	50	—	65	ns	8, 14
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5	—	5	—	5	—	ns	5
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	—	80	—	90	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	85	100,000	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	30	—	30	—	35	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	—	100	—	120	—	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	30	10,000	30	10,000	35	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	25	70	25	85	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	10	—	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	—	15	—	20	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	—	10	—	15	—	ns	
t_{ASR}	Row Address Set-Up Time	0	—	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	15	—	15	—	15	—	ns	
t_{ASC}	Column Address Set-Up Time	0	—	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	20	—	20	—	25	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	65	—	75	—	90	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	—	50	—	60	—	ns	
t_{RCS}	Read Command Set-Up Time	0	—	0	—	0	—	ns	10
t_{RCH}	Read Command Hold Time	0	—	0	—	0	—	ns	10
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	—	0	—	0	—	ns	10

(V_{CC}=5V±10%, T_A=0~70°C) Unit: nS (Note 5,6,7)

SYMBOL	PARAMETER	GM71C4256-85		GM71C4256-10		GM71C4256-12		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WCH}	Write Command Hold Time	20	—	20	—	25	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	65	—	75	—	90	—	ns	
t_{WP}	Write Command Pulse Width	20	—	20	—	25	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	30	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	25	—	30	—	ns	
t_{DS}	Data Set-Up Time	0	—	0	—	0	—	ns	11
t_{DH}	Data Hold Time	20	—	20	—	25	—	ns	11
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	65	—	75	—	90	—	ns	
t_{REF}	Refresh Period	—	8	—	8	—	8	ms	
t_{WCS}	Write Command Set-Up Time	0	—	0	—	0	—	ns	12
t_{CWD}	$\overline{CAS}$ to $\overline{Write}$ Delay Time	65	—	65	—	75	—	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{Write}$ Delay Time	120	—	135	—	160	—	ns	12
t_{AWD}	Column Address to $\overline{Write}$ Delay	80	—	85	—	100	—	ns	12
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	—	0	—	0	—	ns	
t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	20	—	20	—	20	—	ns	
t_{OEA}	$\overline{OE}$ Access Time	—	25	—	25	—	30	ns	
t_{OED}	$\overline{OE}$ to Data Delay	25	—	25	—	30	—	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	25	0	25	0	30	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	25	—	25	—	30	—	ns	

Notes

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All Voltage are refrenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μS is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved..
6. AC measurements assume t_T=5nS.
7. V_{IH}(min) and V_{IL}(max) are referenced levels for measuring timing of input signals. Also transition times are required between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max) and t_{OEZ}(max) defines the time at which the output achieves the open circuit condition and is not refrenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle: If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min) and $t_{AWD} \geq t_{AWD}$(min) the cycle is a read-write cycle and data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a referenced point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a referenced point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

Timing Waveforms

T-46-23-17

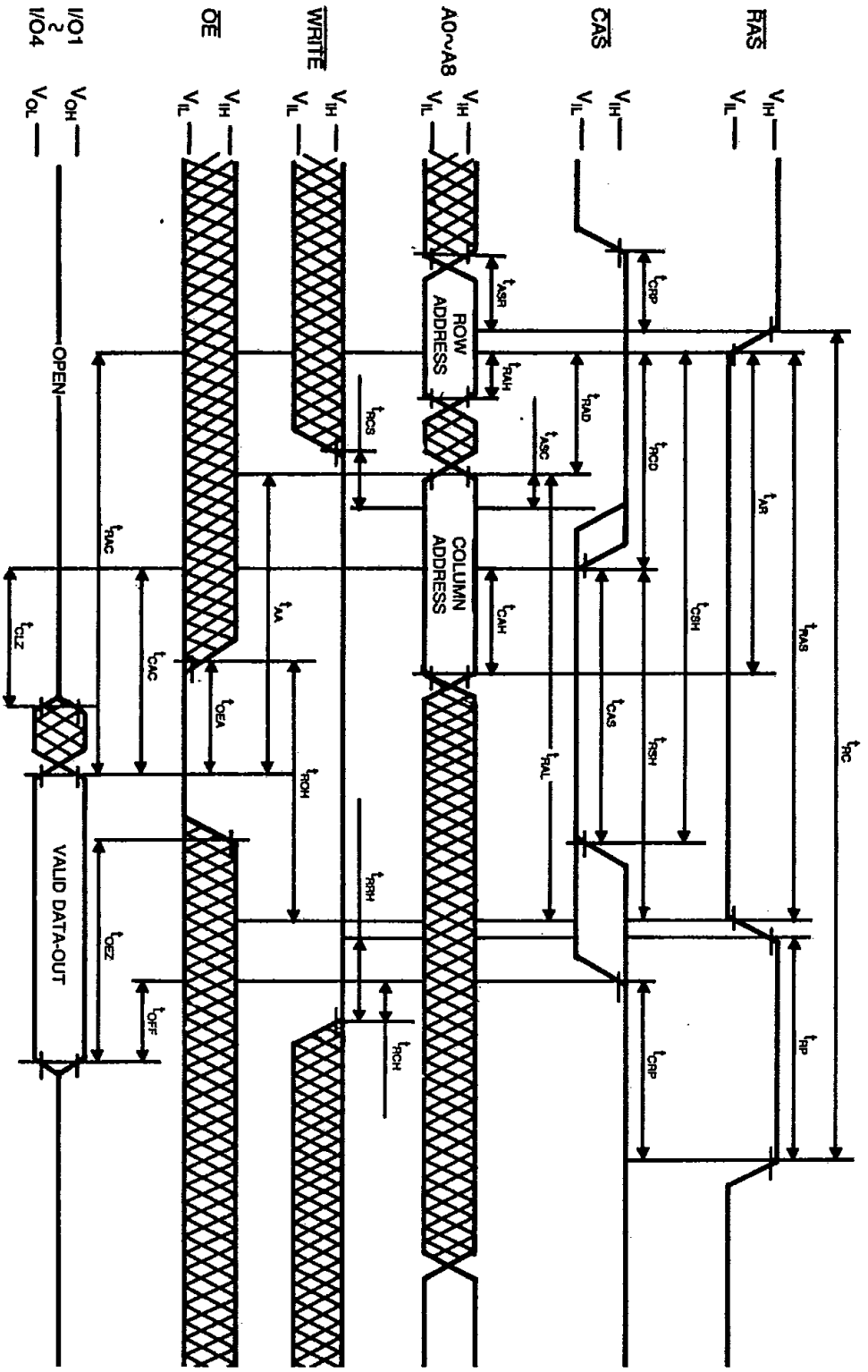


Figure 2. Read Cycle

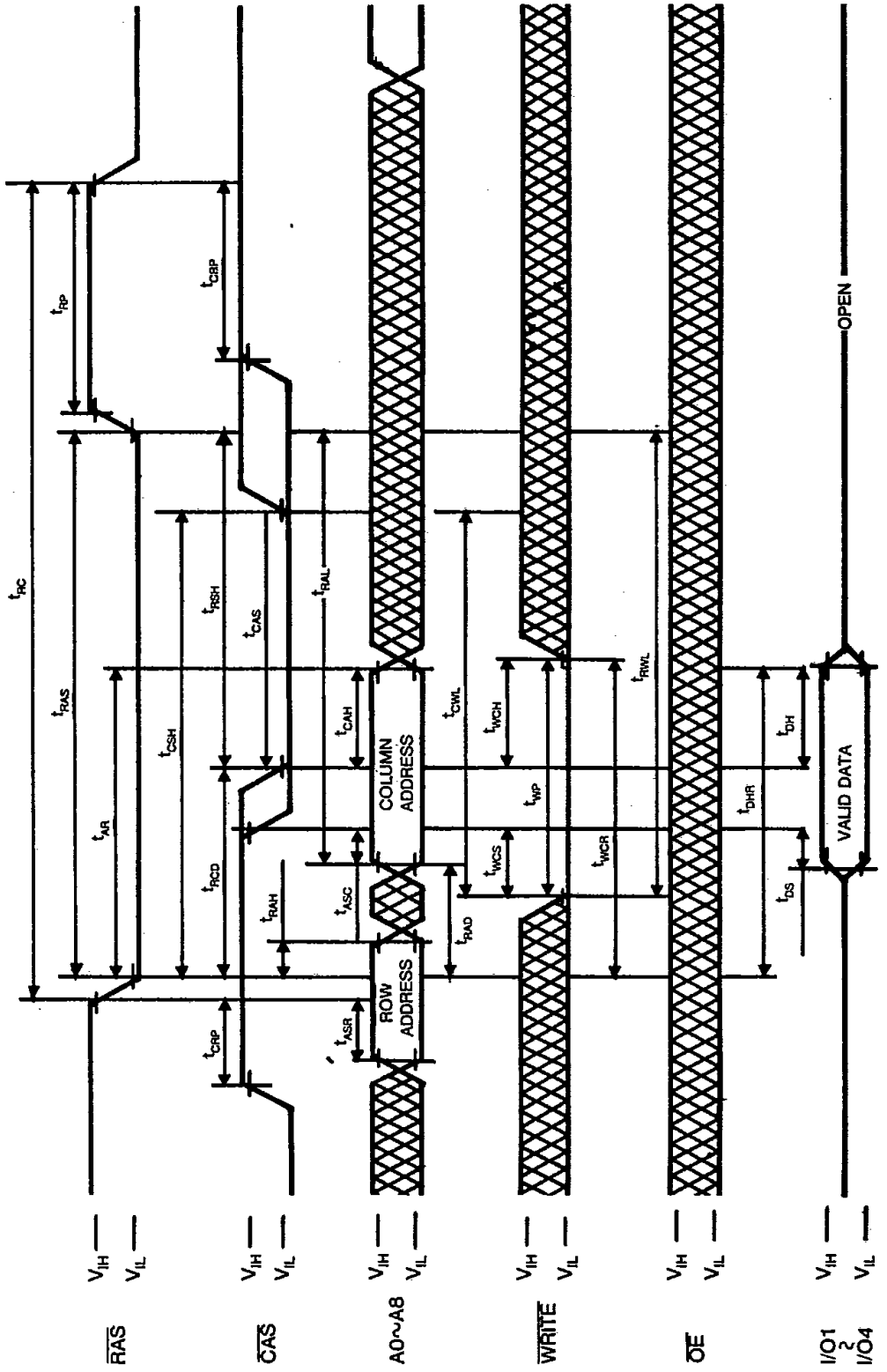


Figure 3. Write Cycle (Early Write)

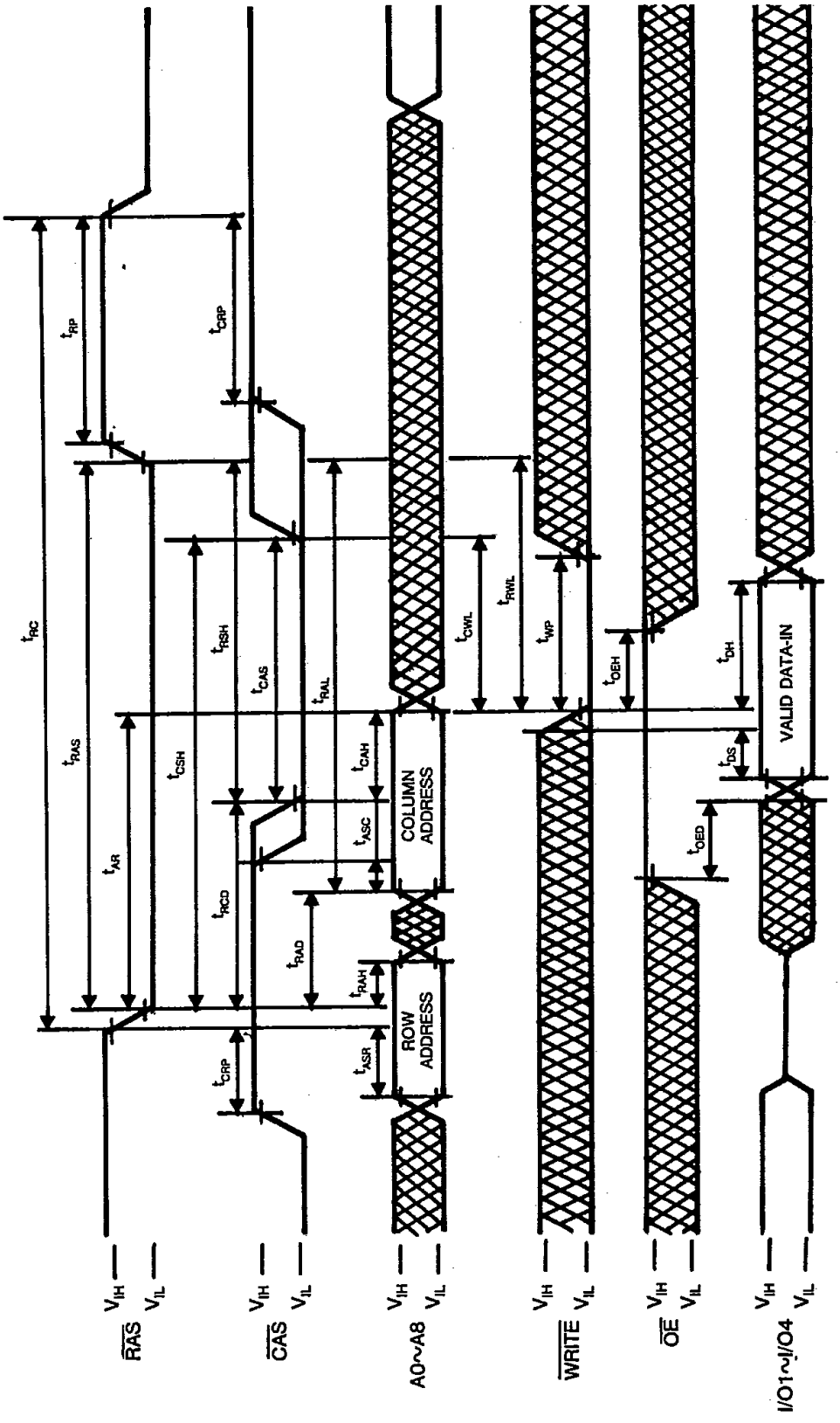


Figure 4. Write Cycle ($\overline{OE}$ Controlled Write)

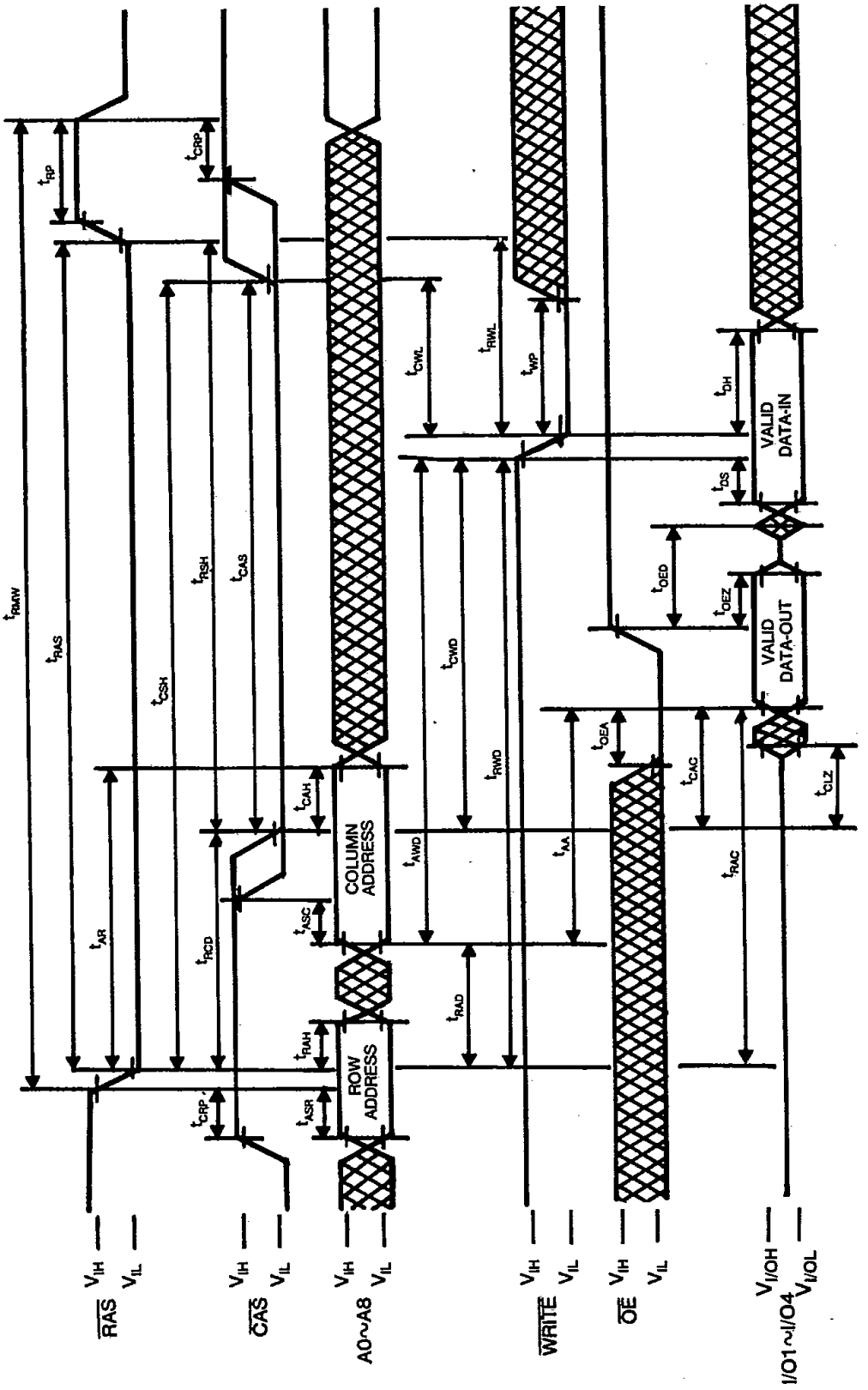


Figure 5. Read-Modify-Write Cycle

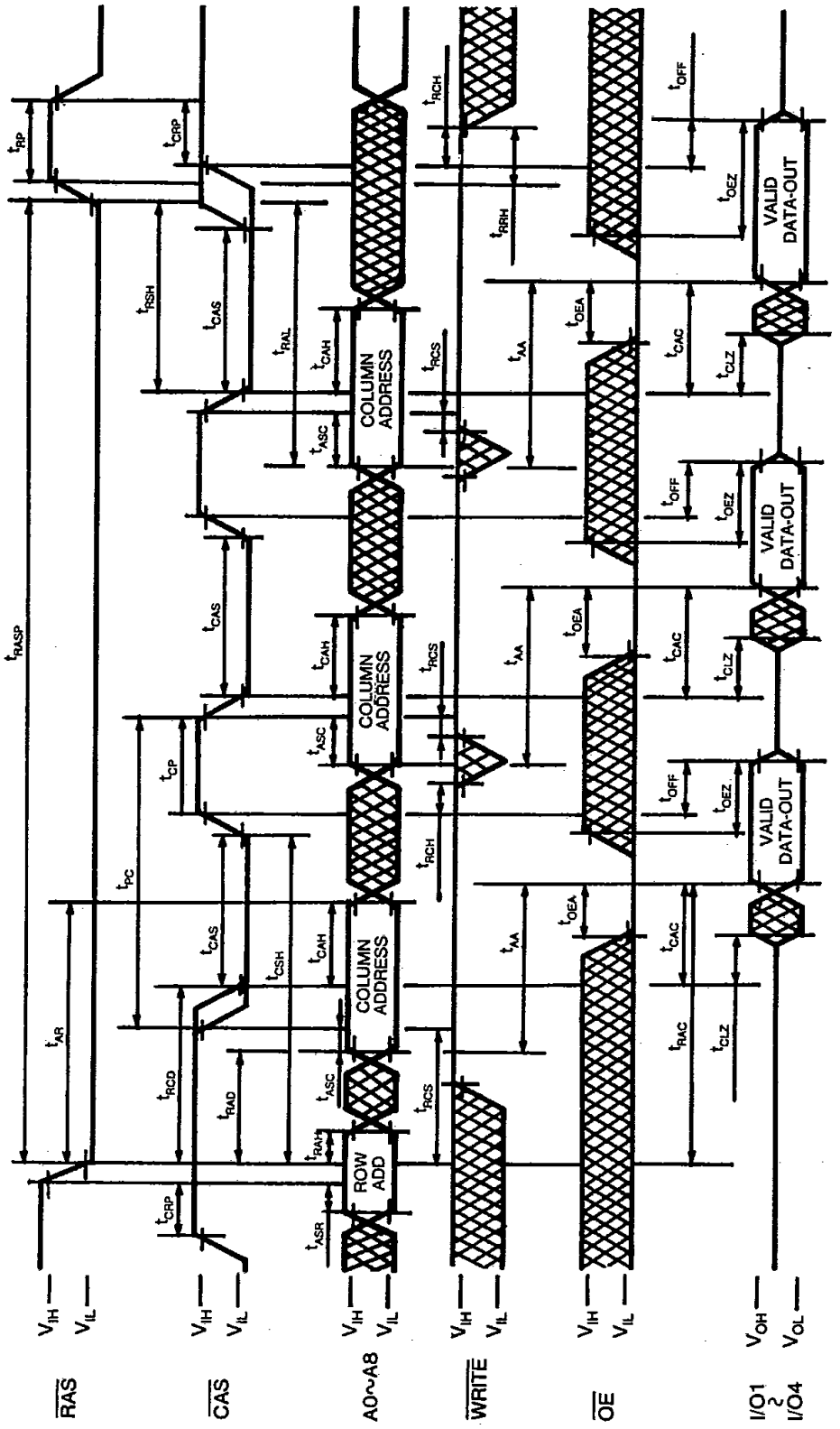


Figure 6. Fast Page Mode Read Cycle

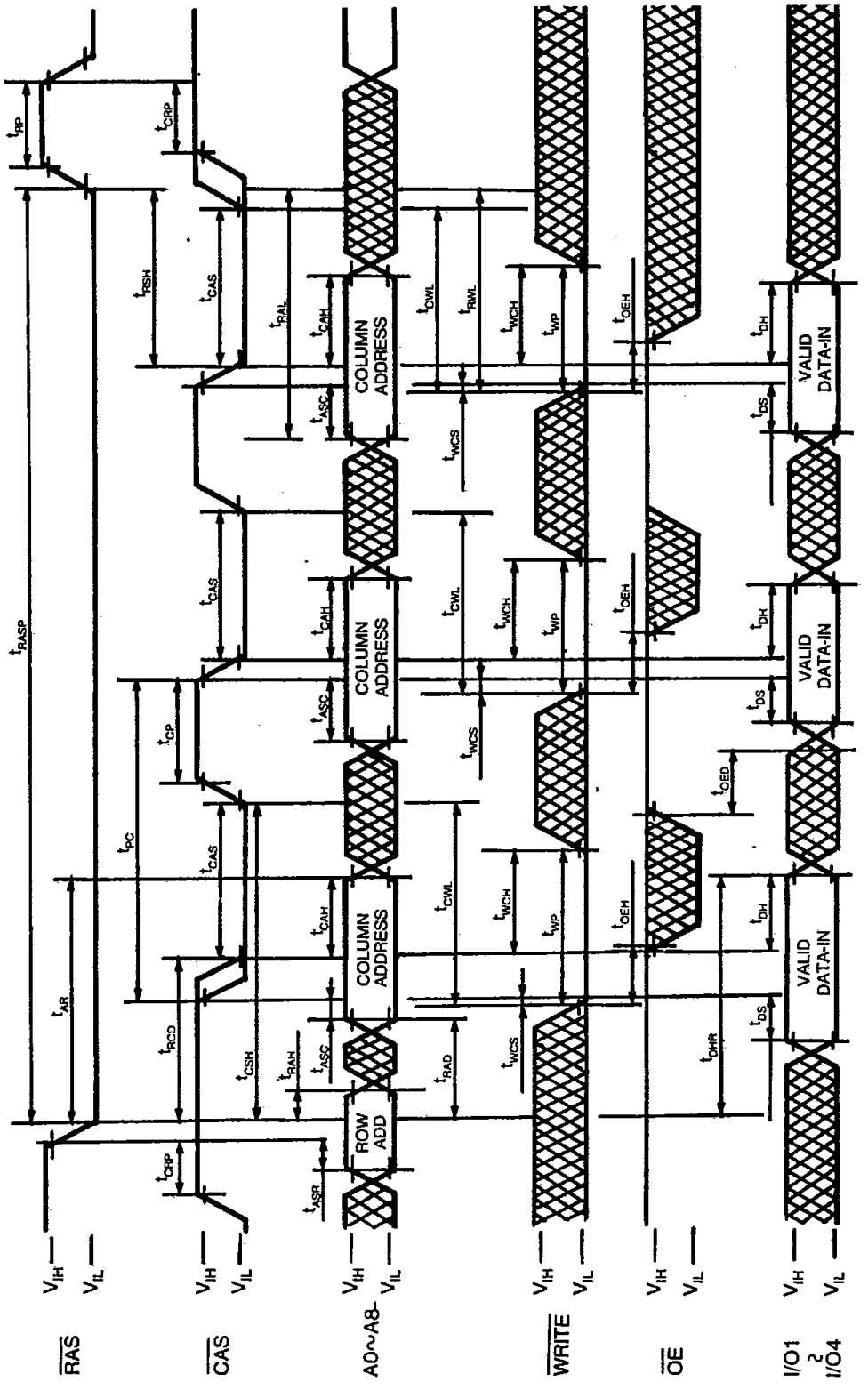


Figure 7. Fast Page Mode Write Cycle

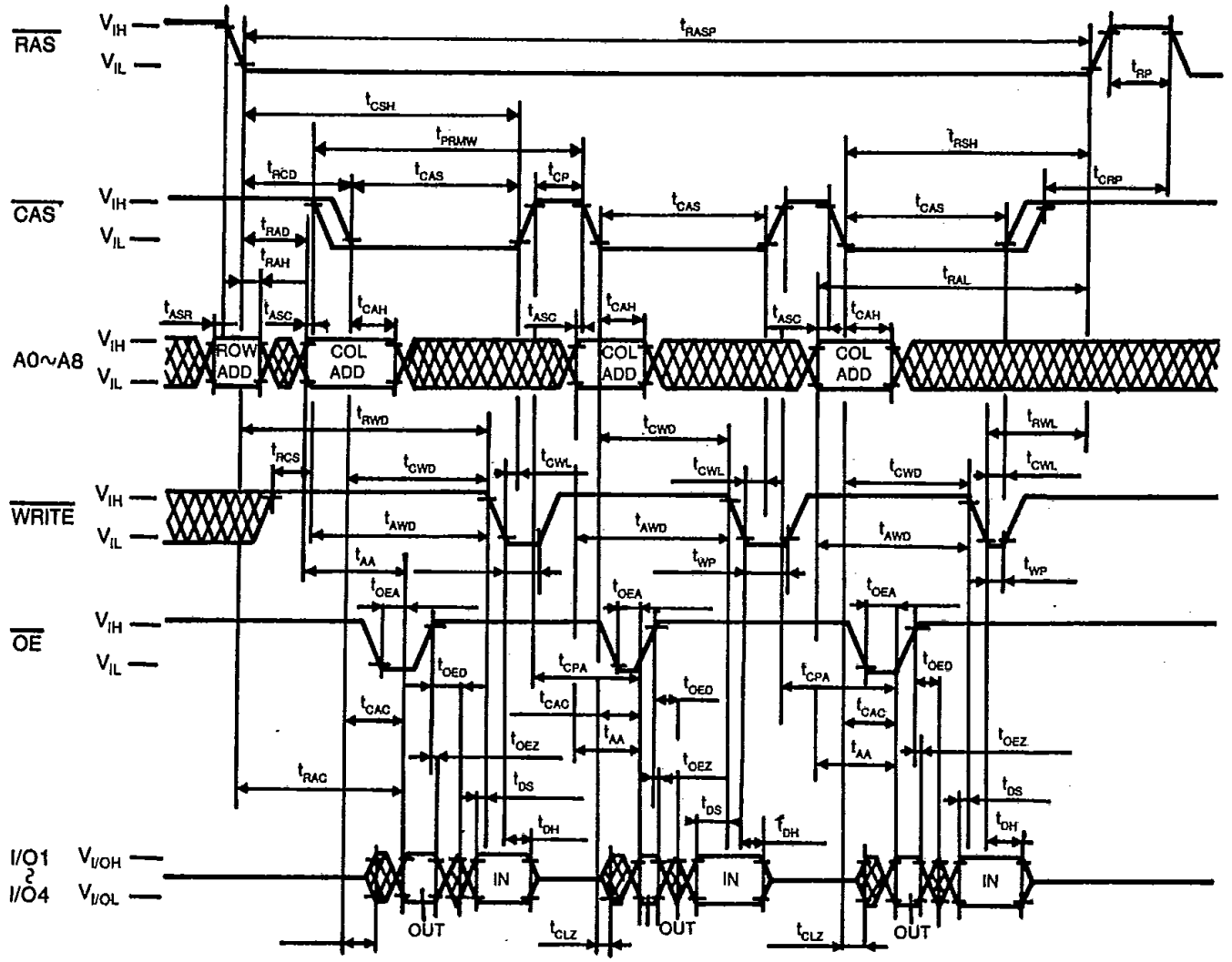


Figure 8. Fast Page Mode Read-Modify-Write Cycle

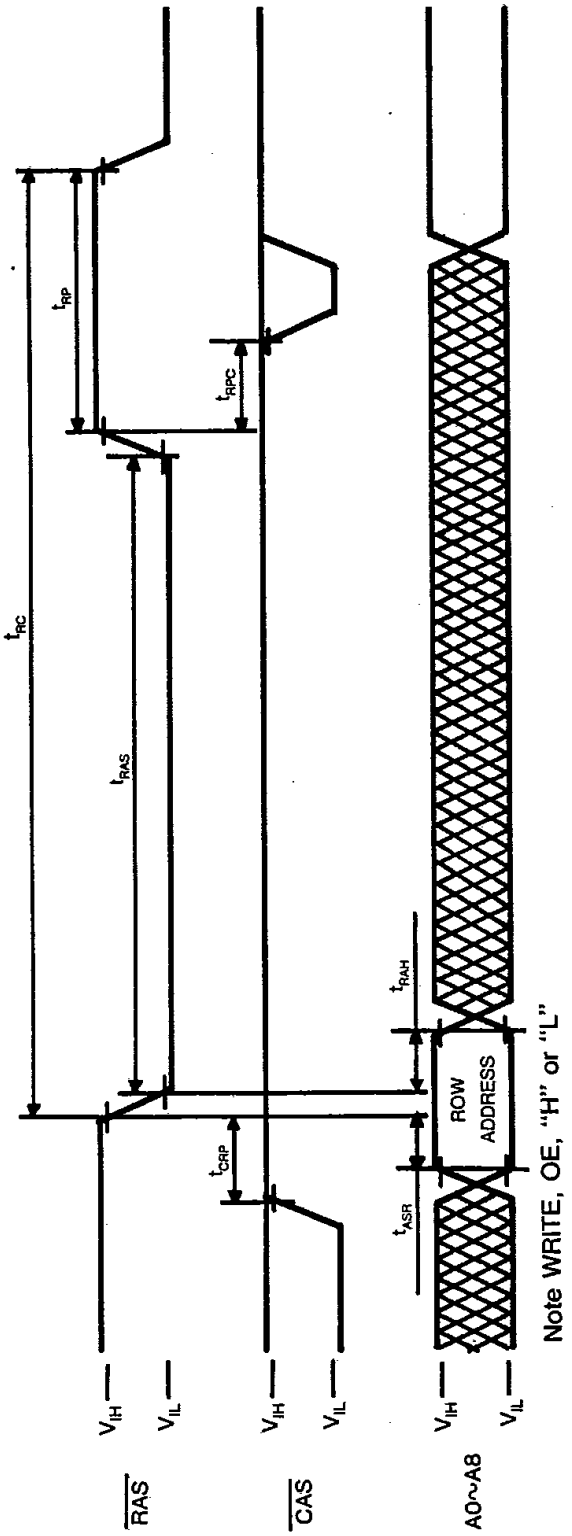
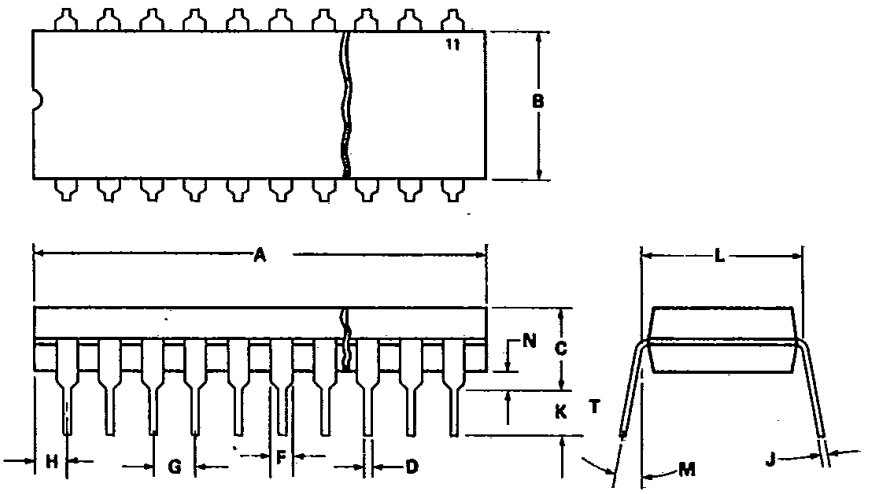


Figure 9. $\overline{RAS}$ Only Refresh Cycle

PACKAGE DIMENSION

T-90-20

PLASTIC DIP



(UNIT: INCHES)

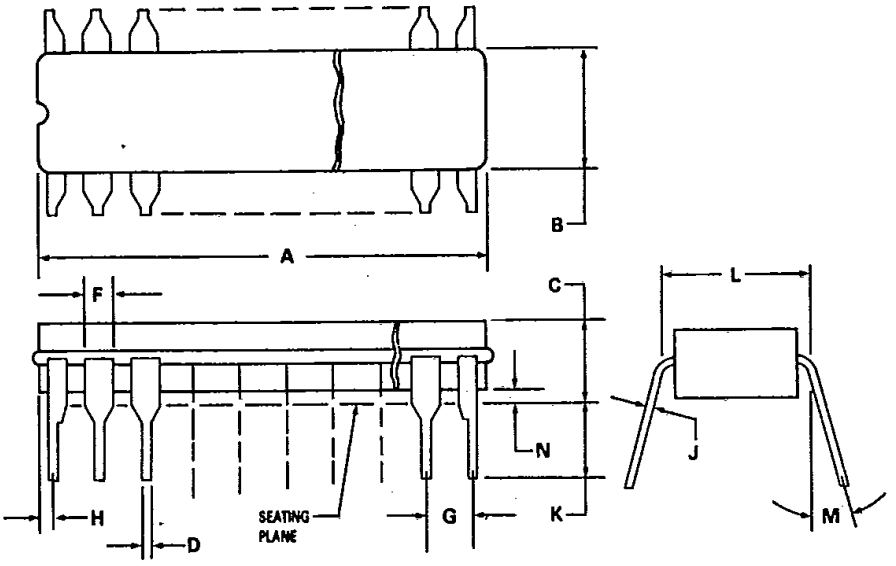
SYMBOL	16 PIN		18 PIN		20 PIN		22 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.738	0.752	0.875	0.900	1.013	1.040	1.095	1.150
B	0.245	0.255	0.245	0.255	0.263	0.273	0.260	0.287
C	0.143	0.152	0.145	0.162	0.143	0.152	0.145	0.160
D	TYP. 0.018		TYP. 0.018		TYP. 0.018		TYP. 0.018	
F	TYP. 0.063		TYP. 0.060		TYP. 0.065		TYP. 0.060	
G	0.09	0.11	0.09	0.11	0.09	0.11	0.09	0.11
H	0.015	0.030	0.04	0.05	0.058	0.066	—	0.075
J	0.009	0.014	0.009	0.015	0.009	0.010	0.009	0.010
K	0.125	0.145	0.125	0.130	0.125	0.132	0.125	0.142
L	0.300 BSC		0.300 BSC		0.300 BSC		0.300 BSC	
M	0′	10′	0′	10′	0′	10′	0′	10′
N	0.015	—	0.015	—	0.015	—	0.015	

SYMBOL	24 PIN		28 PIN					
	MIN	MAX	MIN	MAX				
A	1.243	1.260	1.415	1.460				
B	0.535	0.545	0.535	0.545				
C	0.158	0.170	0.158	0.170				
D	TYP. 0.018		TYP. 0.018					
F	TYP. 0.060		TYP. 0.060					
G	0.09	0.11	0.09	0.11				
H	0.06	0.075	0.06	0.076				
J	0.009	0.015	0.009	0.015				
K	0.125	0.132	0.125	0.132				
L	0.600	0.625	0.600	0.620				
M	0′	10′	0′	10′				
N	0.008	—	0.008	—				

PACKAGE DIMENSION

T-90-20

CER DIP



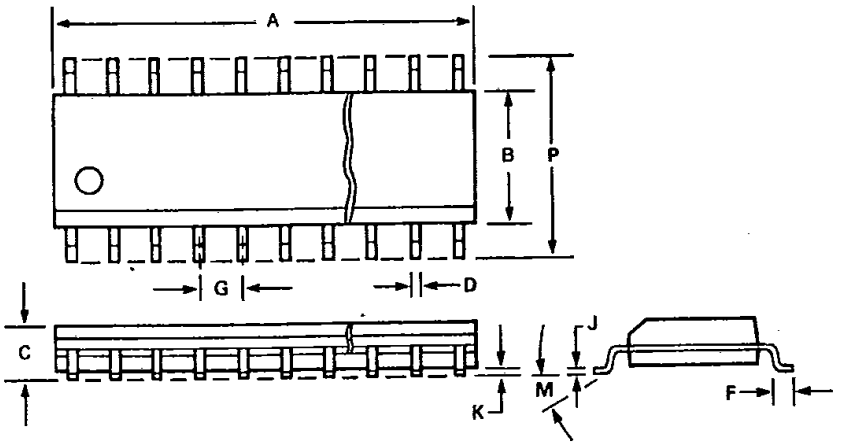
(UNIT : INCHES)

SYMBOL	16 PIN		20 PIN		24 PIN		28 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.753	0.785	0.940	0.985	1.240	1.290	1.440	1.485
B	0.272	0.294	0.265	0.306	0.514	0.526	0.514	0.598
C	0.165	0.200	0.165	0.200	0.165	0.200		0.225
D	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.023
F	0.055	0.065	0.055	0.065	0.055	0.065	0.055	0.065
G	0.09	0.11	0.09	0.11	0.09	0.11	0.09	0.11
H	0.012	0.060	0.012	0.060	0.040	0.098	0.040	0.098
J	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
K	0.125	0.20	0.125	0.20	0.125	0.20	0.125	0.20
L	0.29	0.32	0.29	0.32	0.590	0.620	0.590	0.620
M	0′	10′	0′	10′	0′	10′	0′	10′
N	0.02	0.06	0.02	0.07	0.02	0.07	0.02	0.07

PACKAGE DIMENSION

T-90-20

SOP



(UNIT : INCHES)

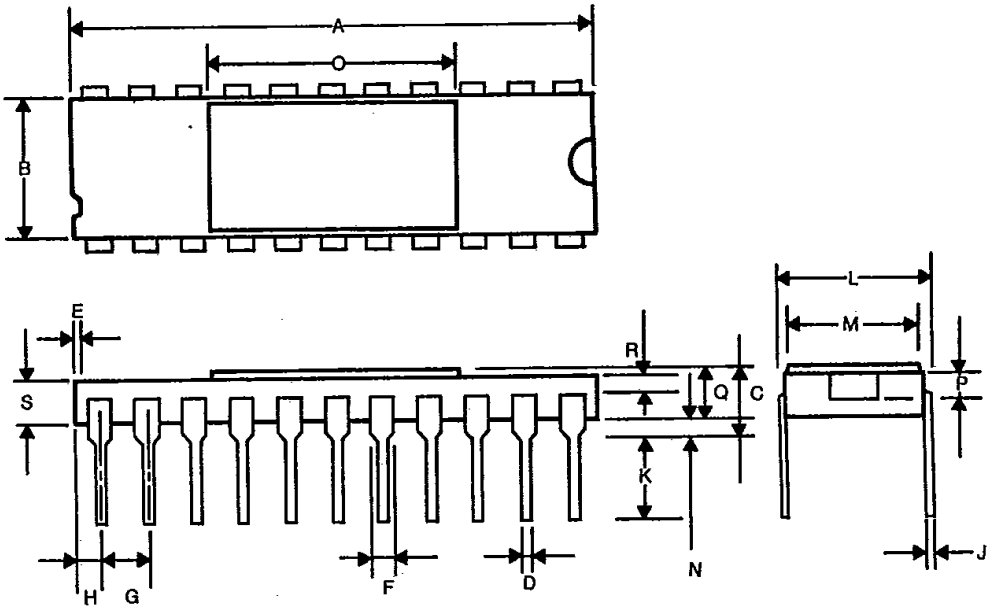
CODE NO.	20 F		24 F		24 FW			
PIN	20 PIN		24 PIN		24 PIN			
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX		
A	0.496	0.510	0.602	0.614	0.622	0.638		
B	0.292	0.299	0.292	0.299	TYP. 0.331			
C	0.097	0.104	0.097	0.104	—	0.098		
D	0.014	0.019	0.014	0.019	0.012	0.018		
F	0.018	0.035	0.018	0.035	TYP 0.039			
G	0.050 BSC		0.050 BSC		0.050 BSC			
J	0.010 BSC		0.010 BSC		0.010 BSC			
K	0.004	0.008	0.0055	0.0115	0.004			
P	0.400	0.410	0.400	0.410	0.453	0.477		
M	0°	8°	0°	8°	—	—		

CODE NO.	28 F		28 FW					
PIN	28 PIN		28 PIN					
SYMBOL	MIN	MAX	MIN	MAX				
A	0.703	0.712	0.720	0.750				
B	0.292	0.289	TYP. 0.331					
C	0.097	0.104		0.098				
D	0.014	0.019	0.012	0.018				
F	0.018	0.035	TYP. 0.039					
G	0.050 BSC		0.050 BSC					
J	0.010 BSC		0.010 BSC					
K	0.0055	0.0115	0.004	—				
P	0.400	0.410	0.453	0.477				
M	0°	8°	—	—				

PACKAGE DIMENSION

SIDE BRAZED

T-90-20



(UNIT: INCHES)

SYMBOL	22 PIN	
	MIN	MAX
A	1.088	1.112
B	0.281	0.298
C	—	0.160
D	0.016	0.020
E	0.004	—
F	TYP. 0.050	
G	0.09	0.105
H	0.035	0.065
J	0.009	0.011

SYMBOL	22 PIN	
	MIN	MAX
K	0.14	0.170
L	0.290	0.310
M	0.265	0.275
N	0.020	0.050
O	0.555	0.565
P	TYP. 0.050	
Q	0.092	0.122
R	0.005	—
S	0.08	—