

Adjustable Micropower Low Dropout SG.COM Linear Regulator with **ENABLE**

Description

The CS8271 is an adjustable micropower voltage regulator with very low quiescent current (60μ A typical at 100μ A load). The output supplies 100mA of load current with a maximum dropout voltage of only 600mV. Control logic includes **ENABLE**. The combination of low quiescent current, outstanding regulator performance and control logic makes the CS8271 ideal for any battery operated equipment.

The logic level compatible **ENABLE** pin allows the user to put the regu-

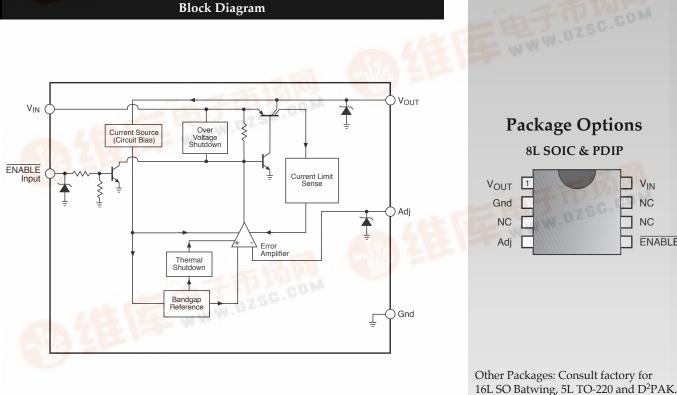
lator into a shutdown mode where it draws only 50µA of quiescent current.

The regulator is protected against reverse battery, short circuit, over voltage, and over temperature conditions. The device can withstand 60V load dump transients making it suitable for use in automotive environments.

The CS8271 is pin compatible with the National Semiconductor LM2931.

Features

- Low Quiescent Current
- **Adjustable Output:** 5V to 12V
- **ENABLE** for Sleep Mode Control
- **100mA Output Current** Capability
 - **Fault Protection** +60V Load Dump -15V Reverse Voltage **Short Circuit Thermal Shutdown**
- Low Reverse Current (Output to Input)





Cherry Semiconductor Corporation 2000 South County Trail, East Greenwich, RI 02818 Tel: (401)885-3600 Fax: (401)885-5786 Email: info@cherry-semi.com Web Site: www.cherry-semi.com

Package Options 8L SOIC & PDIP



CS8271

Absolute Maximum Ratings

Power Dissipation	Internally Limited
Transient Input Voltage	
Reverse Battery	15V
Output Current	Internally Limited
ESD Susceptibility (Human Body Model)	
Junction Temperature	
Storage Temperature	55°C to 150°C
Lead Temperature Soldering	
Wave Solder (through hole styles only)	10 sec. max, 260°C peak
Reflow (SMD styles only)	60 sec. max above 183°C, 230°C peak
Adj and Enable Output	0.3V, 10V
V _{OUT}	0.3V, 20V

Electrical Characteristics	: $V_{OUT} + 1V \le V_{IN} \le 30V$, $5V \le V_{OUT} \le 12V$, $I_{enable} = 0V$; unless otherwise spectrum of the second	_{OUT} = 10mA, ecified.	$-40^{\circ} \le \mathrm{T}_{\mathrm{A}} \le 12$	$5^{\circ}, -40^{\circ} \le T_{J} \le$	150°,
PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT
■ Output Voltage					
Dropout Voltage	$I_{OUT} = 100 \mu A, V_{DROP} = (V_{IN} - V_{OUT})$ $I_{OUT} = 100 mA, V_{DROP} = (V_{IN} - V_{OUT})$		100 400	150 600	mV mV
Load Regulation	Measure V_{OUT} when $I_{OUT} = 100 \mu A$, 100mA. $LD_{REG} = ABS (\Delta V_{OUT})$		0.1	1.0	%V _{OUT}
Line Regulation	$\begin{split} I_{OUT} &= 1 \text{mA. Measure } V_{OUT} \\ \text{when } V_{IN} &= V_{OUT} + 1 \text{V}, 30 \text{V}. \\ \text{LN}_{REG} &= \text{ABS} (\Delta V_{OUT}) \end{split}$		0.1	0.5	%V _{OUT}
Quiescent Current, (I _Q) Active Mode	V_{IN} = 6V, I_{OUT} = 100 μA , V_{OUT} setup for 5V. I_Q = IV_{IN} - I_{OUT}		55	120	μΑ
	V_{IN} = 13V, I_{OUT} = 100 μA , V_{OUT} setup for 12V. I_Q = IV_{IN} - 100 μA		130	200	μΑ
	V_{IN} = 30V, I_{OUT} = 100 μA , V_{OUT} setup for 5V, I_Q = IV_{IN} - 100 μA		150	450	μΑ
	V_{IN} = 30V, I_{OUT} = 100 μA , V_{OUT} setup for 12V, I_Q = IV_{IN} - 100 μA		200	500	μΑ
	$I_{OUT} = 50mA$, $I_Q = IV_{IN}$ - $50mA$		4	7	mA
	I_{OUT} = 100mA, I_Q = IV_{IN} - 100mA		12	21	mA
Quiescent Current, (I _Q) Sleep Mode	$\begin{split} V_{IN} &= 6V, ENABLE = 2.5V, \\ I_{QSLEEP} &= IV_{IN} \end{split}$		20	50	μΑ
	$\label{eq:VIN} \begin{array}{l} V_{IN} = 30V, ENABLE = 2.5V, \\ I_{QSLEEP} = IV_{IN} \end{array}$		75	350	μΑ
Ripple Rejection	<i>f</i> =120Hz, (Note 1)	60	75		dB
Current Limit	V_{OUT} = V_{OUT} - 500mV, I_{LIM} = IV_{OUT}	105	200	300	mA
Short Circuit Output Current	$V_{OUT}=0V$, $I_{SHRT} = IV_{OUT}$	15	100	215	mA
Thermal Limit	(Note 1)	150	180	210	°C
Overvoltage Shutdown	Adjust $V_{\rm IN}$ from 28V to 40V until $V_{\rm OUT}\!\le\!1V$	30	34	38	V
Reverse Current	V_{IN} =0V, I_{REV} = IV_{OUT} , V_{OUT} = 13.2V		100	200	μΑ

$\begin{array}{l} \textbf{Electrical Characteristics:} V_{OUT} + 1V \leq V_{IN} \leq 30V, \\ V_{ENABLE} = 0V; \text{ unless otherwise specified.} \end{array} \\ \begin{array}{l} \textbf{C}_{OUT} = 10\text{ mA}, \\ \textbf{-40^{\circ}} \leq T_{A} \leq 125^{\circ}, \\ \textbf{-40^{\circ}} \leq T_{J} \leq 150^{\circ}, \\ \textbf{V}_{ENABLE} = 0V; \text{ unless otherwise specified.} \end{array} \\ \end{array}$					
PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT
■ ENABLE					
Enable Threshold		1.15	2.0	2.6	V
Enable Input Current	$V_{ENABLE} = 2.6V$ $V_{ENABLE} = 5V$		10 35	20 50	μΑ μΑ

Adjustment Pin	R1: Feedback resistor between V _{OU}	JT and Adjust, I	R2: Adjust r	esistor to gro	ound.
Reference Voltage	$100\mu A \le I_{OU T} \le 100 mA$	1.246	1.272	1.297	V
Adjustment Pin Current	$I_{Adj} = \frac{V_{REF}}{R2} - \frac{(V_{OUT} - V_{REF})}{R1}$		20	500	nA

Note 1: Guaranteed by design, not 100% tested in production.

Package Pin Description			
PACKAGE PIN #	PIN SYMBOL	FUNCTION	
8L SOIC & PDIP			
1	V _{OUT}	100mA output; adjustable from 5V to 12V.	
2	Gnd	Ground.	
3, 6, 7	NC	No Connection.	
4	Adj	Resistor divider from V_{OUT} to Adj, sets output voltage.	
5	ENABLE	Logic level switch, when HIGH, regulator is in sleep mode.	
8	V _{IN}	Input voltage.	

Circuit Description

Output Voltage Adjustment

The output voltage of the CS8271 is adjustable to any value between the reference voltage on the Adj pin, (1.272V Typ.) and the maximum input voltage minus the dropout voltage. To adjust the output voltage, a pair of external resistors R1 and R2 are connected as shown in Figure 1.

The equation for the output voltage is

$$V_{OUT} = V_{REF} x \left(\frac{R1 + R2}{R2}\right) + I_{Adj} x R1$$

where $V_{\rm ref}$ is the typical reference voltage and $I_{\rm Adj}$ is the adjust pin bias current. This is usually 500nA maximum.

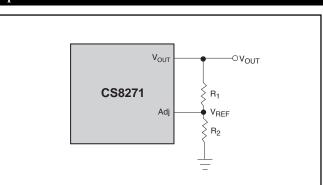


Figure 1: Output Voltage Adjustment.

Circuit Description: continued

Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 2).

If the input voltage rises above 30V (e.g. load dump), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients up to 60V in magnitude.

Short circuit protection limits the amount of current the output transistor can supply. In the case of a CS8271 under a short circuit condition, the output transistor current is limited to 100mA.

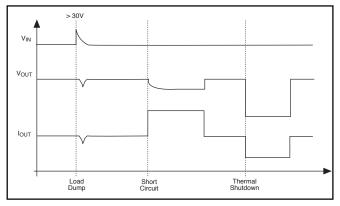


Figure 2: Typical Circuit Waveforms for Output Stage Protection.

Should the junction temperature of the power device exceed 180°C (typ) the power transistor is turned off. Thermal shutdown is an effective means to prevent die overheating since the power transistor is the principle heat source in the IC.

ENABLE

The ENABLE switches the output transistor. When the voltage on the ENABLE pin exceeds 2.0V typ, the output pass transistor turns off, leaving a high impedance facing the load. The IC will remain in Sleep mode, drawing only $20\mu A$ (typ), until the voltage on the ENABLE pin drops below the ENABLE threshold.

Application Notes

Selecting the Right Capacitor Value

The output compensation capacitor C_{OUT} , determines three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The selection of a capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR, can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (-25°C to -40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provide this information.

The value for the output compensation capacitor C_{OUT} shown in Figure 3 should work for most applications, but it is not necessarily the least expensive or the optimal solution.

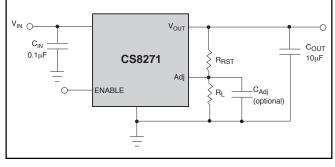


Figure 3: Test and application circuit showing an output compensation capacitor.

To determine an acceptable value for $C_{\rm OUT}$ for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature. Monitor the outputs on the oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. (Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible)

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. (A smaller capacitor will usually cost less and occupy less board space.) If the capacitor oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Application Notes: continued

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real work environment. Vary the ESR to reduce ringing.

Step 7: Remove the unit from the environmental chamber and heat the IC with a heat gun. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of $\pm 20\%$ so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above.

Capacitance on the Adjust pin combined with the feedback resistors R1 and R2 can affect loop stability and should also be considered. The CS8271 internal circuitry produces about 5pF to Ground on the Adjust pin. This capacitance, plus any additional external capacitance on the Adjust pin will create a pole when combined with the resistive feedback network. The effect can be significant when using large values for the feedback resistors to minimize quiescent current.

A capacitor connected from the Adjust pin to Ground provides additional means to compensate the regulator by creating a pole. Alternately, a capacitor can be connected from the Adjust pin to V_{OUT} to create a zero.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 4) is

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}]I_{OUT(max)} + V_{IN(max)}I_Q$$
(1)

where

V_{IN(max)} is the maximum input voltage,

V_{OUT(min)} is the minimum output voltage,

 $I_{\text{OUT}(\text{max})}$ is the maximum output current, for the application

 I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$

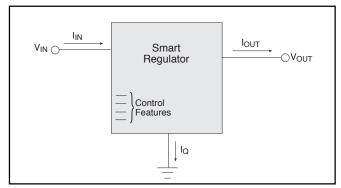


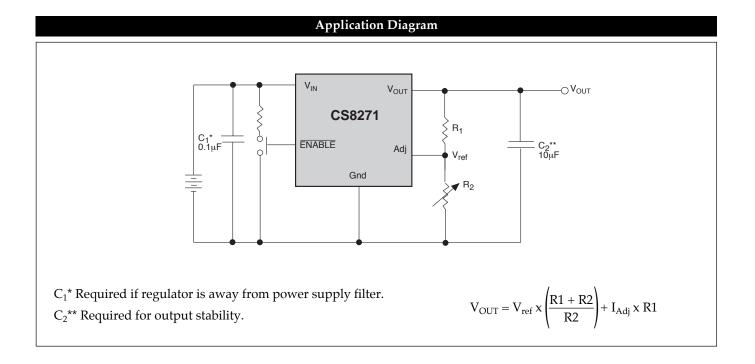
Figure 4: Single output regulator with key performance parameters labeled.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\Theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150^{\circ}\text{C} - \text{T}_{A}}{P_{D}}$$
(2)

The value of $R_{\Theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\Theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.



CS8271

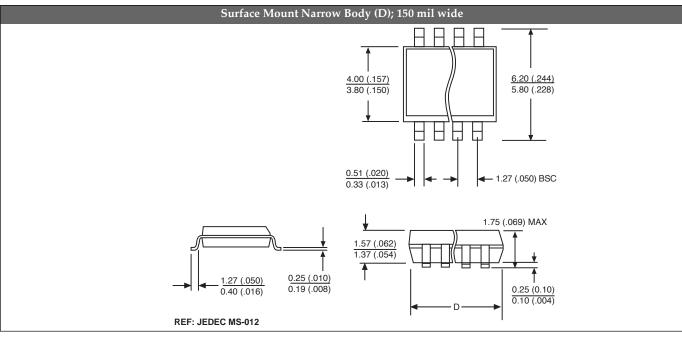
Package Specification

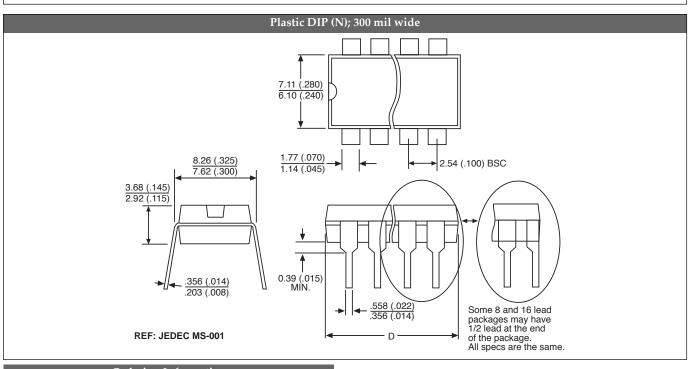
PACKAGE DIMENSIONS IN mm (INCHES)

PACKAGE THERMAL DATA

	D			
Lead Count	Metric English			glish
	Max	Min	Max	Min
8L SOIC	5.00	4.80	.197	.189
8L PDIP	10.16	9.02	.400	.355

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Therm	al Data	8L	8L	
		SOIC	PDIP	
$R_{\Theta JC}$	typ	45	52	°C/W
$R_{\Theta JA}$	typ	165	100	°C/W





Ordering Information

Part Number	Description
CS8271YD8	8L SOIC
CS8271YDR8	8L SOIC (tape & reel)
CS8271YN8	8L PDIP

Cherry Semiconductor Corporation reserves the right to make changes to the specifications without notice. Please contact Cherry Semiconductor Corporation for the latest available information.