TDK SEMICONDUCTOR CORP.

73K322L
CCITT V.23, V.22, V.21 Single-Chip Modem

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DESCRIPTION

The 73K322L is a highly integrated single-chip modem IC which provides the functions needed to construct a CCITT V.23, V.22 and V.21 compatible modem, capable of 1200 or 0-300 bit/s full-duplex operation or 0-1200 bit/s half-duplex operation with or without the back channel over dial-up lines. The 73K322L is an enhancement of the 73K221L single-chip modem with performance characteristics suitable for European and Asian telephone systems. The 73K322L produces either 550 or 1800 Hz guard tone, recognizes and generates a 2100 Hz answer tone, and supports V.21 for 300 Hz FSK operation. It also operates in V.23, 1200 bit/s FSK mode. The 73K322L integrates analog, digital, and switched-capacitor array functions on a single substrate, offering excellent performance and a high level of functional integration in a single 28-pin PLCC or DIP package. The 73K322L operates from a single +5V supply with very low power consumption.

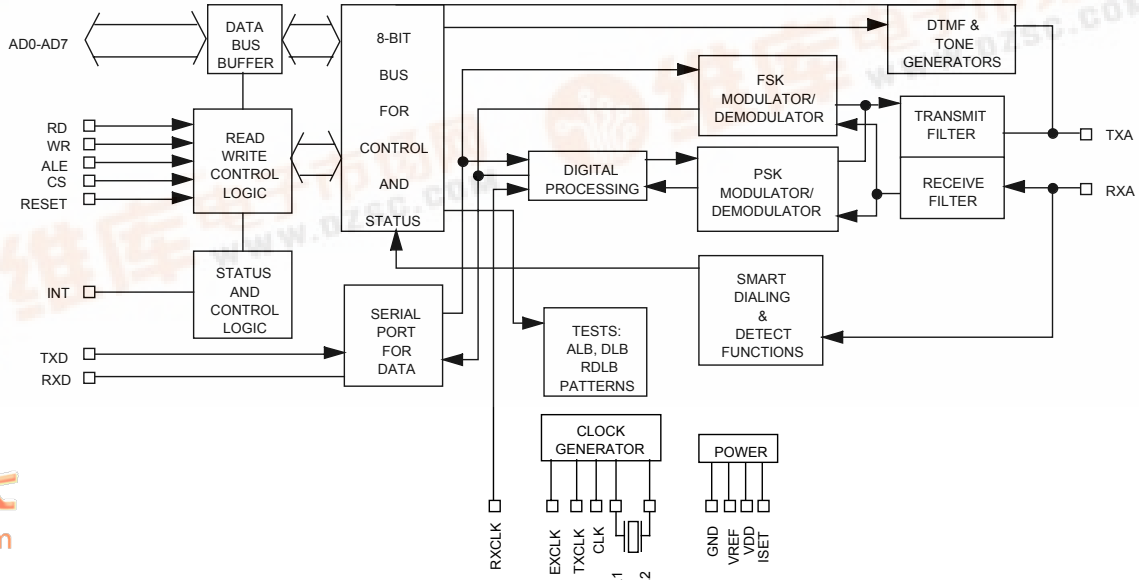
The 73K322L includes the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitor test modes, and a tone generator capable of producing DTMF, answer, calling and 550 or 1800 Hz guard tone. This device supports V.23, V.22 (except mode v) and V.21 modes of operation, allowing both synchronous and

(continued)

FEATURES

- **One-chip CCITT V.23, V.22 and V.21 ITU compatible modem data pump**
- **Full-duplex operation at 0-300 bit/s (FSK) or 600 and 1200 bit/s (DPSK) or 0-1200 bit/s (FSK) forward channel with or without 0-75 bit/s back channel**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial or parallel microprocessor bus for control**
- **Serial port for data transfer**
- **Both synchronous and asynchronous modes of operation**
- **Call progress, carrier, precise answer tone (2100 Hz), calling tone (1300 Hz) and FSK mark detectors**
- **DTMF and 550 or 1800 Hz guard tone generators**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Precise automatic gain control allows 45 dB dynamic range**
- **CMOS technology for low power consumption using 60 mW @ 5V from a single power supply**
- **Surface mount PLCC package available**

BLOCK DIAGRAM



DESCRIPTION (continued)

asynchronous communications. The 73K322L is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial control bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

The 73K322L is ideal for use in either free standing or integral system modem products where multi-standard data communications over the 2-wire switched telephone network is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. The 73K322L is part of TDK Semiconductor Corporation K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

OPERATION

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion. The 73K322L includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data at a regular rate. In Asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC converter. The ASYNC/SYNC converter accepts the data provided on the TXD pin which normally must be 1200 or 600 bit/s +1.0%, -2.5%. The rate converter will then insert or delete stop bits in order to output a signal which is 1200 or 600 bit/s ± 0.01% (± 0.01% is the crystal tolerance).

The SYNC/ASYNC converter also has an extended overspeed mode which allows selection of an output overspeed range of either +1% or +2.3%. In the extended overspeed mode, stop bits are output at 7/8 the normal width.

The serial data stream from the transmit buffer or the rate converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least 2 times N + 3 bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed first through the data descrambler and then through the SYNC/ASYNC converter. The ASYNC/ASYNC converter will reinsert any deleted stop bits and output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

SYNCHRONOUS MODE

The CCITT V.22 standard defines synchronous operation at 600 and 1200 bit/s. Operation is similar to that of the Asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived signal in Internal mode and is connected internally to the RXCLK pin in Slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNCH/SYNCH converter is bypassed when Synchronous mode is selected and data is transmitted out at the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

In DPSK mode the 73K322L modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the V.22 standards. The base-band signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire telephone line. Transmission occurs using either a 1200 Hz (Originate mode) or 2400 Hz carrier (Answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (Answer mode or ALB Originate mode) or a 2400 Hz carrier (Originate mode or ALB Answer mode). The 73K322L uses a phase locked loop coherent demodulation technique for optimum receiver performance.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). V.23 mode uses 1300 and 2100 Hz for the main channel and 390 and 450 Hz for the back channel. The modulation rate of the back channel is up to 75 baud. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are automatically bypassed in the V.21 or V.23 modes.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total receiver dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The detect register is read only and cannot be modified except by modem response to monitored parameters.

SERIAL COMMAND INTERFACE MODE

The serial command interface allows access to the 73K322L control and status registers via a serial command port. In this mode the AD0, AD1 and AD2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The first bit is available after $\overline{RD}$ is brought low and the next seven cycles of EXCLK will then transfer out seven bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the selected register occurs on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, answer tone and weak received signal (long loop condition), special tones such as FSK marking and the 1300 Hz calling tone are also detected. A highly frequency selective call progress detector provides adequate discrimination to accurately detect European call progress signals.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone pairs determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected using the tone register and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	PLCC/PIN DIP NUMBER	TYPE	DESCRIPTION
GND	28	I	System Ground.
VDD	15	I	Power supply input, 5V ±10%. Bypass with 0.1 and 22 µF capacitors to GND.
VREF	26	O	An internally generated reference voltage. Bypass with 0.1 µF capacitor to GND.
ISET	24	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a 0.1 µF capacitor.

PARALLEL MICROPROCESSOR CONTROL INTERFACE

ALE	12	I	Address Latch Enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	I/O	Address/data bus. These bidirectional tri-state multi-plexed lines carry information to and from the internal registers.
$\overline{CS}$	20	I	Chip select. A low on this pin during the falling edge of ALE allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state of $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	I	Read. A low requests a read of the 73K322L internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	25	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.

PARALLEL MICROPROCESSOR CONTROL INTERFACE (continued)

NAME	PLCC/DIP PIN NUMBER	TYPE	DESCRIPTION
$\overline{WR}$	13	I	Write. A low on this informs the 73K322L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are low.

SERIAL MICROPROCESSOR CONTROL INTERFACE

AD0-AD2	4-6	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
AD7	11	I/O	Serial Control Data Input/Output. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	14	I	Read. A low on this input informs the 73K322L that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	13	I	Write. A low on this input informs the 73K322L that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.
Note:	The Serial Control mode is provided by tying ALE high and CS low. In this configuration AD7 becomes the data input and AD0, AD1 and AD2 become the address only. See Serial Control timing diagrams on pages 22 and 23.		

DTE USER INTERFACE

NAME	PLCC/DIP PIN NUMBER	TYPE	DESCRIPTION
EXCLK	19	I	External Clock. This signal is used only in synchronous DPSK transmission when the external timing option has been selected. In the External Timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data available on the TXD pin. Also used for serial control interface.

RS-232 INTERFACE (continued)

NAME	PLCC/DIP PIN NUMBER	TYPE	DESCRIPTION
RXCLK	23	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received DPSK data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present. In V.23 or V.21 mode a clock which is 16 x 1200 (or 16 x 75) or 16 x 300 Hz baud data rate is output, respectively, for driving a UART.
RXD	22	O	Received Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in Synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	O	Transmit Clock. This signal is used only in synchronous DPSK transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the Synchronization mode selection. In Internal Mode the clock is 1200 Hz generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active. In V.23 or V.21 mode the output is a 16 x 1200 (or 16 x 75) or 16 x 300 Hz baud clock, respectively for driving a UART.
TXD	21	I	Transmit Data Input. Serial data for transmission is applied on this pin. In Synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In Asynchronous modes (1200 or 300 baud) no clocking is necessary. DPSK must be 1200/600 bit/s +1%, -2.5% or +2.3%, -2.5% in Extended Overspeed mode.

ANALOG INTERFACE AND OSCILLATOR

RXA	27	I	Received modulated analog signal input from the telephone line interface.
TXA	16	O	Transmit analog output to the telephone line interface.
XTL1 XTL2	2 3	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz Parallel mode crystal and two load capacitors to Ground. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0 and A1 address lines in Serial mode, or the AD0 and AD1 lines in Parallel mode. The AD0 and AD1 lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line.

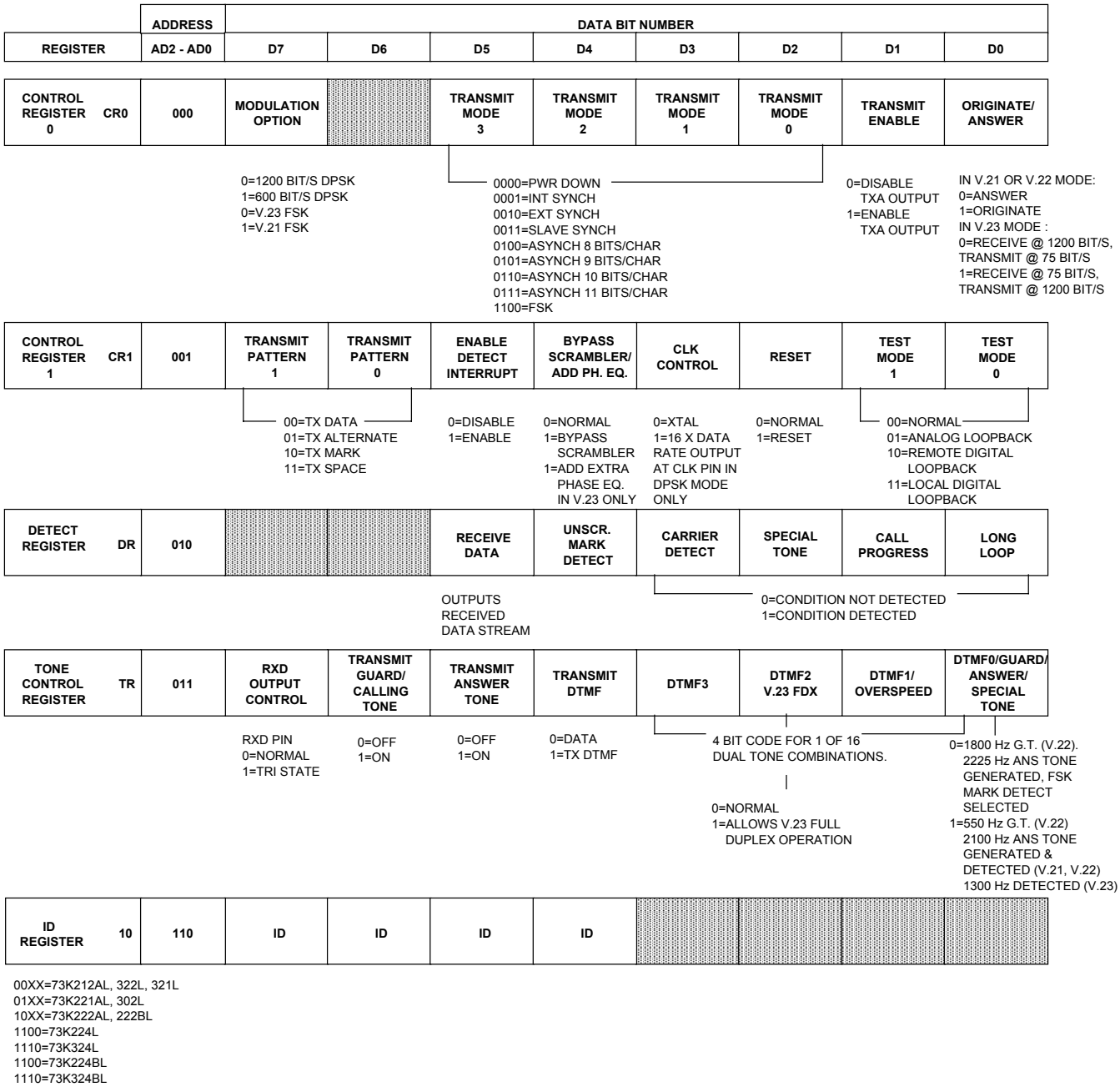
CR1 controls the interface between the microprocessor and the 73K322L internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER/ ADD PH. EQ. (V.23)	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD/ CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ V.23 FDX	DTMF1/ OVERSPEED	DTMF0/GUARD/ ANSWER/SPEC. TONE SELECT
CONTROL REGISTER 2 CR2	100	THESE REGISTER LOCATIONS ARE RESERVED FOR							
CONTROL REGISTER 3 CR3	101	USE WITH OTHER K-SERIES FAMILY MEMBERS							
ID REGISTER ID	110	ID	ID	ID	ID				

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE



00XX=73K212AL, 322L, 321L
01XX=73K221AL, 302L
10XX=73K222AL, 222BL
1100=73K224L
1110=73K324L
1100=73K224BL
1110=73K324BL

CONTROL REGISTER 0

CR0 000	D7	D6	D5	D4	D3	D2	D1	D0
	MODUL. OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects Answer mode in V.21 and V.22 (transmit in high band), receive in low band or in V.23 HDX mode, receive at 1200 bit/s and transmit at 75 bit/s.
		1	Selects Originate mode in V.21 and V.22 (transmit in low band), receive in high band or in V.23 HDX mode, receive at 75 bit/s and transmit at 1200 bit/s.
			Note: This bit works with TR bit D0 to program special tones detected in Tone Register. See detect and tone registers.
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Answer tone and DTMF TX control require TX enable.
D5, D4,D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects Power Down mode. All functions disabled except digital interface.
		0 0 0 1	Internal Synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External Synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz ± 0.01% clock must be supplied externally.
		0 0 1 1	Slave Synchronous mode. Same operation as other Synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects DPSK Asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects DPSK Asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects DPSK Asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects DPSK Asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and 1 or 2 stop bits).
		1 1 0 0	Selects FSK operation.

CONTROL REGISTER 0 (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D6		0	Not used; must be written as a "0."
D7	Modulation Option	D7 D5 D4	Selects:
		0 0 X	PSK Asynchronous mode at 1200 bit/s.
		1 0 X	PSK Asynchronous mode at 600 bit/s.
		0 1 1	FSK CCITT V.23 mode.
		1 1 1	FSK CCITT V.21 mode.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog Loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit carrier from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the CLK pin will be set to the crystal frequency.

CONTROL REGISTER 1 (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D3	CLK Control	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK modes only.
D4	Bypass Scrambler/ Add Phase Equalization (V.23)	0	Selects normal operation. DPSK data is passed through scrambler.
		1	Selects Scrambler Bypass. DPSK data is routed around scrambler in the transmit path. In V.23 mode, additional phase equalization is added to the main channel filters when D4 is set to 1.
D5	Enable Detect	0	Disables interrupt at $\overline{INT}$ pin.
		1	Enables $\overline{INT}$ output. An interrupts will be generated with a change in status of DR bits D1-D4. The special tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA	UNSCR. MARK	CARR. DETECT	SPECIAL TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress band.
D2	Special Tone Detect	0	No special tone detected as programmed by CR0 bit D0 and Tone Register bit D0.
		1	Special tone detected. The detected tone is:
			(1) 2100 Hz answer tone if D0 of TR=1 and the device is in V.21 or V.22 originate mode.
			(2) 1300 Hz calling tone if D0 of TR=1 and the device is in V.21, or V.22 answer mode.
			(3) An FSK mark if D0 of TR = 0.
			Tolerance on special tones is ±3%.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	Unscrambled Mark	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 6.5 ms.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7			Not used.

TONE REGISTER

TR 011	D7	D6	D5	D4	D3	D2	D1	D0
	RXD OUTPUT CONTR.	TRANSMIT GUARD/ CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ V.23 FDX	DTMF 1/ OVER-SPEED	DTMF 0/ G.T./ANSW./ SP. TONE/ SELECT

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0 Guard Tone/ Answer Tone Special Tone/ Detect/Select	D6 D5 D4 D0	D0 interacts with bits D6, D4, and CR0 as shown.
		X X 1 X	Transmit DTMF tones.
		1 X 0 0	Select 1800 Hz guard tone if in V.22 and Answer mode in CR0.
		1 X 0 1	Select 550 Hz guard tone if in V.22 and Answer mode in CR0.
		X X 0 0	Mark of an FSK mode selected in CR0 is to be detected in D2 of DR.
		X X 0 1	2100 Hz answer tone will be detected in D2 of DR if V.21 or V.22 Originate mode is selected in CR0.
			1300 Hz calling tone will be detected in D2 of DR if V.21, or V.22 Answer mode is selected in CR0.
		X 1 0 0	Transmit 2225 Hz Answer Tone
		X 1 0 1	Transmit 2100 Hz Answer Tone
D1	DTMF 1/ Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous DPSK 1200 or 600 bit/s +1.0% -2.5%.
		0 1	Asynchronous DPSK 1200 or 600 bit/s +2.3% -2.5%.
D2	DTMF 2/ V.23 FDX	0	Half-duplex asymmetric operation in V.23 mode.
		1	Full-duplex (4-wire) operation in V.23 mode.
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0	
		0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) are set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3	D2	D1	D0	TONES LOW	HIGH
1	0	0	0	1	697	1209
2	0	0	1	0	697	1336
3	0	0	1	1	697	1477
4	0	1	0	0	770	1209
5	0	1	0	1	770	1336
6	0	1	1	0	770	1477
7	0	1	1	1	852	1209

TONE REGISTER (continued)

TR 011	D7	D6	D5	D4	D3	D2	D1	D0
	RXD OUTPUT CONTR.	TRANSMIT GUARD/ CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ V.23 FDX	DTMF 1/ OVER-SPEED	DTMF 0/ G.T./ANSW./ SP. TONE/ SELECT

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0 (cont.)			KEYBOARD EQUIVALENT / DTMF CODE D3 D2 D1 D0 / TONES LOW HIGH
			8 — 1 0 0 0 — 852 1336
			9 — 1 0 0 1 — 852 1477
			0 — 1 0 1 0 — 941 1336
			* — 1 0 1 1 — 941 1209
			# — 1 1 0 0 — 941 1477
			A — 1 1 0 1 — 697 1633
			B — 1 1 1 0 — 770 1633
			C — 1 1 1 1 — 852 1633
			D — 0 0 0 0 — 941 1633
D4	Transmit DTMF	0	Disable DTMF.
		1	Activate DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	Transmit Answer Tone	0	Disables answer tone generator.
		1	Enables answer tone generator. A 2100 Hz answer tone will be transmitted continuously when the transmit enable bit is set. The device must be in Answer mode. To transmit answer tone, the device must be in DPSK Answer mode.
D6	TX Guard or Calling Tone	0	Disables guard/calling tone generator.
		1	Transmit guard tone if in V.22 and answering; otherwise transmit calling tone, in any other mode including V.23 mode.
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID	ID	ID	ID				

BIT NO.	NAME	CONDITION				DESCRIPTION
D7, D6, D5 D4	Device Identification Signature	D7	D6	D5	D4	Indicates Device:
		0	0	X	X	73K212AL, 73K321L or 73K322L
		0	1	X	X	73K221AL or 73K302L
		1	0	X	X	73K222AL, 73K222BL
		1	1	0	0	73K224L
		1	1	1	0	73K324L
		1	1	0	0	73K224BL
		1	1	1	0	73K324BL

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	7	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VDD Supply voltage		4.5	5	5.5	V
TA, Operating Free-Air Temp.		-40		+85	°C
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
External Components (Refer to Application section for placement.)					
VREF Bypass Capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass Capacitor 1	(External to GND)	0.1			µF
VDD Bypass Capacitor 2	(External to GND)	22			µF
XTL1 Load Capacitor	Depends on crystal characteristics; from pin to GND			40	pF
XTL2 Load Capacitor				20	

DC ELECTRICAL CHARACTERISTICS
(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		8	12	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 KHz			3	mA
Digital Inputs					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Input Capacitance	All Digital Input Pins			10	pF
Digital Outputs					
VOH, Output High Voltage	IOH MIN = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO MAX = 1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = 0 V	-1		-50	µA
CMAX, CLK Output	Maximum Capacitive Load			15	pF
Capacitance					
Inputs	Capacitance, all Digital Input pins			10	pF
XTAL1, 2 Load Capacitors	Depends on crystal characteristics	15		60	pF
CLK	Maximum Capacitive Load			15	pF

DYNAMIC CHARACTERISTICS AND TIMING
(TA = -40°C to +85°C, VDD = Recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
DPSK Modulator					
Carrier Suppression	Measured at TXA	45			dB
Output Amplitude	TX scrambled marks	-11.5	-10	-9	dBm0
FSK Modulator					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+0.35	%
Transmit Level	Transmit Dotting Pattern	-11.5	-10	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern In ALB @ RXD		±3		%
Total Output Jitter	Random Input in ALB @ RXD	-10		+10	%
DTMF Generator					
Freq. Accuracy	Must be in V.22 mode	-0.25		+0.25	%
Output Amplitude	Low Band, V.22 mode	-10	-9	-8	dBm0
Output Amplitude	High Band, V.22 mode	-8	-7	-6	dBm0
Twist	High-Band to Low-Band, V.22 mode	1.0	2.0	3.0	dB
Long Loop Detect	With Sinusoid	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB

Note: Parameters expressed in dBm0 refer to the following definition:

0 dB loss in the Transmit path to the line.

2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Call Progress Detector					
Detect Level	-3 dB points in 285 and 675 Hz	-38			dBm0
Reject Level	Test signal is a 460 Hz sinusoid			-45	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP			40	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP			40	ms
Hysteresis		2			dB
Carrier Detect					
Threshold	DPSK or FSK receive data	-48		-43	dBm0
Delay Time					
V.21		10		20	ms
V.22		15		32	ms
V.23 Forward Channel		6		12	ms
V.23 Back Channel		25		40	ms
Hold Time					
V.21		6		20	ms
V.22		10		24	ms
V.23 Forward Channel		3		8	ms
V.23 Back Channel		10		25	ms
Hysteresis		2			dB
Special Tone Detectors					
Detect Level	See definitions for TR bit D0 mode	-48		-43	dBm0
Delay Time					
2100 Hz answer tone		10		25	ms
1300 Hz calling tone		10		25	ms
390 Hz V.23 back channel mark		20		65	ms

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Special Tone Detectors (continued)					
980 or 1650 Hz V.21 marks		10		25	ms
Hold Time					
2100 Hz answer tone		4		15	ms
1300 Hz calling tone		3		10	ms
390 Hz V.23 back channel mark		10		25	ms
980 or 1650 Hz V.21 marks		5		15	ms
Hysteresis		2			dB
Detect Freq. Range	Any Special Tone	-3		+3	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single Tone out for THD = -50 dB in 0.3 to 3.4 kHz	10 50			kΩ pF
Out of Band Energy	Frequency >12 kHz in all modes			-60	dBm0
Output Impedance	TXA pin, TXA enabled		20	50	Ω
Clock Noise	TXA pin; 76.8 kHz or 122.88 kHz in V.23 main channel		0.1	0.4	mVrms
Carrier VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Freq. Change Assumed		40	100	ms
Recovered Clock					
Capture Range	% of frequency center frequency (center at 1200 Hz)	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms

DYNAMIC CHARACTERISTICS AND TIMING PARALLEL CONTROL INTERFACE

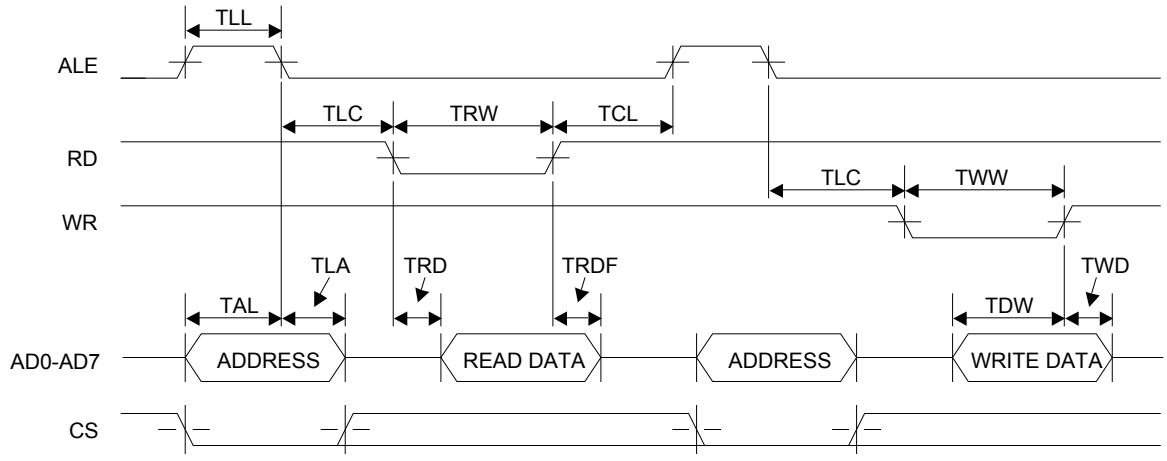
PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Guard Tone Generator					
Tone Accuracy	550 or 1800 Hz	-20		+20	Hz
Tone Level	550 Hz	-4.0	-3.0	-2.0	dB
(Below DPSK Output)	1800 Hz	-7.0	-6.0	-5.0	dB
Harmonic Distortion 700 to 2900 Hz	550 Hz			-50	dB

Timing (Refer to Timing Diagrams)

TAL	$\overline{CS}$	$\overline{CS}$ setup before ALE Low	15			ns
	ADDR	Address setup before ALE low	25			ns
TLA		$\overline{CS}$/Address hold after ALE Low	15			ns
TLC		ALE Low to $\overline{RD}$/$\overline{WR}$ Low	30			ns
TCL		$\overline{RD}$/$\overline{WR}$ Control to ALE High	-5			ns
TRD		Data out from $\overline{RD}$ Low			140	ns
TLL		ALE width	30			ns
TRDF		Data float after RD High			90	ns
TRW		$\overline{RD}$ width	200			ns
TWW		$\overline{WR}$ width	140			ns
TDW		Data setup before $\overline{WR}$ High	25			ns

NOTE: Asserting ALE, CS, and RD or WR concurrently can cause unintentional register accesses. When using non-8031 compatible processors, care must be taken to prevent this from occurring when designing the interface logic.

BUS TIMING DIAGRAM (PARALLEL CONTROL MODE)

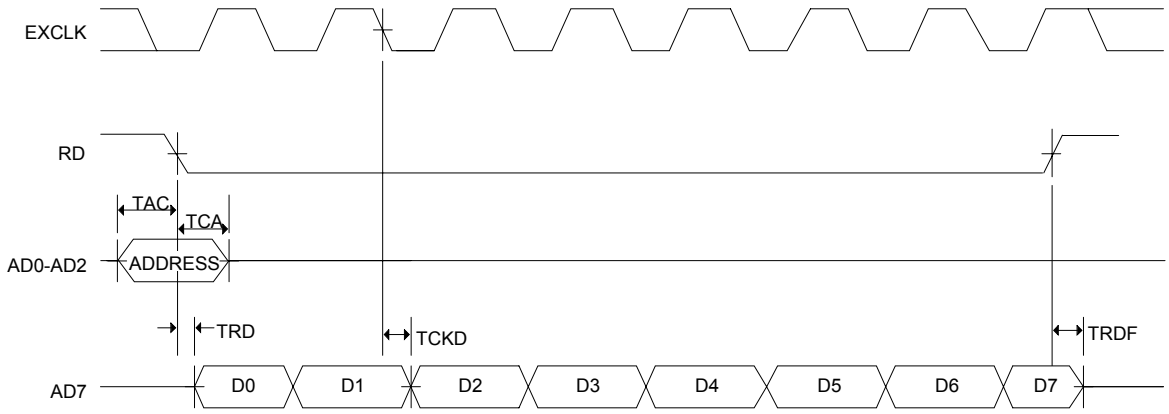


DYNAMIC CHARACTERISTICS AND TIMING SERIAL CONTROL INTERFACE

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Timing (Refer to Timing Diagrams)					
TWW	$\overline{WR}$ width	140		25000	ns
TRD	Data out from $\overline{RD}$ low			140	ns
TRDF	Data float after $\overline{RD}$ high			50	ns
TCKD	Data out after EXCLK Low			200	ns
TCKW	$\overline{WR}$ after EXCLK Low	200			ns
TDCK	Data setup before EXCLK Low	150			ns
TAC	Address setup before control*	50			ns
TCA	Address hold after control*	50			ns
TWH	Data Hold after EXCLK	85			

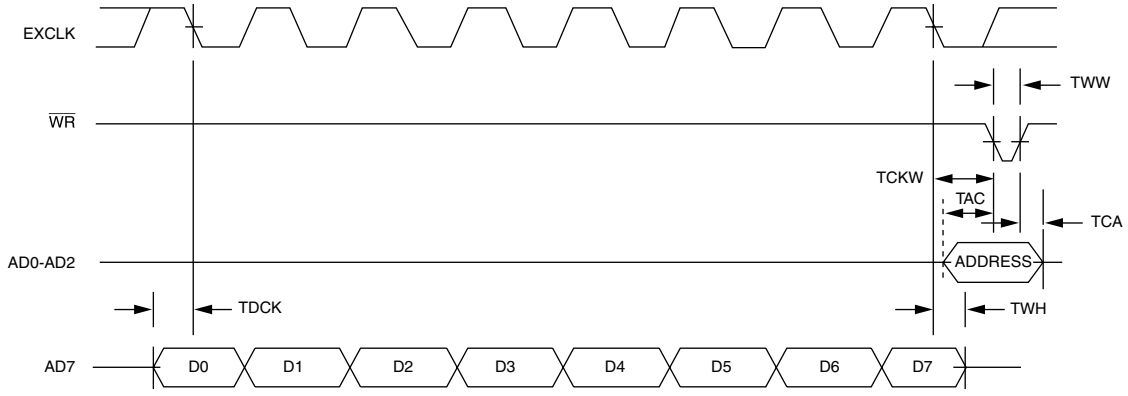
* Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

READ TIMING DIAGRAM (SERIAL CONTROL MODE)



NOTE: At the beginning of a read cycle both EXCLK and RD must be low before bit D0 is output.

WRITE TIMING DIAGRAM (SERIAL VERSION)



73K322L
CCITT V.23, V.22, V.21
Single-Chip Modem

APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the Serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

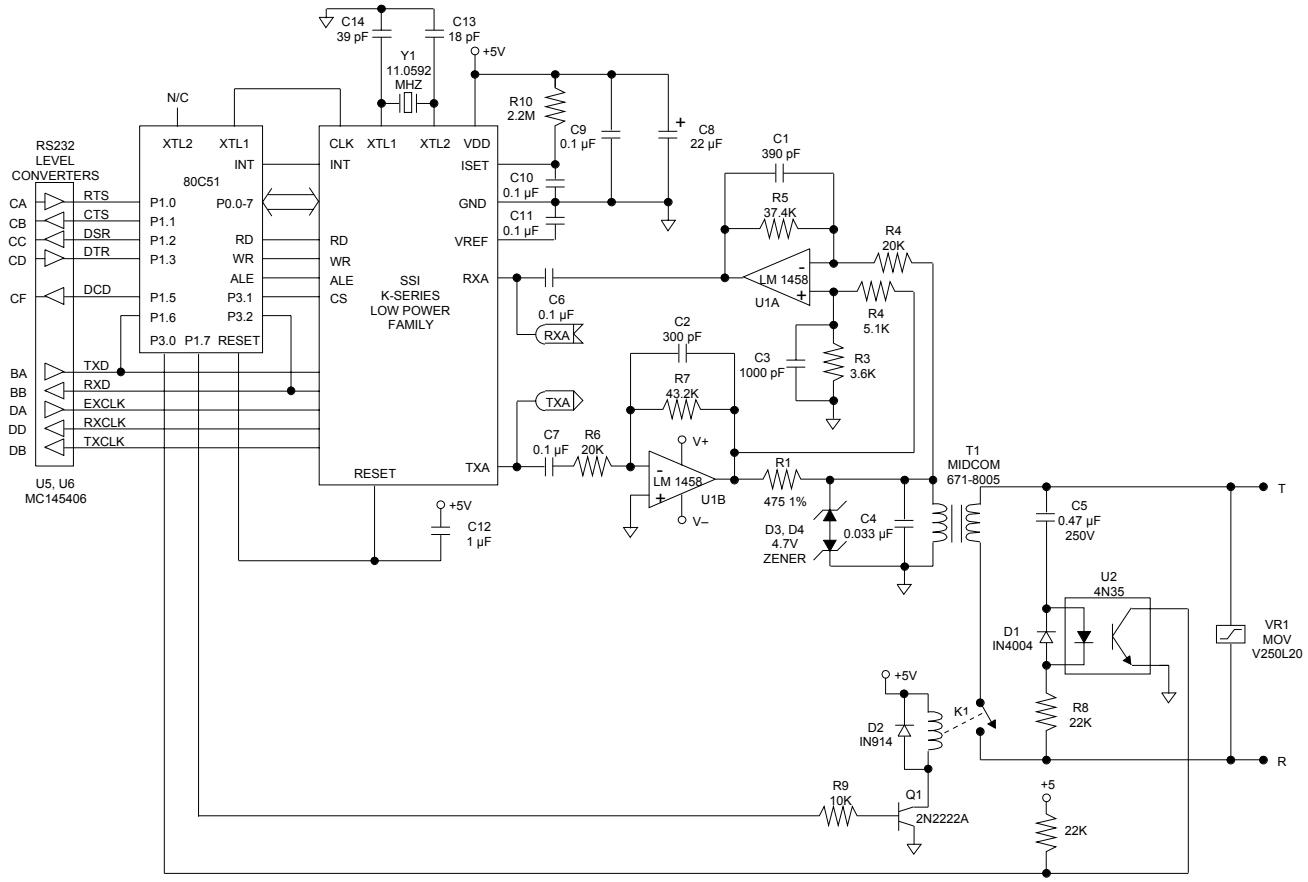


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal Common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

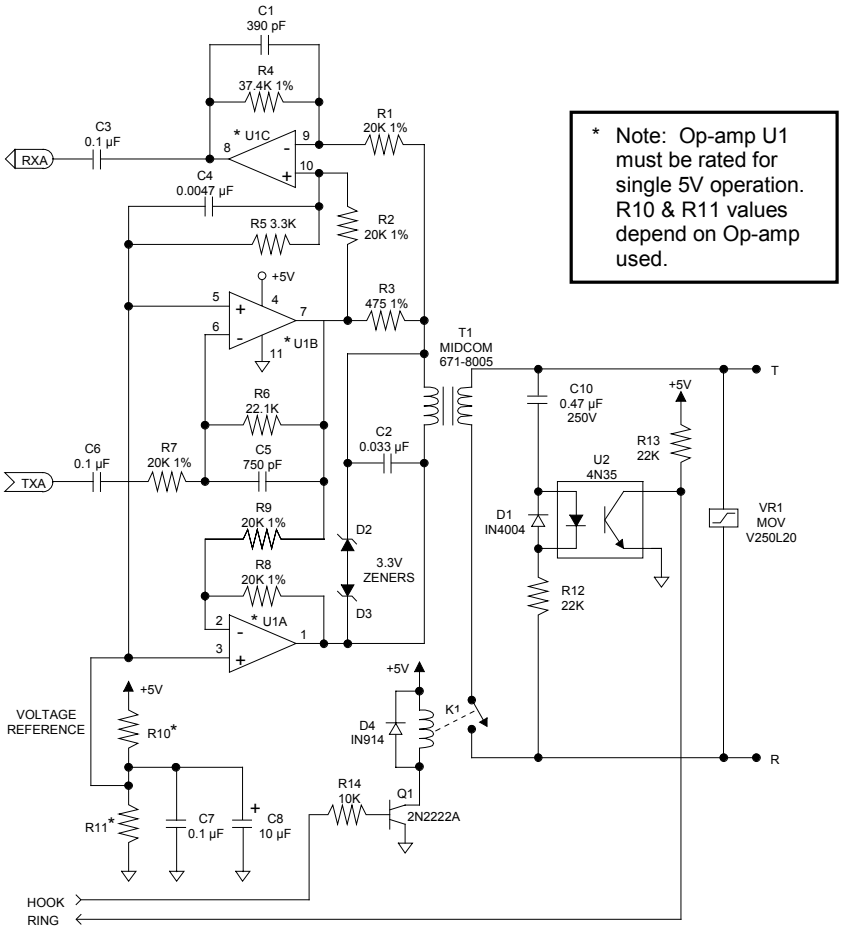


FIGURE 2: Single 5V Hybrid Version

DESIGN CONSIDERATIONS

TDK Semiconductor Corporation's 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals. Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a Parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a Parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K-Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

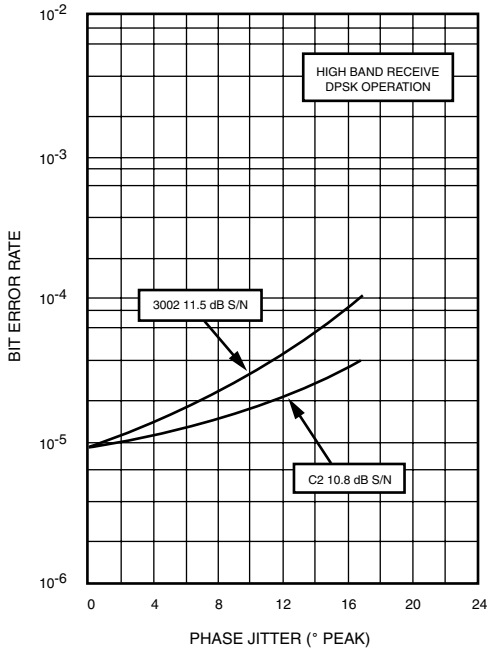
BER vs. S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

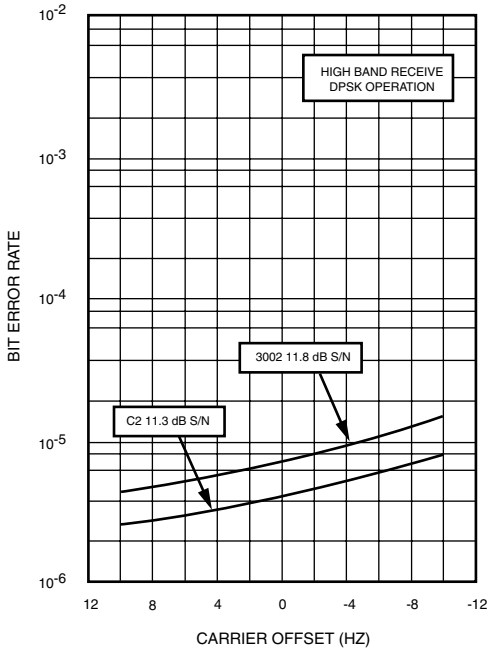
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

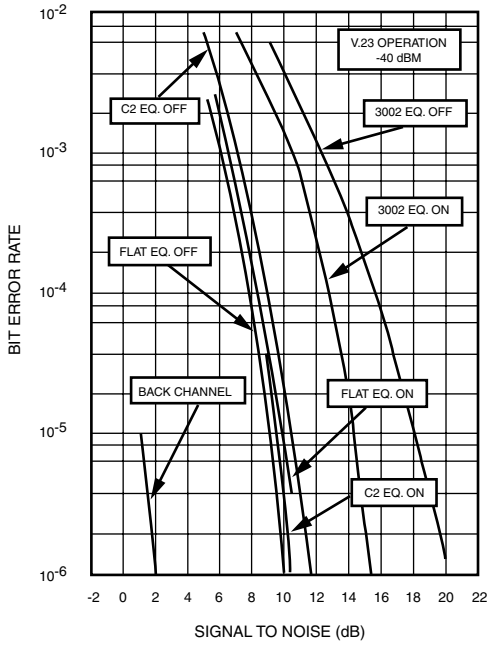
73K322L
BER vs PHASE JITTER



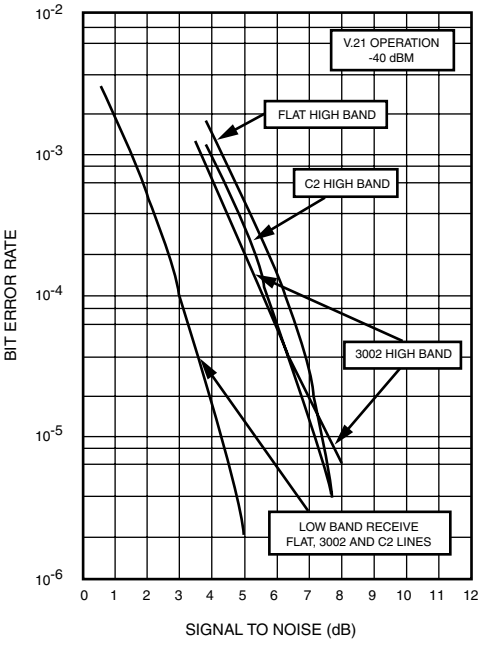
73K322L
BER vs CARRIER OFFSET



73K322L
BER vs S/N (V.23 ONLY)

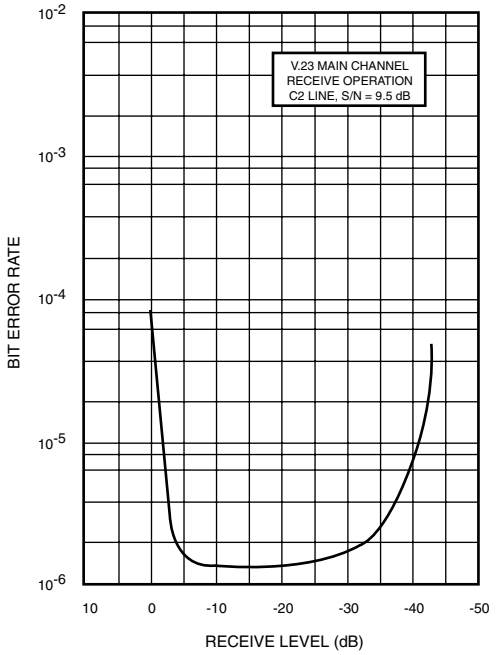


73K322L
BER vs SIGNAL TO NOISE

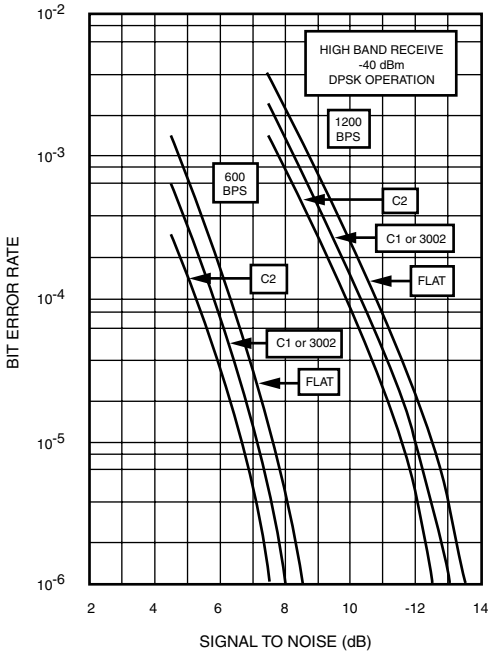


* = “EQ On” Indicates bit CR1 D4 is set for additional phase equalization.

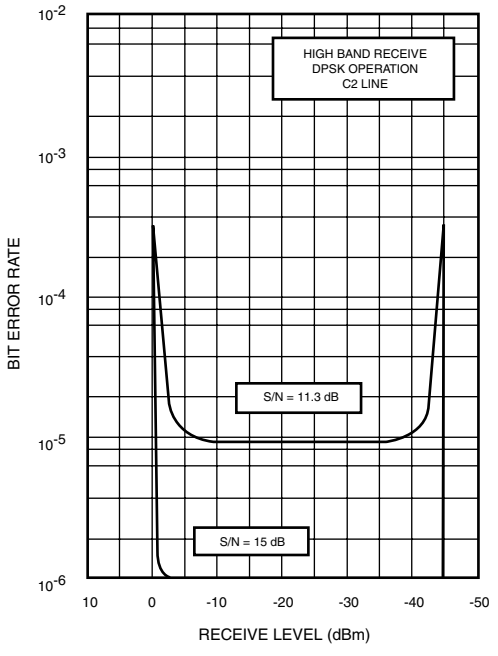
73K322L
BER vs RECEIVE LEVEL (V.23)



73K322L
BER vs SIGNAL TO NOISE



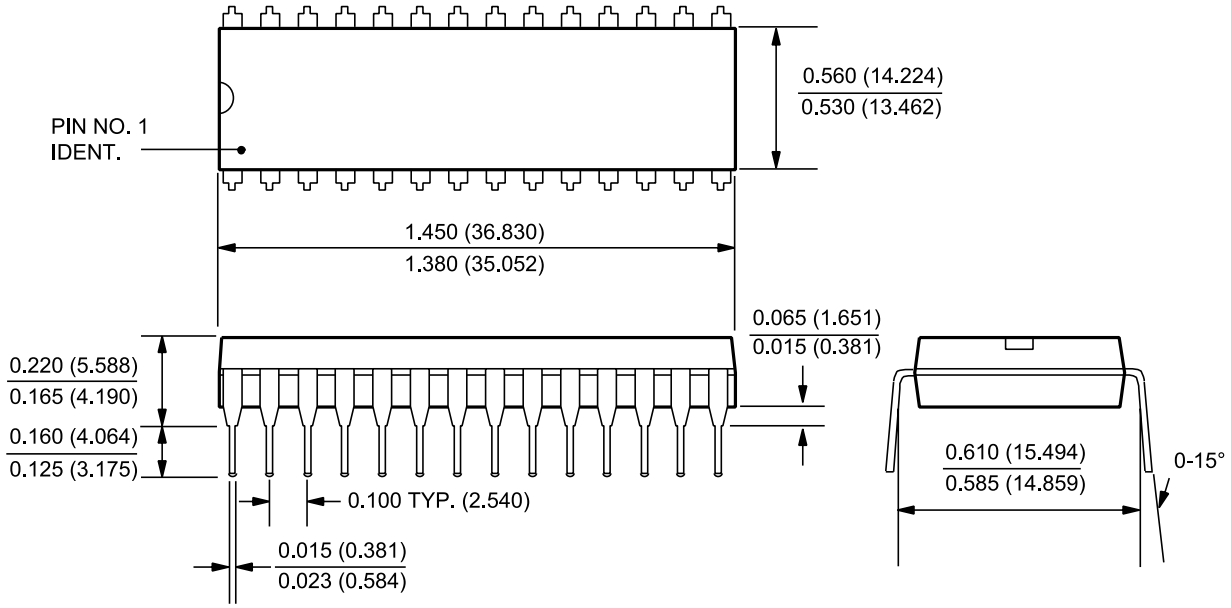
73K322L
BER vs RECEIVE LEVEL



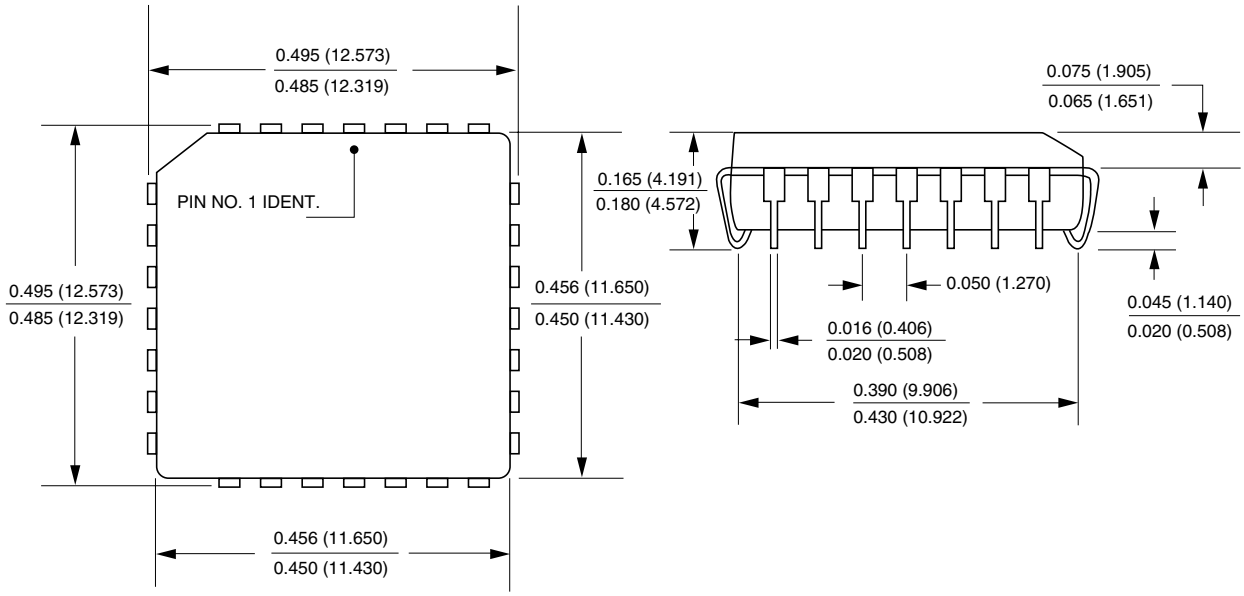
* = “EQ On” Indicates bit CR1 D4 is set for additional phase equalization.

MECHANICAL SPECIFICATIONS

28-Pin DIP



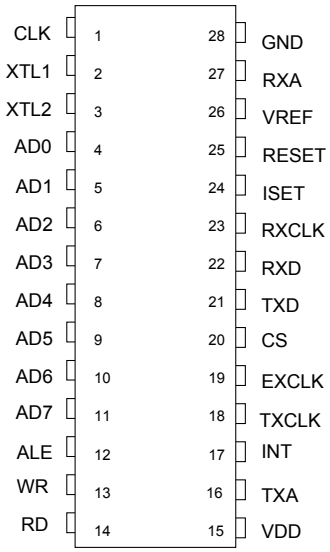
28-Pin PLCC



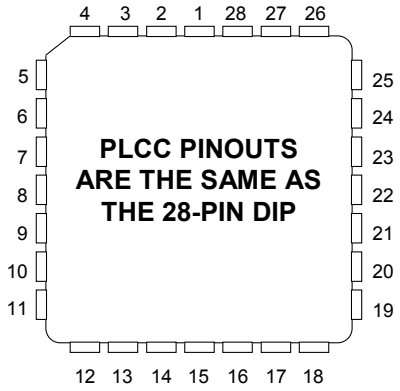
73K322L
CCITT V.23, V.22, V.21
Single-Chip Modem

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



600-Mil
28-Pin DIP
73K322L-IP



28-Pin PLCC
73K322L-IH

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGING MARK
73K322L		
28-Pin 5V Supply		
Plastic Dual-In-Line	73K322L-IP	73K322L-IP
Plastic Leaded Chip Carrier	73K322L-IH	73K322L-IH

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04/24/00- rev. D