

DATA SHEET

74LV273

Octal D-type flip-flop with reset;
positive-edge trigger

Product specification
Supersedes data of 1997 Apr 07
IC24 Data Handbook

1998 May 29

Octal D-type flip-flop with reset; positive edge-trigger

74LV273

FEATURES

- Wide operating voltage: 1.0 to 5.5V
- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between $V_{CC} = 2.7V$ and $V_{CC} = 3.6V$
- Typical V_{OLP} (output ground bounce) $< 0.8V$ @ $V_{CC} = 3.3V$, $T_{amb} = 25^{\circ}C$
- Typical V_{OHV} (output V_{OH} undershoot) $> 2V$ @ $V_{CC} = 3.3V$, $T_{amb} = 25^{\circ}C$
- Ideal buffer for MOS microprocessor or memory
- Common clock and master reset
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV273 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC/HCT273.

The 74LV273 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop.

All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the \overline{MR} input.

The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

QUICK REFERENCE DATA

GND = 0V; $T_{amb} = 25^{\circ}C$; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n ; MR to Q_n	$C_L = 15pF$ $V_{CC} = 3.3V$	12 13	ns
f_{max}	Maximum clock frequency		110	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1 and 2	20	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacitance in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is $V_I = GND$ to V_{CC}

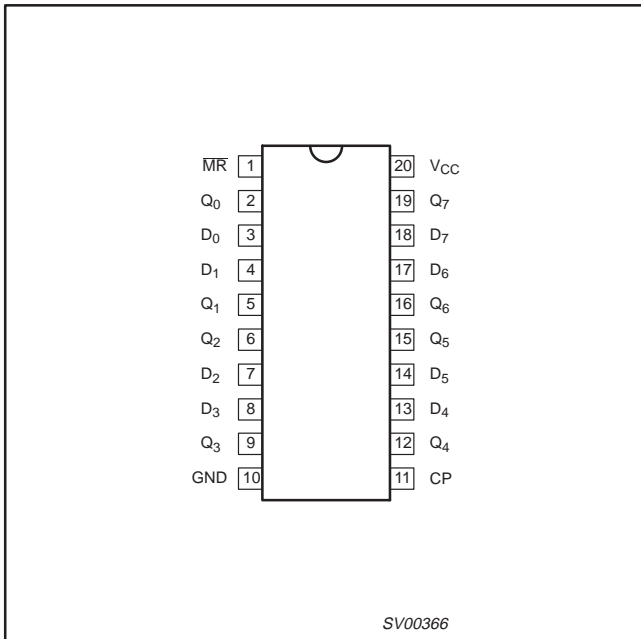
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic DIL	-40°C to +125°C	74LV273 N	74LV273 N	SOT146-1
20-Pin Plastic SO	-40°C to +125°C	74LV273 D	74LV273 D	SOT163-1
20-Pin Plastic SSOP Type II	-40°C to +125°C	74LV273 DB	74LV273 DB	SOT339-1
20-Pin Plastic TSSOP	-40°C to +125°C	74LV273 PW	74LV273PW DH	SOT360-1

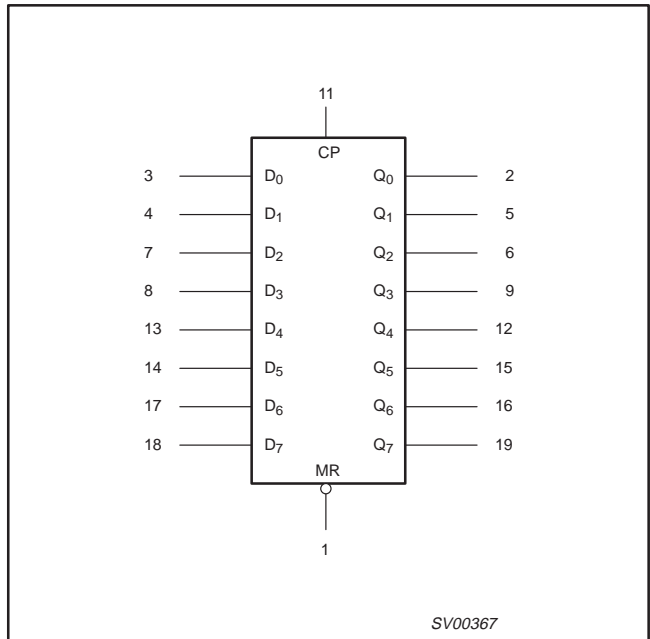
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PIN CONFIGURATION



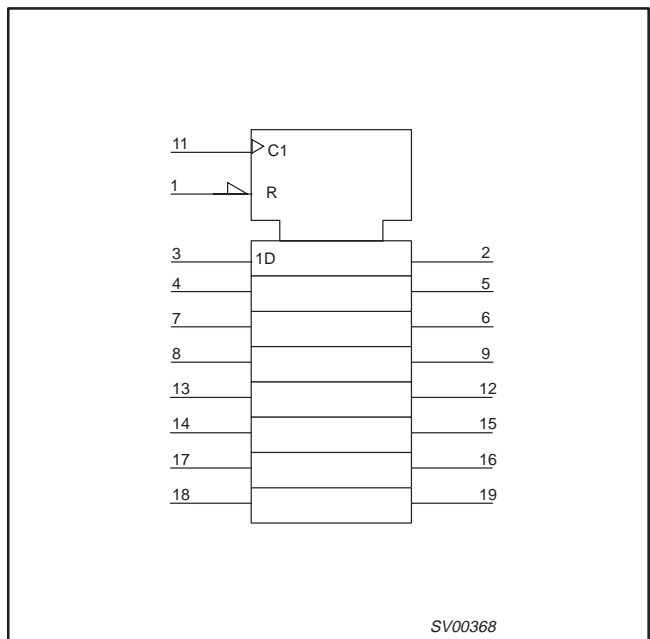
LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	\overline{MR}	Master reset input (active-LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	Flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	Data inputs
10	GND	Ground (0V)
11	CP	Clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	Positive supply voltage

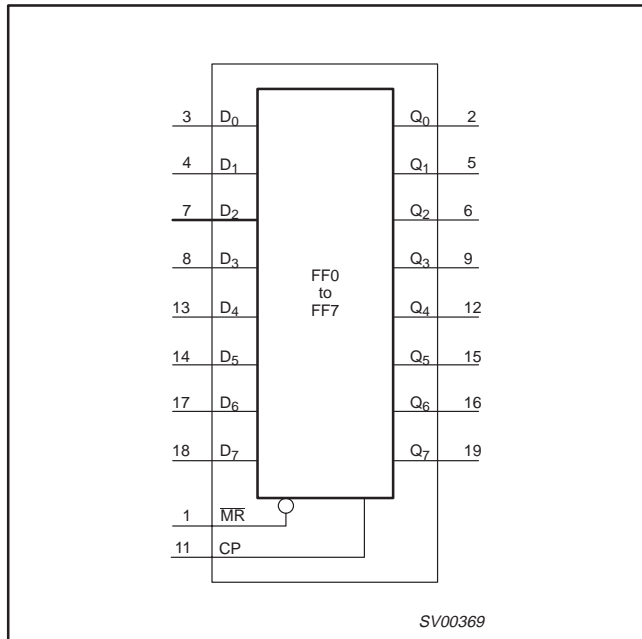
LOGIC SYMBOL (IEEE/IEC)



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FUNCTIONAL DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{\text{MR}}$	CP	D_n	Q_0 to Q_7
Reset (clear)	L	X	X	L
Load ('1')	H	↑	h	H
Load ('0')	H	↑	l	L

- H = HIGH voltage level
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
 L = LOW voltage level
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
 ↑ = LOW-to-HIGH clock transition
 X = Don't care

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	$V_{CC} = 1.0V$ to $2.0V$ $V_{CC} = 2.0V$ to $2.7V$ $V_{CC} = 2.7V$ to $3.6V$ $V_{CC} = 3.6V$ to $5.5V$	– – – –	– – – –	500 200 100 50	ns/V

NOTES:

1. The LV is guaranteed to function down to $V_{CC} = 1.0V$ (input levels GND or V_{CC}); DC characteristics are guaranteed from $V_{CC} = 1.2V$ to $V_{CC} = 5.5V$.

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ABSOLUTE MAXIMUM RATINGS^{1, 2}

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND},$ $\pm I_{CC}$	DC V_{CC} or GND current for types with –standard outputs		50	mA
T_{stg}	Storage temperature range		-65 to +150	°C
P_{TOT}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: -40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR THE LV FAMILY

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP ¹	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	$V_{CC} = 1.2V$	0.9			0.9		V
		$V_{CC} = 2.0V$	1.4			1.4		
		$V_{CC} = 2.7$ to $3.6V$	2.0			2.0		
		$V_{CC} = 4.5$ to $5.5V$	$0.7 \cdot V_{CC}$			$0.7 \cdot V_{CC}$		
V_{IL}	LOW level Input voltage	$V_{CC} = 1.2V$			0.3		0.3	V
		$V_{CC} = 2.0V$			0.6		0.6	
		$V_{CC} = 2.7$ to $3.6V$			0.8		0.8	
		$V_{CC} = 4.5$ to $5.5V$			$0.3 \cdot V_{CC}$		$0.3 \cdot V_{CC}$	
V_{OH}	HIGH level output voltage; all outputs	$V_{CC} = 1.2V; V_I = V_{IH}$ or $V_{IL}; -I_O = 100\mu A$		1.2				V
		$V_{CC} = 2.0V; V_I = V_{IH}$ or $V_{IL}; -I_O = 100\mu A$	1.8	2.0		1.8		
		$V_{CC} = 2.7V; V_I = V_{IH}$ or $V_{IL}; -I_O = 100\mu A$	2.5	2.7		2.5		
		$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; -I_O = 100\mu A$	2.8	3.0		2.8		
		$V_{CC} = 4.5V; V_I = V_{IH}$ or $V_{IL}; -I_O = 100\mu A$	4.3	4.5		4.3		
	HIGH level output voltage; STANDARD outputs	$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; -I_O = 6mA$	2.40	2.82		2.20		V
$V_{CC} = 4.5V; V_I = V_{IH}$ or $V_{IL}; -I_O = 12mA$		3.60	4.20		3.50			
V_{OL}	LOW level output voltage; all outputs	$V_{CC} = 1.2V; V_I = V_{IH}$ or $V_{IL}; I_O = 100\mu A$		0				V
		$V_{CC} = 2.0V; V_I = V_{IH}$ or $V_{IL}; I_O = 100\mu A$		0	0.2		0.2	
		$V_{CC} = 2.7V; V_I = V_{IH}$ or $V_{IL}; I_O = 100\mu A$		0	0.2		0.2	
		$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; I_O = 100\mu A$		0	0.2		0.2	
		$V_{CC} = 4.5V; V_I = V_{IH}$ or $V_{IL}; I_O = 100\mu A$		0	0.2		0.2	
	LOW level output voltage; STANDARD outputs	$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; I_O = 6mA$		0.25	0.40		0.50	V
$V_{CC} = 4.5V; V_I = V_{IH}$ or $V_{IL}; I_O = 12mA$			0.35	0.55		0.65		

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DC CHARACTERISTICS FOR THE LV FAMILY (Continued)

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS				UNIT	
			-40°C to +85°C		-40°C to +125°C			
I_I	Input leakage current	$V_{CC} = 5.5V$; $V_I = V_{CC}$ or GND			1.0		1.0	μA
I_{CC}	Quiescent supply current; MSI	$V_{CC} = 5.5V$; $V_I = V_{CC}$ or GND; $I_O = 0$			20.0		160	μA
ΔI_{CC}	Additional quiescent supply current per input	$V_{CC} = 2.7V$ to $3.6V$; $V_I = V_{CC} - 0.6V$			500		850	μA

NOTE:1. All typical values are measured at $T_{amb} = 25^\circ C$.**AC CHARACTERISTICS**GND = 0V; $t_r = t_f = 2.5ns$; $C_L = 50pF$; $R_L = 1K\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION $V_{CC}(V)$	LIMITS -40 to +85 °C			LIMITS -40 to +125 °C		UNIT
				MIN	TYP ¹	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n	Figure 1	1.2	–	75	–	–	–	ns
			2.0	–	26	32	–	41	
			2.7	–	19	24	–	30	
			3.0 to 3.6	–	14 ²	19	–	24	
			4.5 to 5.5	–	–	16	–	20	
t_{PHL}	Propagation delay MR to Q_n	Figure 2	1.2	–	80	–	–	–	ns
			2.0	–	27	44	–	56	
			2.7	–	20	33	–	41	
			3.0 to 3.6	–	15 ²	26	–	33	
			4.5 to 5.5	–	–	22	–	28	
t_W	Clock pulse width HIGH or LOW	Figure 1	2.0	34	9	–	41	–	ns
			2.7	25	6	–	30	–	
			3.0 to 3.6	20	5 ²	–	24	–	
t_W	Master reset pulse width LOW	Figure 2	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	6 ²	–	24	–	
t_{rem}	Removal time MR to CP	Figure 2	1.2	–	–10	–	–	–	ns
			2.0	5	–4	–	5	–	
			2.7	5	–3	–	5	–	
			3.0 to 3.6	5	–2 ²	–	5	–	
t_{su}	Set-up time D_n to CP	Figure 3	1.2	–	20	–	–	–	ns
			2.0	22	7	–	26	–	
			2.7	16	5	–	19	–	
			3.0 to 3.6	13	4 ²	–	15	–	
t_h	Hold time D_n to CP	Figure 3	1.2	–	–10	–	–	–	ns
			2.0	5	–4	–	5	–	
			2.7	5	–3	–	5	–	
			3.0 to 3.6	5	–2 ²	–	5	–	
f_{max}	Maximum clock pulse frequency	Figure 1	2.0	14	40	–	12	–	MHz
			2.7	19	75	–	16	–	
			3.0 to 3.6	24	100 ²	–	20	–	

NOTE:1. Unless otherwise stated, all typical values are at $T_{amb} = 25^\circ C$.2. Typical value measured at $V_{CC} = 3.3V$.3. Typical value measured at $V_{CC} = 5.0V$.

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AC WAVEFORMS

$V_M = 1.5V$ at $V_{CC} \geq 2.7V \leq 3.6V$
 $V_M = 0.5V * V_{CC}$ at $V_{CC} < 2.7V$ and $\geq 4.5V$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

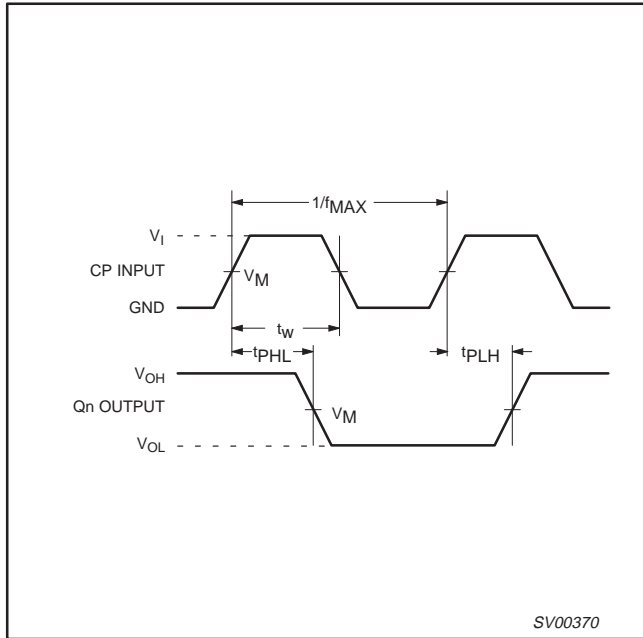


Figure 1. The clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency

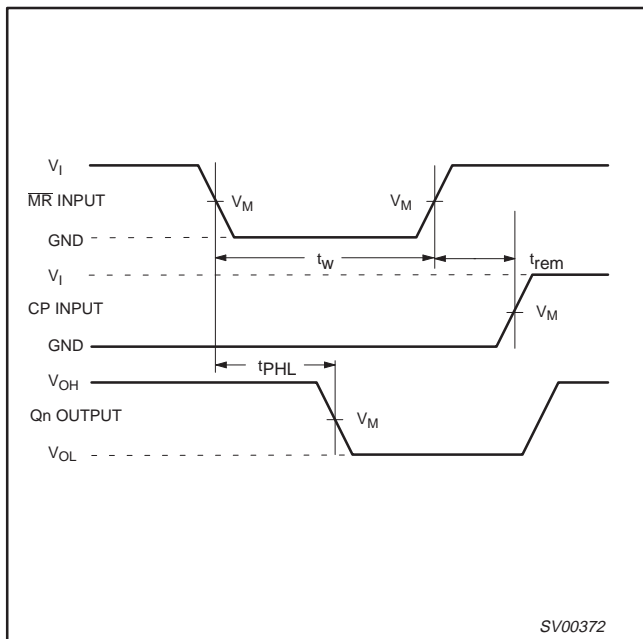


Figure 2. The master reset (MR) pulse width, the master reset to output (Q_n) propagations delay and the master reset to clock (CP) removal time

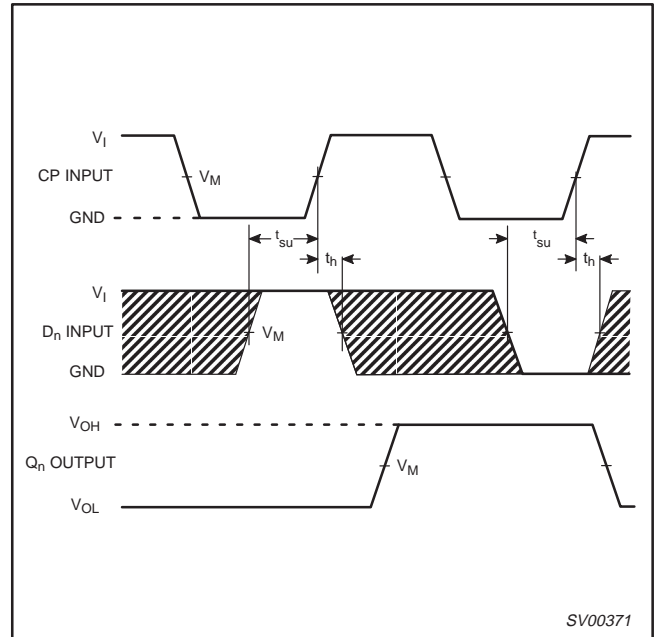


Figure 3. Data set-up and hold times for the data input (D_n)

NOTE:
 The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT

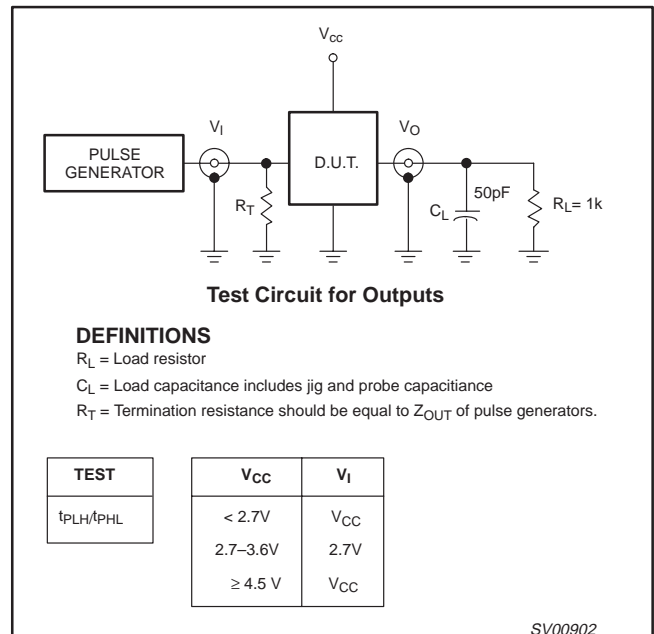


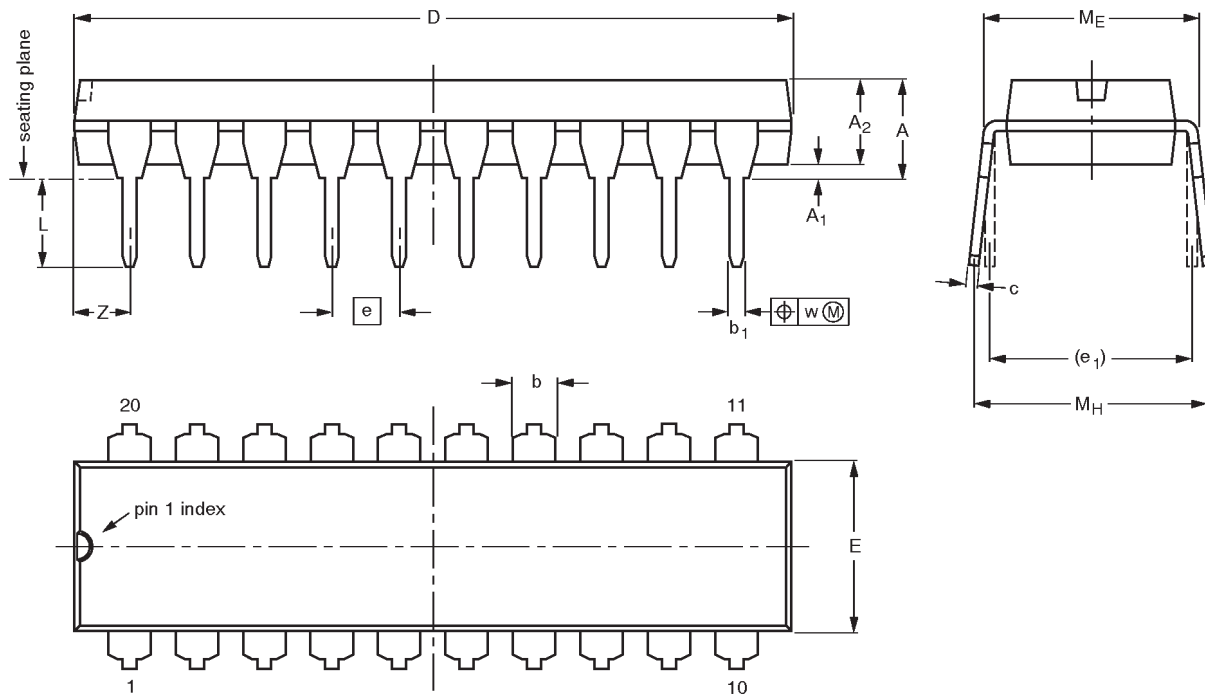
Figure 4. Load circuitry for switching times

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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1




DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

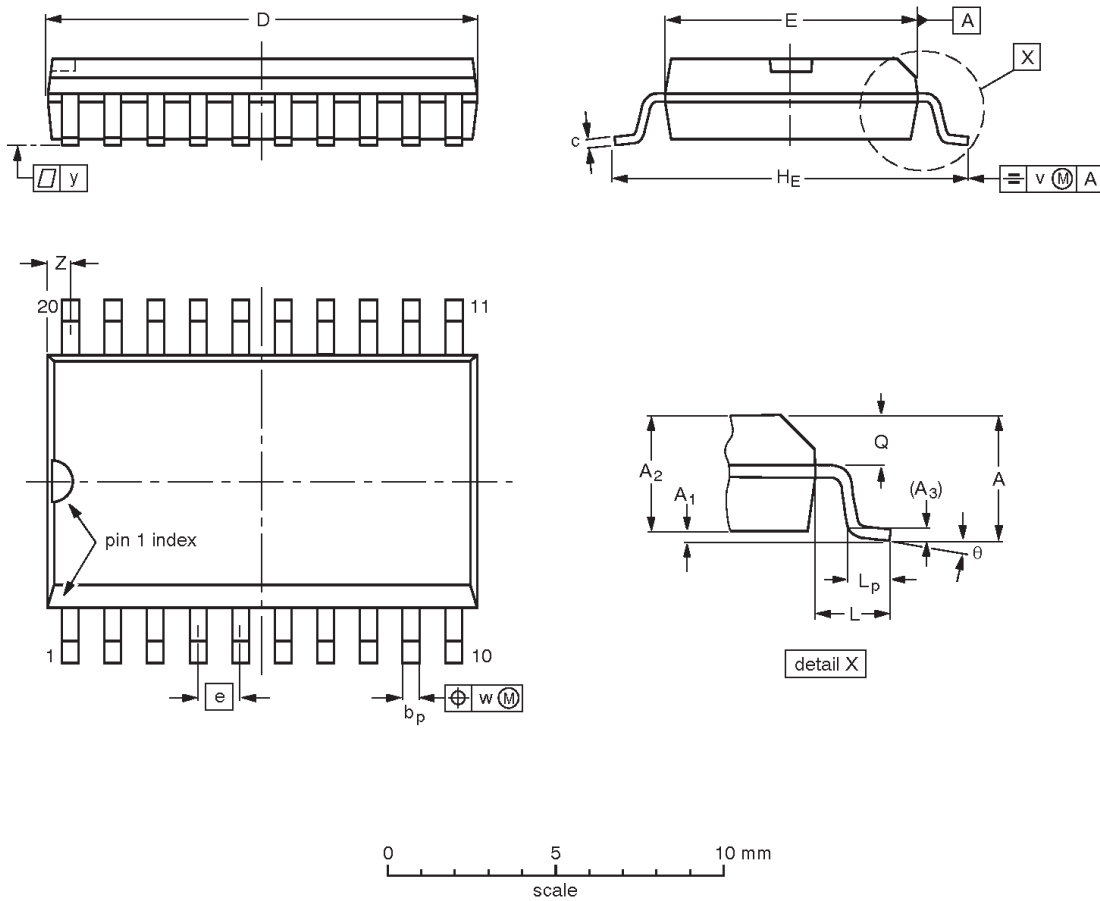
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			-92-11-17 95-05-24

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	HE	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65 0.10	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

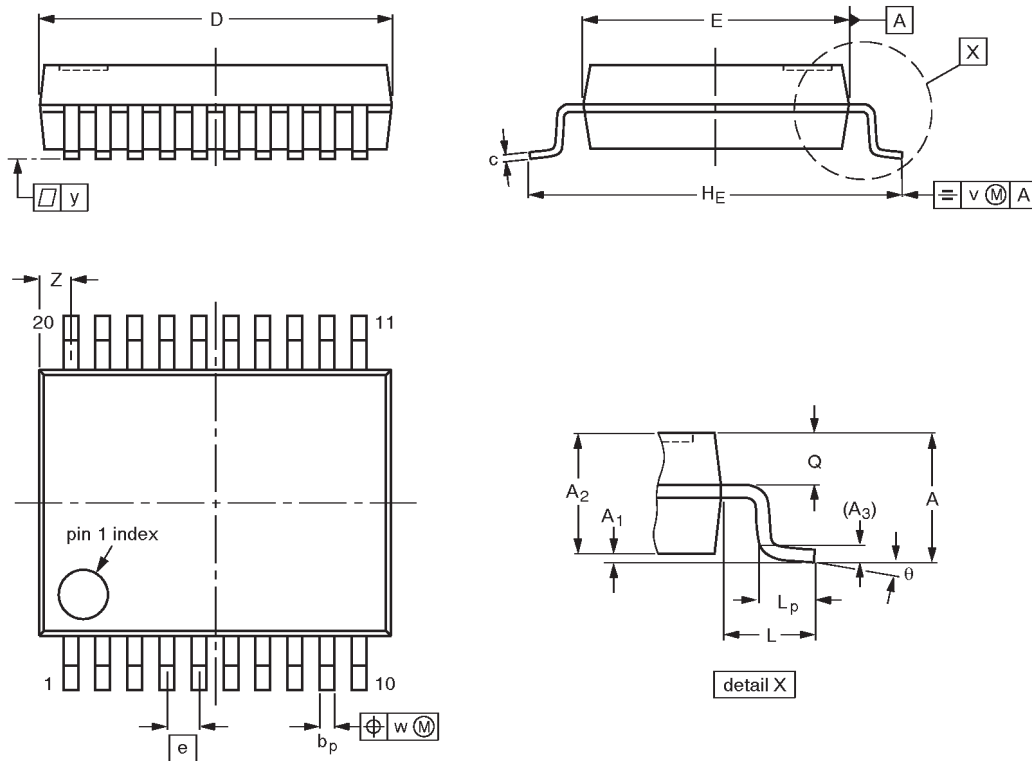
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	IEC	JEDEC	EIAJ		
SOT163-1	075E04	MS-013AC			-92-11-17 95-01-24

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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

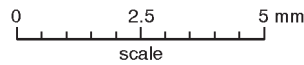
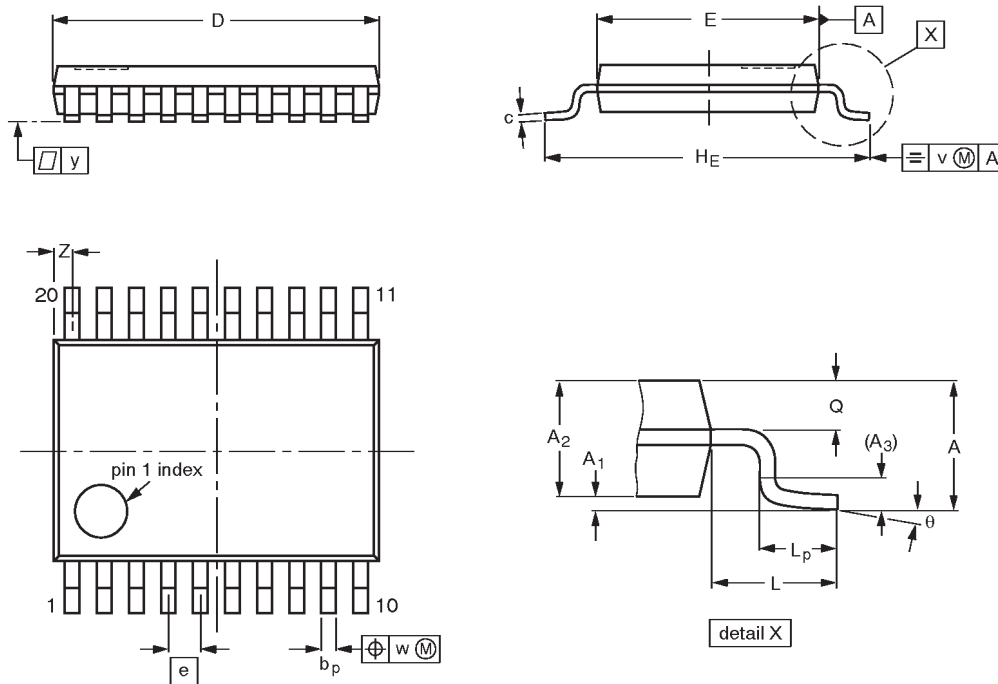
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				93-09-08 95-02-04

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	HE	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				93-06-16 95-02-04

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DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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