

September 1986 Revised February 2000

DM74174

Hex/Quad D-Type Flip-Flop with Clear

General Description

These positive-edge triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input.

Information at the D inputs meeting the setup and hold time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or LOW level, the D input signal has no effect at the output.

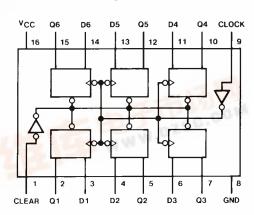
Features

- Contains six flip-flops with single-rail outputs
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
 Buffer/storage registers
 Shift registers
 Pattern generators
- Typical clock frequency 40 MHz
- Typical power dissipation per flip-flop 38 mW

Ordering Code:

Order Number	Package Number	Package Description			
DM74174	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide			

Connection Diagram



Function Table

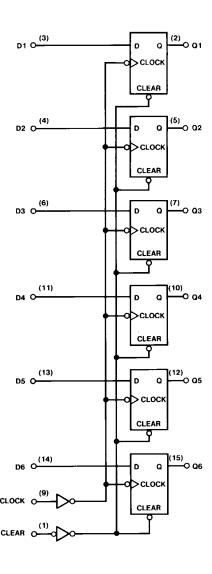
(Each Flip-Flop)

	Inputs			
Clear	Clock	D	Q	
L	X	X	M.A.F.	
Н	1	Н	Н	
H	1	L	L	
Н	L	Χ	Q_0	

- H = HIGH Level (steady state)
- L = LOW Level (steady state)
- X = Don't Care
- \uparrow = Transition from LOW-to-HIGH level

 \mathbf{Q}_0 = The level of \mathbf{Q} before the indicated steady-state input conditions were established.





Absolute Maximum Ratings(Note 1)

Supply Voltage 7V
Input Voltage 5.5V
Operating Free Air Temperature Range 0°C to +70°C
Storage Temperature Range -65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Pa	rameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage		4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage		2			V
V _{IL}	LOW Level Input Voltage				0.8	V
I _{OH}	HIGH Level Output Current				-0.8	mA
I _{OL}	LOW Level Output Current				16	mA
f _{CLK}	Clock Frequency (Note 2)		0		30	MHz
t _W	Pulse Width	Clock LOW	25			
	(Note 2)	Clock HIGH	10			ns
		Clear	20			
t _{SU}	Data Setup Time (Note 2)		20			ns
t _H	Data Hold Time (Note 2)		0			ns
t _{REL}	Clear Release Time (Note 2)		30			ns
T _A	Free Air Operating Temperature		0		70	°C

Note 2: $T_A = 25^{\circ}C$ and $V_{CC} = 5V$.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 3)	Max	Units
VI	Input Clamp Voltage	V _{CC} = Min, I _I = -12 mA			-1.5	V
V _{OH}	HIGH Level	V _{CC} = Min, I _{OH} = Max	2.4			V
	Output Voltage	$V_{IL} = Max, V_{IH} = Min$				V
V _{OL}	LOW Level	V _{CC} = Min, I _{OL} = Max			0.4	V
	Output Voltage	$V_{IH} = Min, V_{IL} = Max$			0.4	v
I _I	Input Current @ Max Input Voltage	$V_{CC} = Max, V_I = 5.5V$			1	mA
I _{IH}	HIGH Level Input Current	V _{CC} = Max, V _I = 2.4V			40	μΑ
I _{IL}	LOW Level Input Current	$V_{CC} = Max, V_I = 0.4V$			-1.6	mA
Ios	Short Circuit Output Current	V _{CC} = Max (Note 4)	-18		-57	mA
Icc	Supply Current	V _{CC} = Max (Note 5)		45	65	mA

Note 3: All typicals are at $V_{CC} = 5V$, $T_A = 25^{\circ}C$.

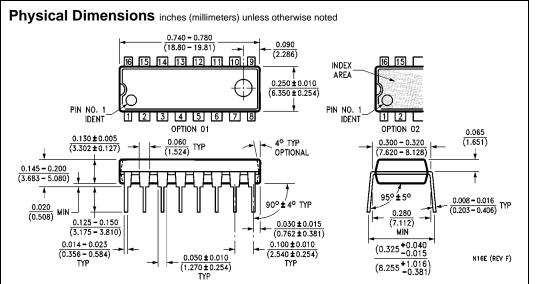
Note 4: Not more than one output should be shorted at a time.

Note 5: With all outputs open and all DATA and CLEAR inputs at 4.5V, I_{CC} is measured after a momentary ground, then 4.5V applied to the CLOCK input.

Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^{\circ}C$

Symbol	Parameter	From (Input)	$R_L = 400\Omega$, $C_L = 15 pF$		Units
		To (Output)	Min	Max	- Onits
f _{MAX}	Maximum Clock Frequency		30		MHz
	Propagation Delay Time	Clock to Any Q		25	ns
	LOW-to-HIGH Level Output				
11112	Propagation Delay Time	Clock to Any Q		25	ns
	HIGH-to-LOW Level Output				
t _{PHL}	Propagation Delay Time	Class to Any O		40	ns
	HIGH-to-LOW Level Output	Clear to Any Q			



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E

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