



October 1993  
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## 74ABT16543 16-Bit Registered Transceiver with 3-STATE Outputs

### General Description

The ABT16543 16-bit transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. Each byte has separate control inputs, which can be shorted together for full 16-bit operation.

### Features

- Back-to-back registers for storage
- Bidirectional data path
- A and B outputs have current sourcing capability of 32 mA and current sinking capability of 64 mA
- Separate control logic for each byte
- 16-bit version of the ABT543
- Separate controls for data flow in each direction
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

### Ordering Code:

Order Number	Package Number	Package Description
74ABT16543CSSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ABT16543CMTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram

Pin Assignment for SSOP and TSSOP

OEAB <sub>1</sub>	1	56	OEBA <sub>1</sub>
LEAB <sub>1</sub>	2	55	LEBA <sub>1</sub>
CEAB <sub>1</sub>	3	54	CEBA <sub>1</sub>
GND	4	53	GND
A <sub>0</sub>	5	52	B <sub>0</sub>
A <sub>1</sub>	6	51	B <sub>1</sub>
V <sub>CC</sub>	7	50	V <sub>CC</sub>
A <sub>2</sub>	8	49	B <sub>2</sub>
A <sub>3</sub>	9	48	B <sub>3</sub>
A <sub>4</sub>	10	47	B <sub>4</sub>
GND	11	46	GND
A <sub>5</sub>	12	45	B <sub>5</sub>
A <sub>6</sub>	13	44	B <sub>6</sub>
A <sub>7</sub>	14	43	B <sub>7</sub>
A <sub>8</sub>	15	42	B <sub>8</sub>
A <sub>9</sub>	16	41	B <sub>9</sub>
A <sub>10</sub>	17	40	B <sub>10</sub>
GND	18	39	GND
A <sub>11</sub>	19	38	B <sub>11</sub>
A <sub>12</sub>	20	37	B <sub>12</sub>
A <sub>13</sub>	21	36	B <sub>13</sub>
V <sub>CC</sub>	22	35	V <sub>CC</sub>
A <sub>14</sub>	23	34	B <sub>14</sub>
A <sub>15</sub>	24	33	B <sub>15</sub>
GND	25	32	GND
CEAB <sub>2</sub>	26	31	CEBA <sub>2</sub>
LEAB <sub>2</sub>	27	30	LEBA <sub>2</sub>
OEAB <sub>2</sub>	28	29	OEBA <sub>2</sub>

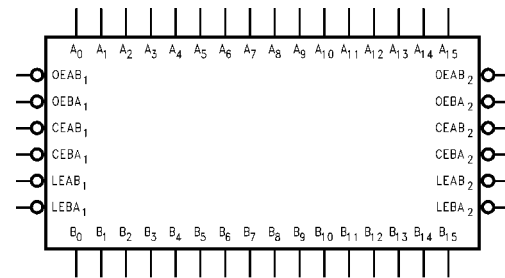
### Pin Descriptions

Pin Names	Description
OEAB <sub>n</sub>	A-to-B Output Enable Input (Active LOW)
OEBA <sub>n</sub>	B-to-A Output Enable Input (Active LOW)
CEAB <sub>n</sub>	A-to-B Enable Input (Active LOW)
CEBA <sub>n</sub>	B-to-A Enable Input (Active LOW)
LEAB <sub>n</sub>	A-to-B Latch Enable Input (Active LOW)
LEBA <sub>n</sub>	B-to-A Latch Enable Input (Active LOW)
A <sub>0</sub> -A <sub>15</sub>	A-to-B Data Inputs or B-to-A 3-STATE Outputs
B <sub>0</sub> -B <sub>15</sub>	B-to-A Data Inputs or A-to-B 3-STATE Outputs

74ABT16543 16-Bit Registered Transceiver with 3-STATE Outputs



## Logic Symbol



## Data I/O Control Table

Inputs			Latch Status	Output Buffers
CEAB <sub>n</sub>	LEAB <sub>n</sub>	OEAB <sub>n</sub>	(Byte n)	(Byte n)
H	X	X	Latched	HIGH Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	HIGH Z
L	X	L	—	Driving

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

A-to-B data flow shown;

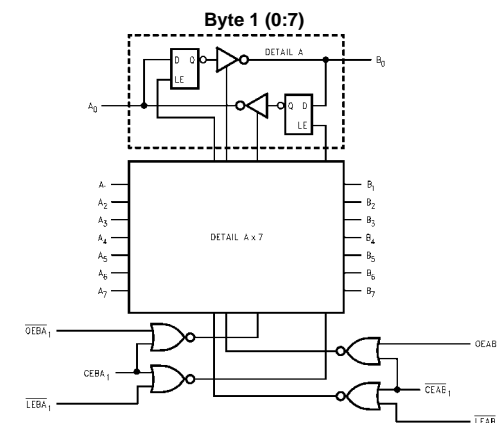
B-to-A flow control is the same, except using  $\overline{\text{CEBA}}_n$ ,  $\overline{\text{LEBA}}_n$  and  $\overline{\text{OEBA}}_n$ .

## Functional Description

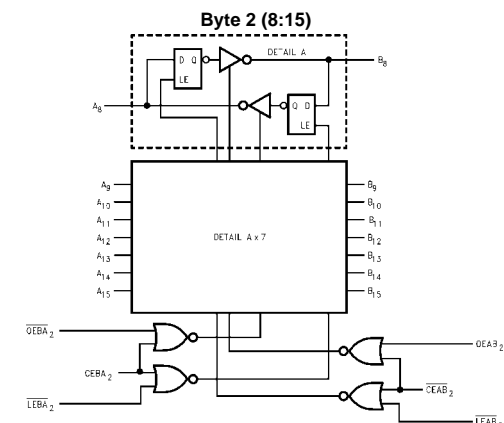
The ABT16543 contains two sets of D-type latches, with separate input and output controls for each. For data flow from A to B, for example, the A to B Enable (CEAB) input must be low in order to enter data from the A port or take data from the B-Port as indicated in the Data I/O Control Table. With  $\overline{\text{CEAB}}$  low, a low signal on (LEAB) input makes the A to B latches transparent; a subsequent low to high transition of the LEAB line puts the A latches in the storage

mode and their outputs no longer change with the A inputs. With  $\overline{\text{CEAB}}$  and OEAB both low, the B output buffers are active and reflect the data present on the output of the A latches. Control of data flow from B to A is similar, but using the  $\overline{\text{CEBA}}$ ,  $\overline{\text{LEBA}}$  and  $\overline{\text{OEBA}}$ . Each byte has separate control inputs, allowing the device to be used as two 8-bit transceivers or as one 16-bit transceiver.

## Logic Diagrams



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



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**Absolute Maximum Ratings**(Note 1)

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +150°C
V <sub>CC</sub> Pin Potential to	
Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or	
Power-Off State	–0.5V to +5.5V
in the HIGH State	–0.5V to V <sub>CC</sub>
Current Applied to Output	
in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

DC Latchup Source Current	–500 mA
Over Voltage Latchup (I/O)	10V

**Recommended Operating Conditions**

Free Air Ambient Temperature	–40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			–1.2	V	Min	I <sub>IN</sub> = –18 mA (Non I/O Pins)
V <sub>OH</sub>	Output HIGH Voltage	2.5					I <sub>OH</sub> = –3 mA, (A <sub>n</sub> , B <sub>n</sub> )
		2.0					I <sub>OH</sub> = –32 mA, (A <sub>n</sub> , B <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage			0.55	V	Min	I <sub>OL</sub> = 64 mA, (A <sub>n</sub> , B <sub>n</sub> )
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 $\mu$ A, (Non-I/O Pins) All Other Pins Grounded
I <sub>IH</sub>	Input HIGH Current			1	$\mu$ A	Max	V <sub>IN</sub> = 2.7V (Non-I/O Pins) ((Note 3) V <sub>IN</sub> = V <sub>CC</sub> (Non-I/O Pins)
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7	$\mu$ A	Max	V <sub>IN</sub> = 7.0V (Non-I/O Pins)
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)			100	$\mu$ A	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub>	Input LOW Current			–1	$\mu$ A	Max	V <sub>IN</sub> = 0.5V (Non-I/O Pins) (Note 3) V <sub>IN</sub> = 0.0V (Non-I/O Pins)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			10	$\mu$ A	0V–5.5V	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> ); OEAB or CEAB = 2V
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			–10	$\mu$ A	0V–5.5V	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> ); OEAB or CEAB = 2V
I <sub>OS</sub>	Output Short-Circuit Current	–100		–275	mA	Max	V <sub>OUT</sub> = 0V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current			50	$\mu$ A	Max	V <sub>OUT</sub> = V <sub>CC</sub> (A <sub>n</sub> , B <sub>n</sub> )
I <sub>ZZ</sub>	Bus Drainage Test			100	$\mu$ A	0.0V	V <sub>OUT</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> ); All Others GND
I <sub>CCH</sub>	Power Supply Current			1.0	mA	Max	All Outputs HIGH
I <sub>CCL</sub>	Power Supply Current			60	mA	Max	All Outputs LOW
I <sub>CCZ</sub>	Power Supply Current			1.0	mA	Max	Outputs 3-STATE All Others at V <sub>CC</sub> or GND
I <sub>CCT</sub>	Additional I <sub>CC</sub> /Input			2.5	mA	Max	V <sub>I</sub> = V <sub>CC</sub> – 2.1V All Others at V <sub>CC</sub> or GND
I <sub>CCD</sub>	Dynamic I <sub>CC</sub> No Load (Note 3)			0.25	mA/MHz	Max	Outputs Open, CEAB, OEAB, LEAB = GND, CEBA = V <sub>CC</sub> . One Bit Toggling, 50% Duty Cycle

**Note 3:** Guaranteed but not tested.

## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +85°C V <sub>CC</sub> = 4.5V–5.5V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	1.5	3.0	5.7	1.5	5.7	ns
t <sub>PHL</sub>	A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>						
t <sub>PLH</sub>	Propagation Delay	1.5	3.0	5.5	1.5	5.5	ns
t <sub>PHL</sub>	$\overline{\text{LEAB}}_n$ to B <sub>n</sub> , $\overline{\text{LEBA}}_n$ to A <sub>n</sub>						
t <sub>PZH</sub>	Enable Time	1.5	2.8	5.2	1.5	5.2	ns
t <sub>PZL</sub>	$\text{OEBA}_n$ or $\text{OEAB}_n$ to A <sub>n</sub> or B <sub>n</sub>						
t <sub>PHZ</sub>	Disable Time	1.6	3.1	6.0	1.6	6.0	ns
t <sub>PLZ</sub>	$\text{OEAB}_n$ or $\text{OEBA}_n$ to A <sub>n</sub> or B <sub>n</sub>						
t <sub>PZH</sub>	Enable Time	1.5	3.1	6.2	1.5	6.2	ns
t <sub>PZL</sub>	$\text{CEBA}_n$ or $\text{CEAB}_n$ to A <sub>n</sub> or B <sub>n</sub>						
t <sub>PHZ</sub>	Disable Time	1.7	3.2	6.3	1.7	6.3	ns
t <sub>PLZ</sub>	$\text{CEBA}_n$ or $\text{CEAB}_n$ to A <sub>n</sub> or B <sub>n</sub>						

## AC Operating Requirements

(SSOP Package)

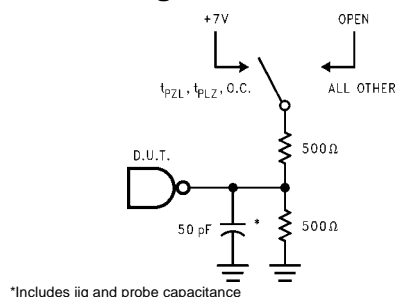
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		T <sub>A</sub> = -55°C to +85°C V <sub>CC</sub> = 4.5V–5.5V C <sub>L</sub> = 50 pF		Units
		Min	Max	Min	Max	
t <sub>S</sub> (H)	Setup Time, HIGH or LOW	2.0		2.0		ns
t <sub>S</sub> (L)	A <sub>n</sub> or B <sub>n</sub> to $\overline{\text{LEBA}}_n$ or $\overline{\text{LEAB}}_n$	2.0		2.0		
t <sub>H</sub> (H)	Hold Time, HIGH or LOW	1.0		1.0		ns
t <sub>H</sub> (L)	A <sub>n</sub> or B <sub>n</sub> to $\overline{\text{LEBA}}_n$ or $\overline{\text{LEAB}}_n$	1.0		1.0		
t <sub>W</sub> (L)	Pulse Width, LOW	3.0		3.0		ns

## Capacitance

Symbol	Parameter	Typ	Units	Conditions T <sub>A</sub> = 25°C
C <sub>IN</sub>	Input Capacitance	5.0	pF	V <sub>CC</sub> = 0V (non I/O pins)
C <sub>I/O</sub> (Note 4)	Output Capacitance	11.0	pF	V <sub>CC</sub> = 5.0V (A <sub>n</sub> , B <sub>n</sub> )

**Note 4:** C<sub>I/O</sub> is measured at frequency, f = 1 MHz, per MIL-STD-883, Method 3012.

## AC Loading



\*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

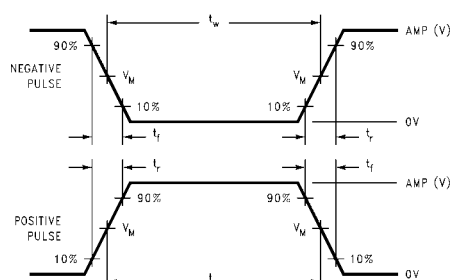


FIGURE 2.  $V_M = 1.5V$

### Input Pulse Requirements

Amplitude	Rep. Rate	$t_w$	$t_r$	$t_f$
3V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

## AC Waveforms

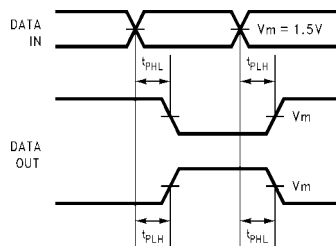


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

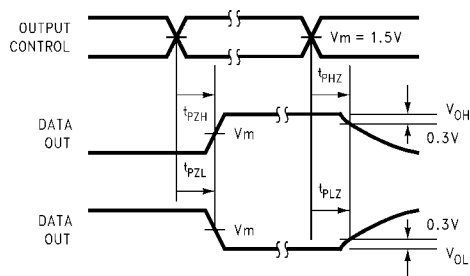


FIGURE 6. 3-STATE Output HIGH and LOW Enable and Disable Times

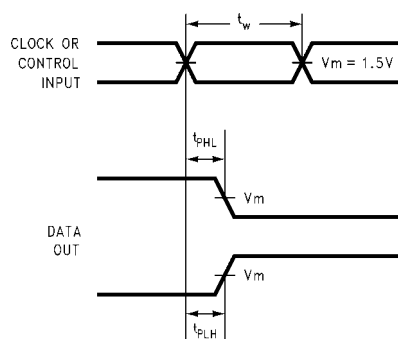


FIGURE 5. Propagation Delay, Pulse Width Waveforms

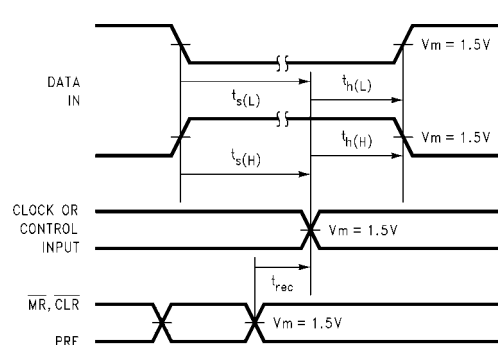
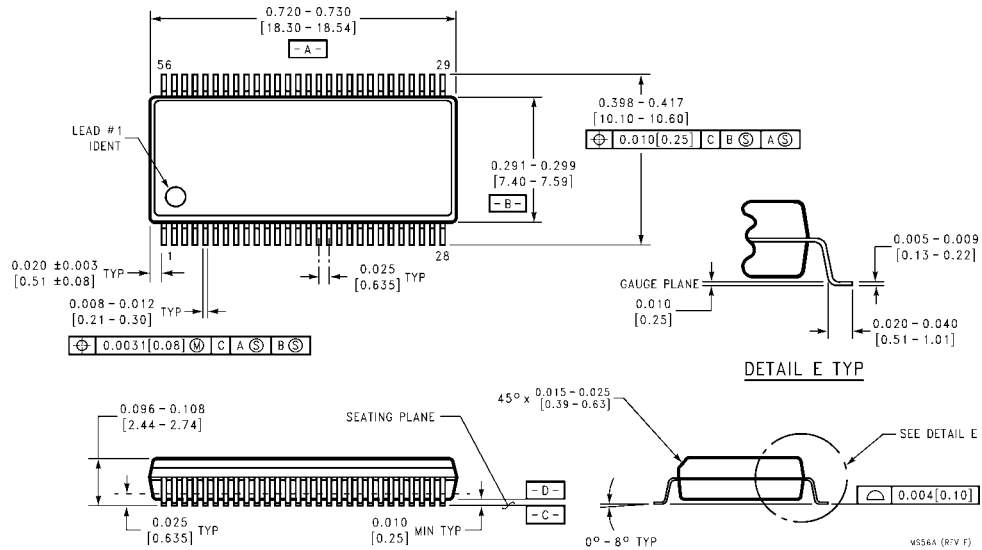


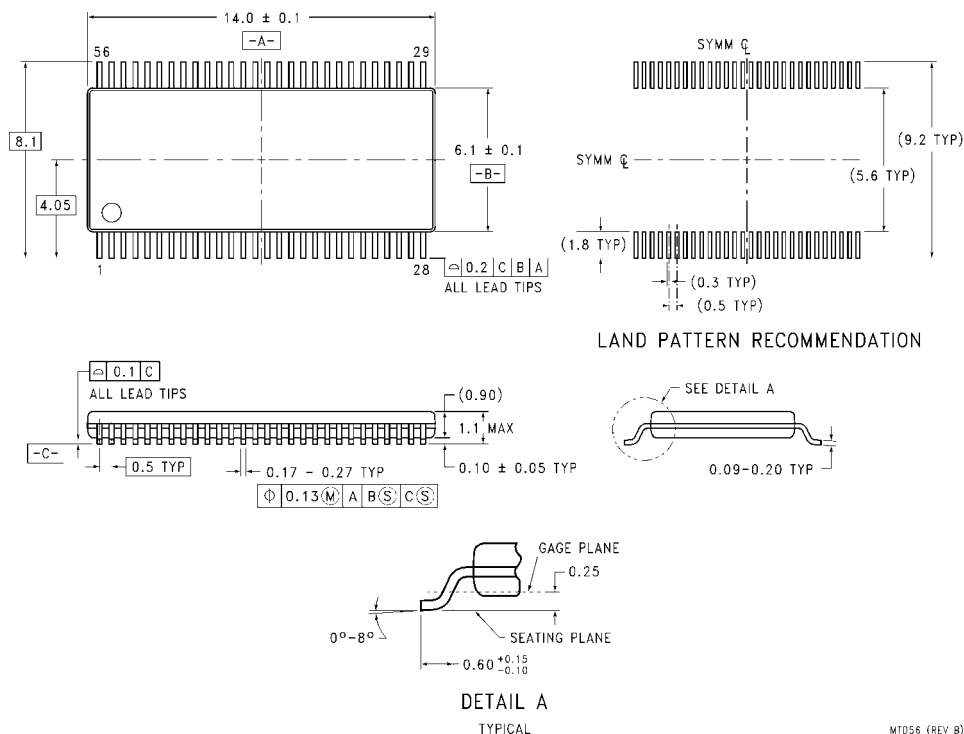
FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

# Physical Dimensions inches (millimeters) unless otherwise noted



**56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide  
Package Number MS56A**

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide  
Package Number MTD56

MTD56 (REV B)

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