DATA SHEET

74ABT16652
74ABTH16652
16-bit transceiver/register, non-inverting (3-State)

Product specification
Supersedes data of 1995 Aug 17
IC23 Data Handbook

1998 Feb 27

Philips Semiconductors

16-bit transceiver/register, non-inverting (3-State)

74ABT16652
74ABTH16652

FEATURES

- Independent registers for A and B buses
- Multiple V_{CC} and GND pins minimize switching noise
- Power-up 3-State
- 74ABTH16652 incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Power-up reset
- Live insertion/extraction permitted
- Multiplexed real-time and stored data
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16652 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16652 transceiver/register consists of two sets of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes HIGH. Output Enable (nOEAB, (n$\overline{\text{OEBA}}$) and Select (n$\overline{\text{SAB}}$, n$\overline{\text{SBA}}$) pins are provided for bus management.

Two options are available, 74ABT16652 which does not have the bus-hold feature and 74ABTH16652 which incorporates the bus-hold feature.

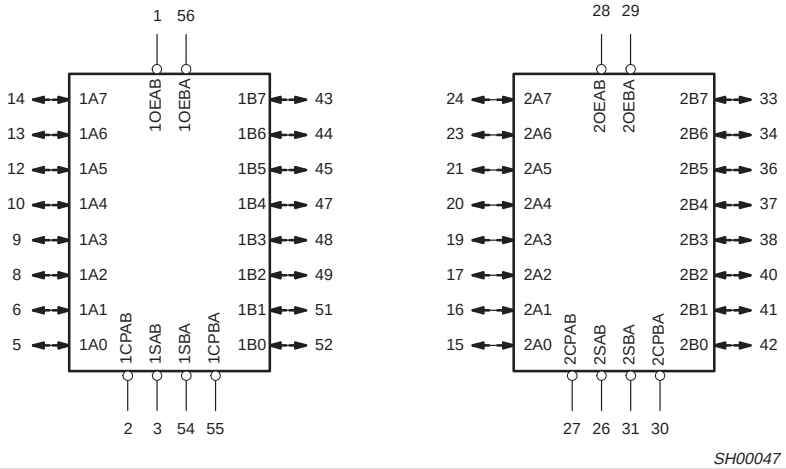
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx	C_L = 50pF; V_{CC} = 5V	2.3 1.8	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} =5.5V	500	µA
I_{CCL}		Outputs low; V_{CC} = 5.5V	8	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16652 DL	BT16652 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16652 DGG	BT16652 DGG	SOT364-1
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16652 DL	BH16652 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16652 DGG	BH16652 DGG	SOT364-1

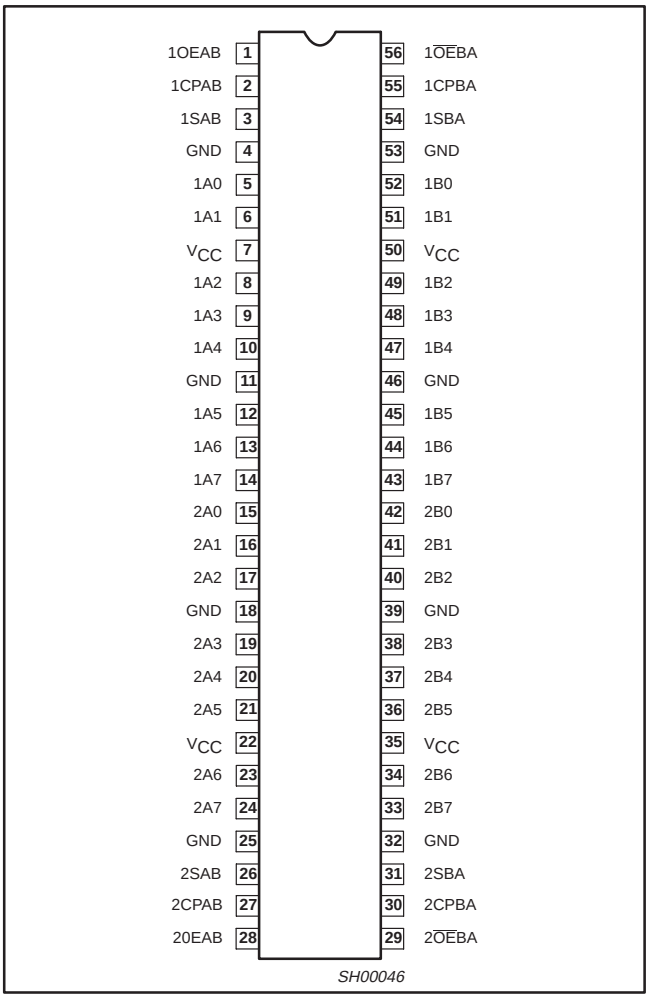
LOGIC SYMBOL



16-bit transceiver/register, non-inverting (3-State)

74ABT16652
74ABTH16652

PIN CONFIGURATION



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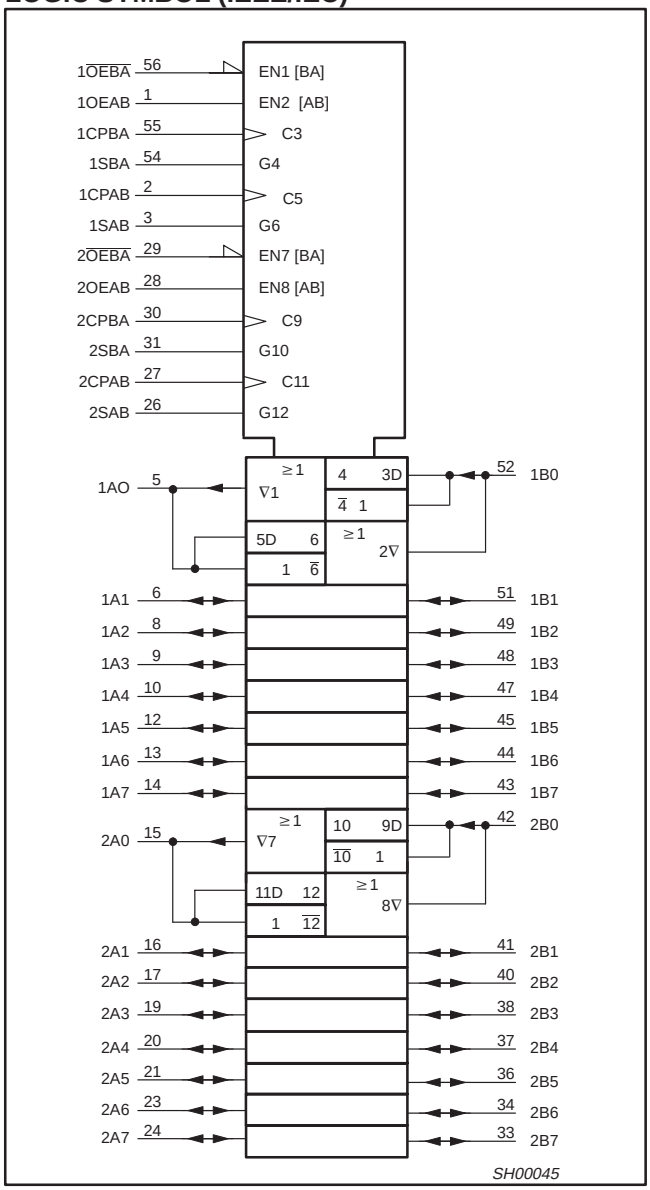
LOGIC SYMBOL (IEEE/IEC)



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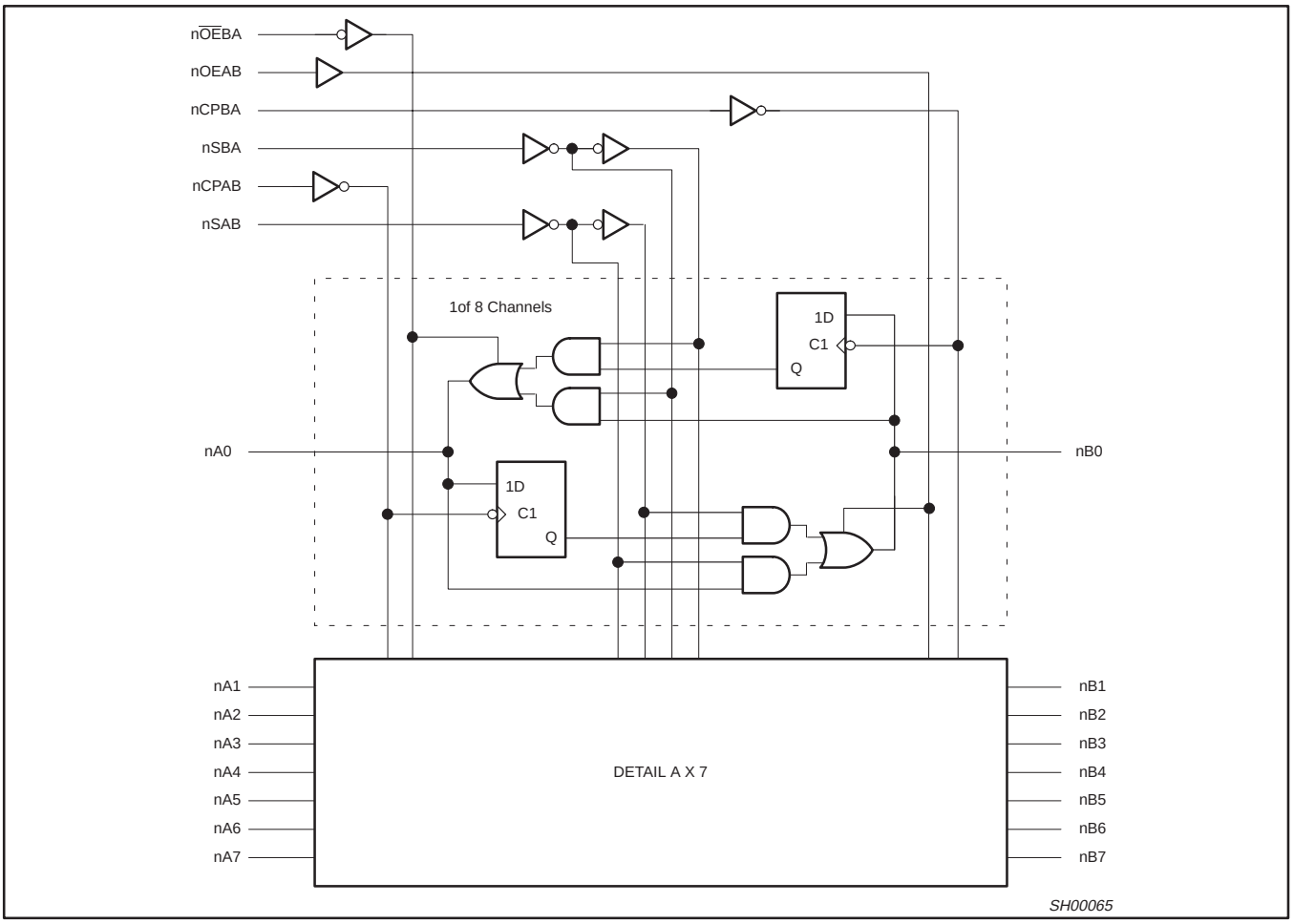
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55, 27, 30	1CPAB, 1CPBA, 2CPAB, 2CPBA	Clock input A to B / Clock input B to A
3, 54, 26, 31	1SAB, 1SBA, 2SAB, 2SBA	Select input A to B / Select input B to A
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs (A side)
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs (B side)
1, 56, 28, 29	1OEAB, 1$\overline{\text{OEBA}}$, 2OEAB, 2$\overline{\text{OEBA}}$	Output enable inputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



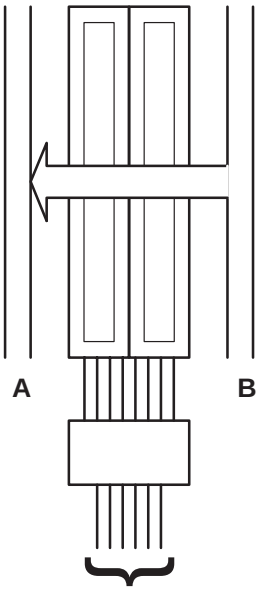
FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
nOEAB	nOEBA	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx	
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B data
X H	H H	↑ ↑	H or L ↑	X **	X X	Input	Unspecified output*	Store A, Hold B Store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X **	Unspecified output*	Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Store A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus Stored B data to A bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the nOEBA and nOEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
** If both Select controls (nSAB and nSBA) are Low, then clocks can occur simultaneously. If either Select control is High, the clocks must be staggered in order to load both registers.

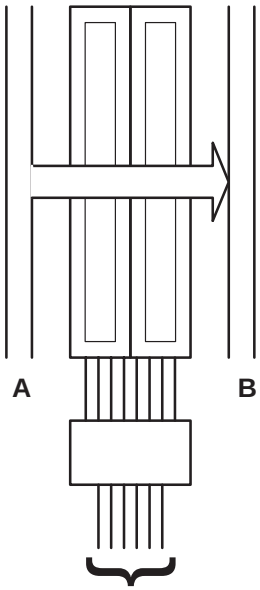
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74ABT16652.The select pins determine whether data is stored or transferred through the device in real time. The output enable pins determine the direction of the data flow.

REAL TIME BUS TRANSFER BUS B TO BUS A



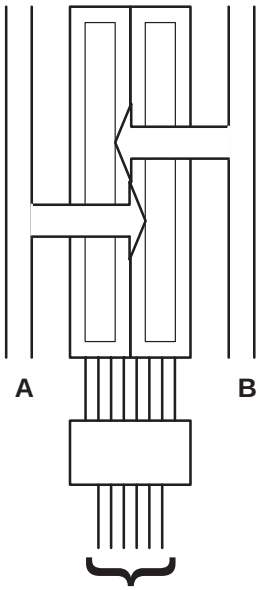
nOEAB	nOEBA	nCPAB	nCPBA	nSAB	nSBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER BUS A TO BUS B



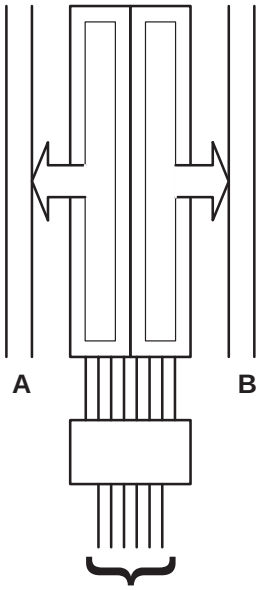
nOEAB	nOEBA	nCPAB	nCPBA	nSAB	nSBA
H	H	X	X	L	X

STORAGE FROM A, B, OR A AND B



nOEAB	nOEBA	nCPAB	nCPBA	nSAB	nSBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

TRANSFER STORED DATA TO A OR B



nOEAB	nOEBA	nCPAB	nCPBA	nSAB	nSBA
H	L	H | L	H | L	H	H

SH00066

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or HIGH state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in LOW state	128	mA
		output in HIGH state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA			–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}		3.0	4.0		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}		2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}			0.35	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5V; I_{OL} = 1mA; V_I = GND or V_{CC}			0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or V_{CC}	Control pins		±0.01	±1.0		±1.0	µA
I_{HOLD}	Bus Hold current A or B Ports[5] 74ABTH16652	V_{CC} = 4.5V; V_I = 0.8V		35			35		µA
		V_{CC} = 4.5V; V_I = 2.0V		–75			–75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±800					
I_{OFF}	Power-off leakage current	V_{CC} = 0V; V_O = 4.5V; V_I = 0V or 5.5V			±1.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.0V; V_I = GND or V_{CC}			±1.0	±50		±50	µA
I_{IH} + I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 5.5V; V_I = V_{IL} or V_{IH}			1.0	10		10	µA
I_{IL} + I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.0V; V_I = V_{IL} or V_{IH}			–1.0	–10		–10	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{cc}			5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		–50	–80	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.5	2		2	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			8	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}			0.5	2		2	mA
ΔI_{CC}	Additional supply current per input pin[2] 74ABT16652	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND			5.0	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2] 74ABTH16652	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND			200	500		500	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0 and 2.1V. When the part enables with V_{CC} between 2.1V and 4.5V, the outputs will correctly function with respect to all input logic states.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	125			125		MHz
t_{PLH} t_{PHL}	Propagation delay nCPAB to nBx or nCPBA to nAx	1	1.5 1.5	3.3 2.8	4.0 4.1	1.5 1.5	4.9 4.7	ns
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	2	1.0 1.0	2.3 1.8	3.2 4.1	1.0 1.0	3.9 4.6	ns
t_{PLH} t_{PHL}	Propagation delay nSAB to nBx or nSBA to nAx	3	1.0 1.0	3.4 2.6	4.3 4.3	1.0 1.0	5.0 5.0	ns
t_{PZH} t_{PZL}	Output enable time $n\overline{OEBA}$ to nAx	5 6	1.0 1.5	2.5 2.2	4.1 4.4	1.0 1.5	5.0 5.3	ns
t_{PHZ} t_{PLZ}	Output disable time $n\overline{OEBA}$ to nAx	5 6	1.5 1.5	3.6 2.7	4.4 3.6	1.5 1.5	4.9 4.0	ns
t_{PZH} t_{PZL}	Output enable time nOEAB to nBx	5 6	1.0 1.5	2.9 3.0	3.6 3.9	1.0 1.5	4.2 4.6	ns
t_{PHZ} t_{PLZ}	Output disable time nOEAB to nBx	5 6	2.0 1.5	3.1 2.3	5.5 4.5	2.0 1.5	5.9 5.2	ns

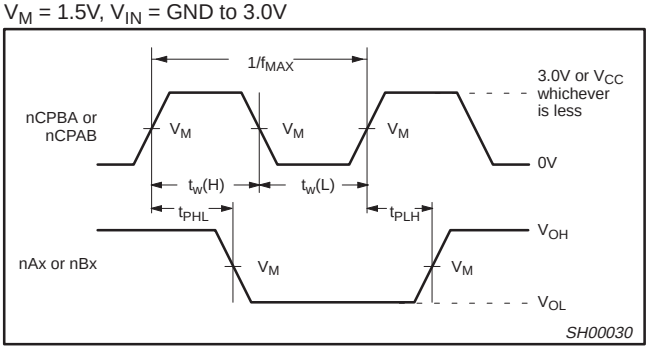
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

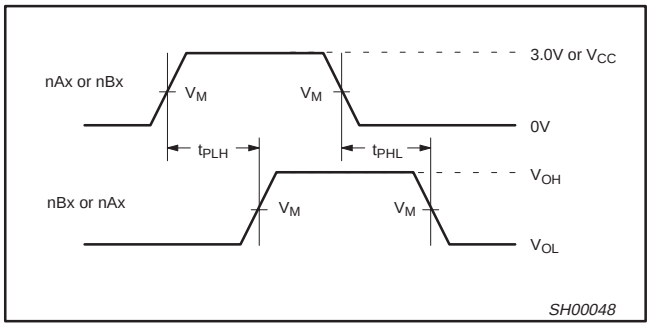
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Setup time nAx to nCPBA, nBx to nCPAB	4	3.0 3.0	1.2 0.8	3.0 3.0	ns
$t_h(H)$ $t_h(L)$	Hold time nAx to nCPBA, nBx to nCPAB	4	1.0 1.0	–0.7 –1.1	1.0 1.0	ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low nCPAB or nCPBA	1	4.3 4.3	1.0 1.0	4.3 4.3	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V



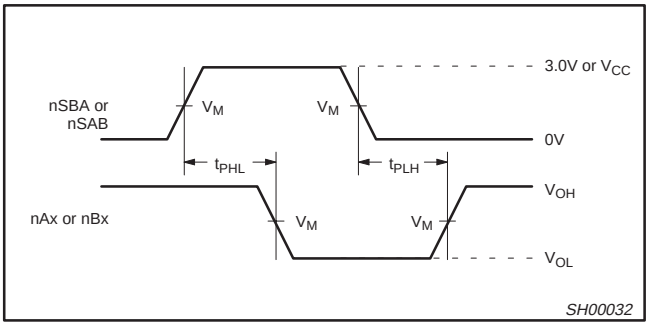
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



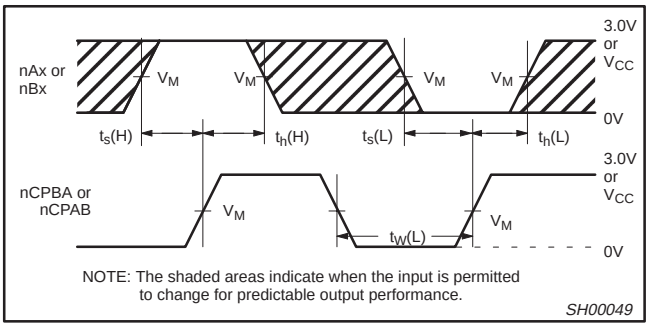
Waveform 2. Propagation Delay, nAx to nBx or nBx to nAx

AC WAVEFORMS (Continued)

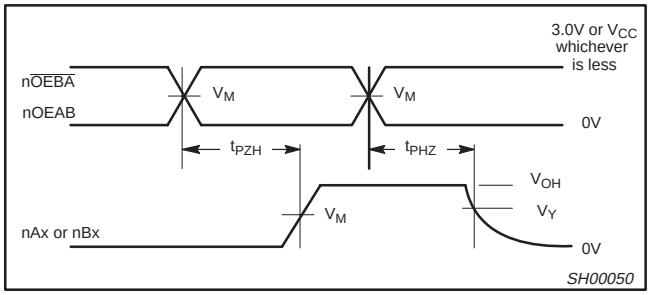
V_M = 1.5V, V_{IN} = GND to 3.0V



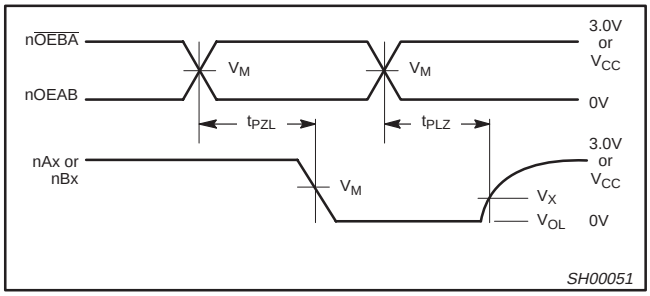
Waveform 3. Propagation Delay, SBA to nAx or SAB to nBx



Waveform 4. Data Setup and Hold Times

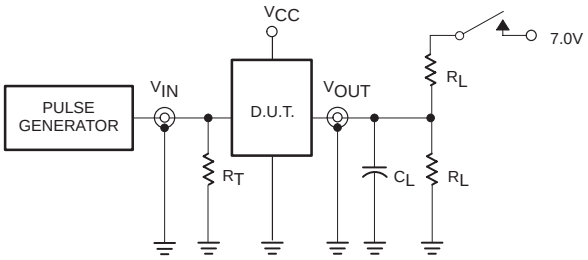


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

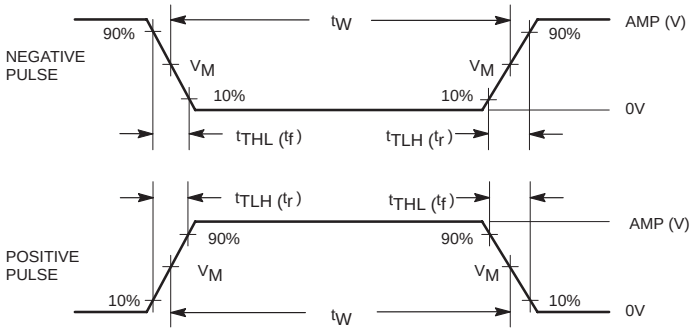
TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open



V_M = 1.5V
Input Pulse Definition

DEFINITIONS:

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT16	3.0V	1MHz	500ns	2.5ns	2.5ns

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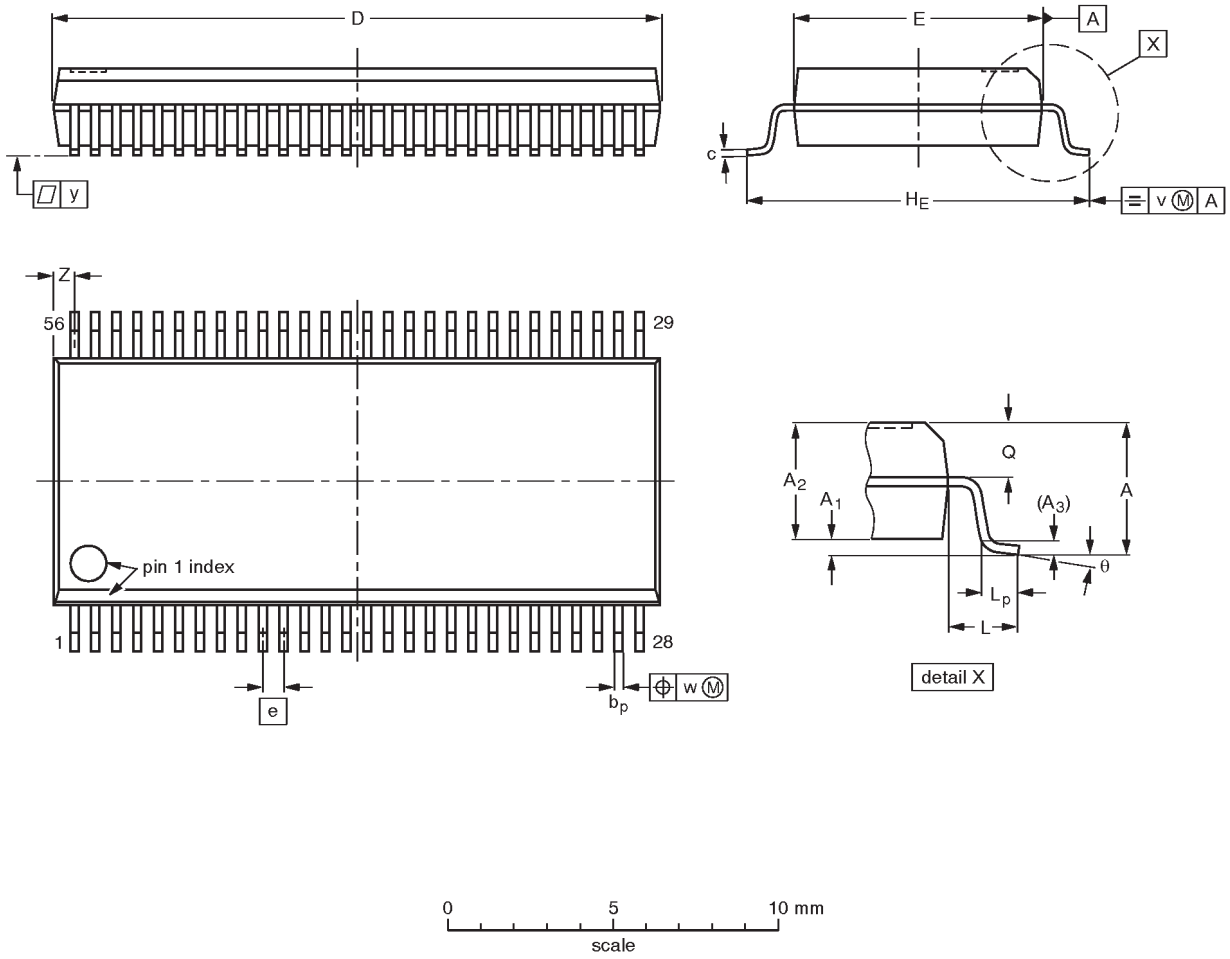
SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm **SOT371-1**



DIMENSIONS (mm are the original dimensions)

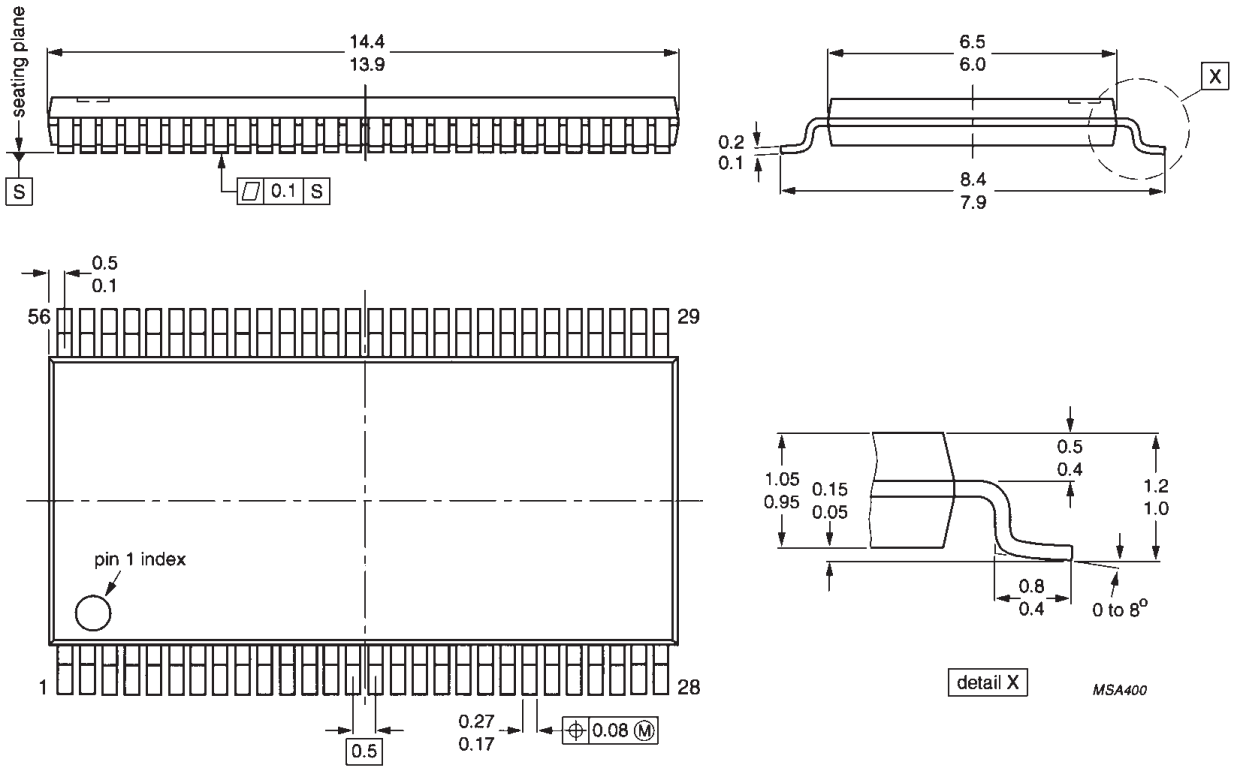
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				~~93-11-02~~ 95-02-04

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm **SOT364-1**



Dimensions in mm.

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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