

**FAIRCHILD**  
SEMICONDUCTOR®

May 1992  
Revised March 2005

74ABT244 Octal Buffer/Line Driver with 3-STATE Outputs

## 74ABT244

### Octal Buffer/Line Driver with 3-STATE Outputs

#### General Description

The ABT244 is an octal buffer and line driver with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver.

#### Features

- Non-inverting buffers
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Disable time less than enable time to avoid bus contention

#### Ordering Code:

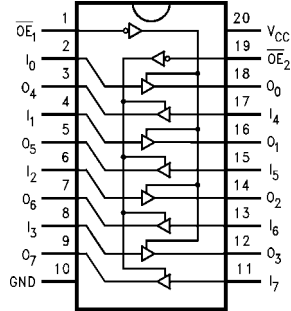
| Order Number              | Package Number | Package Description   |
|---------------------------|----------------|---|
| 74ABT244CSC               | M20B           | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide          |
| 74ABT244CSJ               | M20D           | Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide               |
| 74ABT244CMSA              | MSA20          | 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide               |
| 74ABT244CMSAX_NL (Note 1) | MSA20          | Pb-Free 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide       |
| 74ABT244CMTC              | MTC20          | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide         |
| 74ABT244CMTCX_NL (Note 1) | MTC20          | Pb-Free 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74ABT244CPC               | N20A           | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide              |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.  
Pb-Free package per JEDEC J-STD-020B.

**Note 1:** "\_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.



**Connection Diagram**



**Pin Descriptions**

| Pin Names                          | Description                         |
|------------------------------------|-------------------------------------|
| $\overline{OE}_1, \overline{OE}_2$ | Output Enable Input<br>(Active LOW) |
| $I_0-I_7$                          | Inputs                              |
| $O_0-O_7$                          | Outputs                             |

**Truth Table**

| $\overline{OE}_1$ | $I_{0-3}$ | $O_{0-3}$ | $\overline{OE}_2$ | $I_{4-7}$ | $O_{4-7}$ |
|-------------------|-----------|-----------|-------------------|-----------|-----------|
| H                 | X         | Z         | H                 | X         | Z         |
| L                 | H         | H         | L                 | H         | H         |
| L                 | L         | L         | L                 | L         | L         |

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

**Absolute Maximum Ratings**(Note 2)

|  |                                      |
|--|--------------------------------------|
| Storage Temperature  | -65°C to +150°C                      |
| Ambient Temperature under Bias   | -55°C to +125°C                      |
| Junction Temperature under Bias  | -55°C to +150°C                      |
| V <sub>CC</sub> Pin Potential to Ground Pin                            | -0.5V to +7.0V                       |
| Input Voltage (Note 3)   | -0.5V to +7.0V                       |
| Input Current (Note 3)   | -30 mA to +5.0 mA                    |
| Voltage Applied to Any Output<br>in the Disabled or<br>Power-Off State | -0.5V to 5.5V                        |
| in the HIGH State  | -0.5V to V <sub>CC</sub>             |
| Current Applied to Output<br>in LOW State (Max)                        | twice the rated I <sub>OL</sub> (mA) |
| DC Latchup Source Current  | -500 mA                              |
| Over Voltage Latchup (I/O)   | 10V                                  |

**Recommended Operating Conditions**

|   |                |
|---|----------------|
| Free Air Ambient Temperature                    | -40°C to +85°C |
| Supply Voltage                                  | +4.5V to +5.5V |
| Minimum Input Edge Rate ( $\Delta V/\Delta t$ ) |                |
| Data Input                                      | 50 mV/ns       |
| Enable Input                                    | 20 mV/ns       |

**Note 2:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 3:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

| Symbol           | Parameter                           | Min             | Typ             | Max  | Units      | V <sub>CC</sub>                         | Conditions   |  |
|------------------|-------------------------------------|-----------------|-----------------|------|------------|---|--|--|
| V <sub>IH</sub>  | Input HIGH Voltage                  | 2.0             |                 |      | V          |   | Recognized HIGH Signal   |  |
| V <sub>IL</sub>  | Input LOW Voltage                   |                 |                 | 0.8  | V          |   | Recognized LOW Signal  |  |
| V <sub>CD</sub>  | Input Clamp Diode Voltage           |                 |                 | -1.2 | V          | Min                                     | I <sub>IN</sub> = -18 mA   |  |
| V <sub>OH</sub>  | Output HIGH Voltage                 | 2.5             |                 |      | V          | Min                                     | I <sub>OH</sub> = -3 mA  |  |
|                  |                                     | 2.0             |                 |      | V          | Min                                     | I <sub>OH</sub> = -32 mA   |  |
| V <sub>OL</sub>  | Output LOW Voltage                  |                 |                 | 0.55 |            |   | I <sub>OL</sub> = 64 mA  |  |
| I <sub>IH</sub>  | Input HIGH Current                  |                 |                 | 1    | μA         | Max                                     | V <sub>IN</sub> = 2.7V (Note 5)  |  |
|                  |                                     |                 |                 | 1    | μA         | Max                                     | V <sub>IN</sub> = V <sub>CC</sub>  |  |
| I <sub>BV1</sub> | Input HIGH Current Breakdown Test   |                 |                 | 7    | μA         | Max                                     | V <sub>IN</sub> = 7.0V   |  |
| I <sub>IL</sub>  | Input LOW Current                   |                 |                 | -1   | μA         | Max                                     | V <sub>IN</sub> = 0.5V (Note 5)  |  |
|                  |                                     |                 |                 | -1   | μA         | Max                                     | V <sub>IN</sub> = 0.0V   |  |
| V <sub>ID</sub>  | Input Leakage Test                  | 4.75            |                 |      | V          | 0.0                                     | I <sub>ID</sub> = 1.9 μA<br>All Other Pins Grounded                                    |  |
| I <sub>OZH</sub> | Output Leakage Current              |                 |                 | 10   | μA         | 0 - 5.5V                                | V <sub>OUT</sub> = 2.7V; $\overline{OE}_n = 2.0V$                                      |  |
| I <sub>OZL</sub> | Output Leakage Current              |                 |                 | -10  | μA         | 0 - 5.5V                                | V <sub>OUT</sub> = 0.5V; $\overline{OE}_n = 2.0V$                                      |  |
| I <sub>OS</sub>  | Output Short-Circuit Current        | -100            |                 | -275 | mA         | Max                                     | V <sub>OUT</sub> = 0.0V  |  |
| I <sub>CEx</sub> | Output High Leakage Current         |                 |                 | 50   | μA         | Max                                     | V <sub>OUT</sub> = V <sub>CC</sub>   |  |
| I <sub>ZZ</sub>  | Bus Drainage Test                   |                 |                 | 100  | μA         | 0.0                                     | V <sub>OUT</sub> = 5.5V; All Others GND  |  |
| I <sub>CCH</sub> | Power Supply Current                |                 |                 | 50   | μA         | Max                                     | All Outputs HIGH   |  |
| I <sub>CCL</sub> | Power Supply Current                |                 |                 | 30   | mA         | Max                                     | All Outputs LOW  |  |
| I <sub>CCZ</sub> | Power Supply Current                |                 |                 | 50   | μA         | Max                                     | $\overline{OE}_n = V_{CC}$ ,<br>All Others at V <sub>CC</sub> or Ground                |  |
| I <sub>CCT</sub> | Additional I <sub>CC</sub> /Input   | Outputs Enabled |                 | 2.5  | mA         |   | V <sub>I</sub> = V <sub>CC</sub> - 2.1V  |  |
|                  |                                     |                 | Outputs 3-STATE |      | 2.5        | mA                                      | Max  | Enable Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V |
|                  |                                     |                 |                 |      | 50         | μA                                      |  | Data Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V   |
|                  |                                     |                 |                 |      |            | All Others at V <sub>CC</sub> or Ground |  |  |
| I <sub>CCD</sub> | Dynamic I <sub>CC</sub><br>(Note 5) | No Load         |                 |      | mA/<br>MHz | Max                                     | Outputs OPEN<br>$\overline{OE}_n = GND$ , (Note 4)<br>One Bit Toggling, 50% Duty Cycle |  |

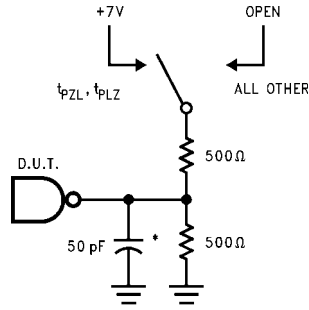
**Note 4:** For 8 bits toggling, I<sub>CCD</sub> < 0.8 mA/MHz.

**Note 5:** Guaranteed, but not tested.

| DC Electrical Characteristics  |  |   |      |     |  |                 |   |      |       |
|--|--|---|------|-----|--|-----------------|---|------|-------|
| (SOIC package)   |  |   |      |     |  |                 |   |      |       |
| Symbol   | Parameter                                    | Min   | Typ  | Max | Units  | V <sub>CC</sub> | Conditions<br>C <sub>L</sub> = 50 pF,<br>R <sub>L</sub> = 500Ω  |      |       |
| V <sub>OLP</sub>   | Quiet Output Maximum Dynamic V <sub>OL</sub> |   | 0.5  | 0.8 | V  | 5.0             | T <sub>A</sub> = 25°C (Note 6)  |      |       |
| V <sub>OLV</sub>   | Quiet Output Minimum Dynamic V <sub>OL</sub> | -1.3  | -0.8 |     | V  | 5.0             | T <sub>A</sub> = 25°C (Note 6)  |      |       |
| V <sub>OHV</sub>   | Minimum HIGH Level Dynamic Output Voltage    | 2.7   | 3.1  |     | V  | 5.0             | T <sub>A</sub> = 25°C (Note 8)  |      |       |
| V <sub>IHD</sub>   | Minimum HIGH Level Dynamic Input Voltage     | 2.0   | 1.5  |     | V  | 5.0             | T <sub>A</sub> = 25°C (Note 7)  |      |       |
| V <sub>ILD</sub>   | Maximum LOW Level Dynamic Input Voltage      |   | 1.1  | 0.8 | V  | 5.0             | T <sub>A</sub> = 25°C (Note 7)  |      |       |
| <p><b>Note 6:</b> Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.</p> <p><b>Note 7:</b> Max number of data inputs (n) switching. n – 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>). Guaranteed, but not tested.</p> <p><b>Note 8:</b> Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.</p>  |  |   |      |     |  |                 |   |      |       |
| AC Electrical Characteristics  |  |   |      |     |  |                 |   |      |       |
| (SOIC and SSOP package)  |  |   |      |     |  |                 |   |      |       |
| Symbol   | Parameter                                    | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = +5V<br>C <sub>L</sub> = 50 pF   |      |     | T <sub>A</sub> = -55°C to +125°C<br>V <sub>CC</sub> = 4.5V–5.5V<br>C <sub>L</sub> = 50 pF                                    |                 | T <sub>A</sub> = -40°C to +85°C<br>V <sub>CC</sub> = 4.5V–5.5V<br>C <sub>L</sub> = 50 pF                                      |      | Units |
|  |  | Min   | Typ  | Max | Min  | Max             | Min   | Max  |       |
| t <sub>PLH</sub>   | Propagation Delay                            | 1.0   | 2.5  | 3.6 | 1.0  | 5.3             | 1.0   | 3.6  | ns    |
| t <sub>PHL</sub>   | Data to Outputs                              | 1.0   | 2.3  | 3.6 | 1.0  | 5.0             | 1.0   | 3.6  |       |
| t <sub>PZH</sub>   | Output Enable                                | 1.5   | 3.5  | 6.0 | 0.8  | 6.5             | 1.5   | 6.0  | ns    |
| t <sub>PZL</sub>   | Time   | 1.5   | 3.6  | 6.0 | 1.2  | 7.9             | 1.5   | 6.0  |       |
| t <sub>PHZ</sub>   | Output Disable                               | 1.7   | 3.5  | 5.6 | 1.2  | 7.6             | 1.7   | 5.6  | ns    |
| t <sub>PLZ</sub>   | Time   | 1.7   | 3.3  | 5.6 | 1.0  | 7.9             | 1.7   | 5.6  |       |
| Extended AC Electrical Characteristics   |  |   |      |     |  |                 |   |      |       |
| (SOIC package)   |  |   |      |     |  |                 |   |      |       |
| Symbol   | Parameter                                    | T <sub>A</sub> = -40°C to +85°C<br>V <sub>CC</sub> = 4.5V–5.5V<br>C <sub>L</sub> = 50 pF<br>8 Outputs Switching<br>(Note 9) |      |     | T <sub>A</sub> = -40°C to +85°C<br>V <sub>CC</sub> = 4.5V–5.5V<br>C <sub>L</sub> = 250 pF<br>1 Output Switching<br>(Note 10) |                 | T <sub>A</sub> = -40°C to +85°C<br>V <sub>CC</sub> = 4.5V–5.5V<br>C <sub>L</sub> = 250 pF<br>8 Outputs Switching<br>(Note 11) |      | Units |
|  |  | Min   | Typ  | Max | Min  | Max             | Min   | Max  |       |
| f <sub>TOGGLE</sub>  | Max Toggle Frequency                         | 100   |      |     |  |                 |   |      | MHz   |
| t <sub>PLH</sub>   | Propagation Delay                            | 1.5   |      | 5.0 | 1.5  | 6.0             | 2.5   | 8.5  | ns    |
| t <sub>PHL</sub>   | Data to Outputs                              | 1.5   |      | 5.0 | 1.5  | 6.0             | 2.5   | 8.5  |       |
| t <sub>PZH</sub>   | Output Enable Time                           | 1.5   |      | 6.5 | 2.5  | 7.5             | 2.5   | 10.0 | ns    |
| t <sub>PZL</sub>   | Time   | 1.5   |      | 6.5 | 2.5  | 7.5             | 2.5   | 12.0 |       |
| t <sub>PHZ</sub>   | Output Disable Time                          | 1.0   |      | 5.6 | (Note 12)  |                 | (Note 12)   |      | ns    |
| t <sub>PLZ</sub>   | Time   | 1.0   |      | 5.6 |  |                 |   |      |       |
| <p><b>Note 9:</b> This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).</p> <p><b>Note 10:</b> This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.</p> <p><b>Note 11:</b> This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.</p> <p><b>Note 12:</b> The 3-STATE delays are dominated by the RC network (500Ω, 250 pF) on the output and have been excluded from the datasheet.</p> |  |   |      |     |  |                 |   |      |       |

| <b>Skew</b>   |  |   |  |  |
|---|--|---|--|--|
| Symbol  | Parameter                                  | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$<br>$V_{CC} = 4.5\text{V} - 5.5\text{V}$<br>$C_L = 50\text{ pF}$<br>8 Outputs Switching<br>(Note 15) | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$<br>$V_{CC} = 4.5\text{V} - 5.5\text{V}$<br>$C_L = 250\text{ pF}$<br>8 Outputs Switching<br>(Note 16) | Units                                  |
|   |  | Max   | Max  |  |
| $t_{OSHL}$<br>(Note 13)   | Pin to Pin Skew<br>HL Transitions          | 0.8   | 1.8  | ns                                     |
| $t_{OSLH}$<br>(Note 13)   | Pin to Pin Skew<br>LH Transitions          | 0.8   | 1.8  | ns                                     |
| $t_{PS}$<br>(Note 17)   | Duty Cycle<br>LH-HL Skew                   | 1.0   | 2.5  | ns                                     |
| $t_{OST}$<br>(Note 13)  | Pin to Pin Skew<br>LH/HL Transitions       | 1.0   | 2.5  | ns                                     |
| $t_{PV}$<br>(Note 14)   | Device to Device Skew<br>LH/HL Transitions | 1.5   | 3.0  | ns                                     |
| <p><b>Note 13:</b> Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (<math>t_{OSHL}</math>), LOW-to-HIGH (<math>t_{OSLH}</math>), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW (<math>t_{OST}</math>). The specification is guaranteed but not tested.</p> <p><b>Note 14:</b> Propagation delay variation for a given set of conditions (i.e., temperature and <math>V_{CC}</math>) from device to device. This specification is guaranteed but not tested.</p> <p><b>Note 15:</b> This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.)</p> <p><b>Note 16:</b> These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.</p> <p><b>Note 17:</b> This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.</p> |  |   |  |  |
| <b>Capacitance</b>  |  |   |  |  |
| Symbol  | Parameter                                  | Typ   | Units  | Conditions<br>$T_A = 25^\circ\text{C}$ |
| $C_{IN}$  | Input Capacitance                          | 5.0   | pF   | $V_{CC} = 0\text{V}$                   |
| $C_{OUT}$ (Note 18)   | Output Capacitance                         | 9.0   | pF   | $V_{CC} = 5.0\text{V}$                 |
| <p><b>Note 18:</b> <math>C_{OUT}</math> is measured at frequency <math>f = 1\text{ MHz}</math>, per MIL-STD-883, Method 3012.</p>   |  |   |  |  |

### AC Loading



\*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

### AC Waveforms

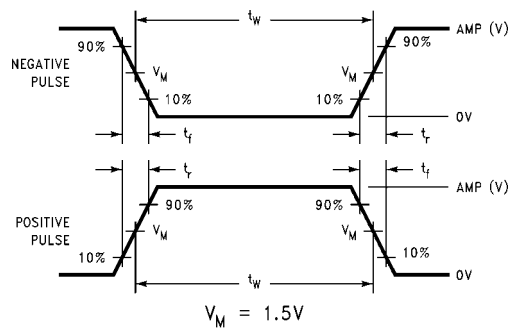


FIGURE 2. Test Input Signal Levels

| Amplitude | Rep. Rate | $t_w$  | $t_r$  | $t_f$  |
|-----------|-----------|--------|--------|--------|
| 3.0V      | 1 MHz     | 500 ns | 2.5 ns | 2.5 ns |

FIGURE 3. Test Input Signal Requirements

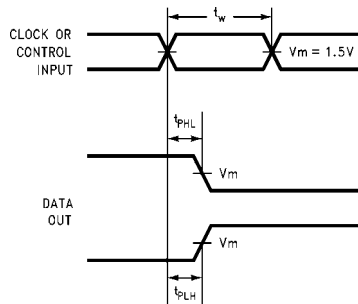


FIGURE 4. Propagation Delay, Pulse Width Waveforms

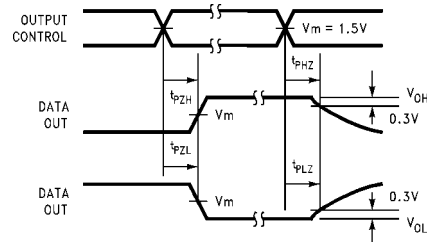


FIGURE 5. 3-STATE Output HIGH and LOW Enable and Disable Times

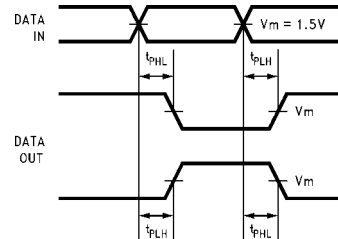


FIGURE 6. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

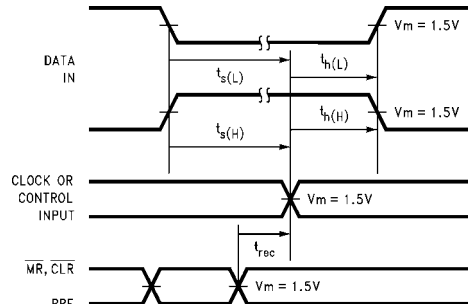
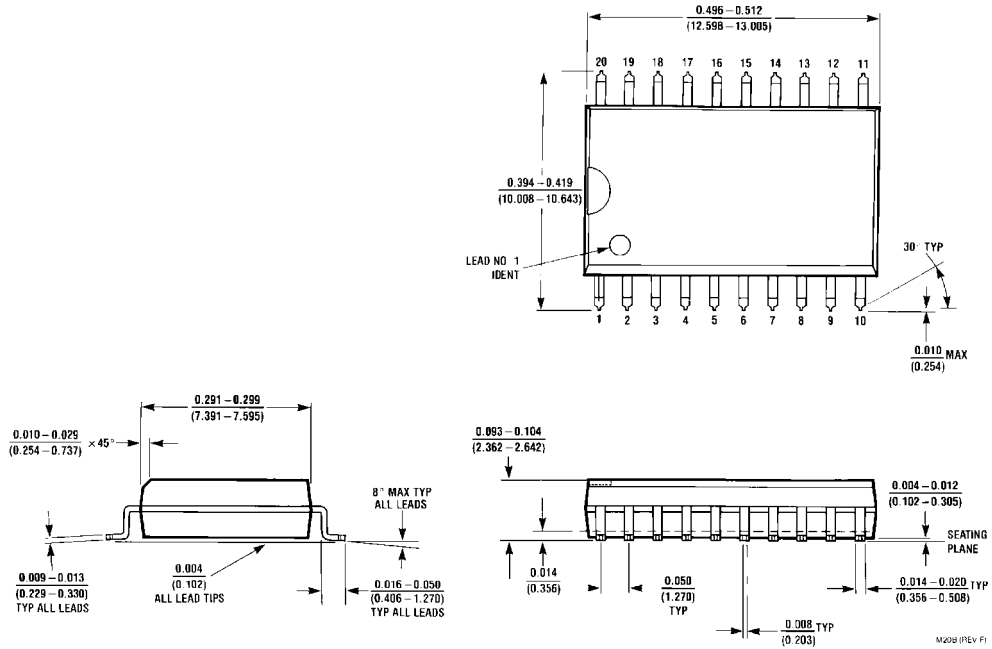


FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

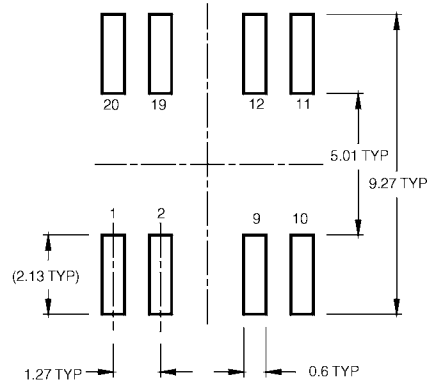
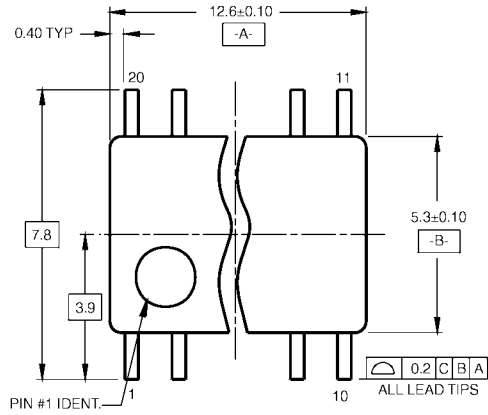
**Physical Dimensions** inches (millimeters) unless otherwise noted



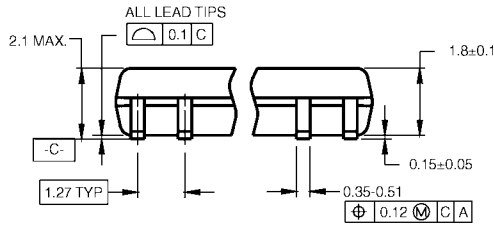
20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide  
Package Number M20B

M20B (REV F)

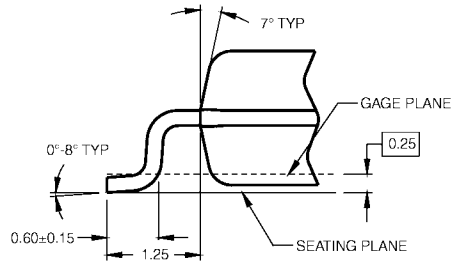
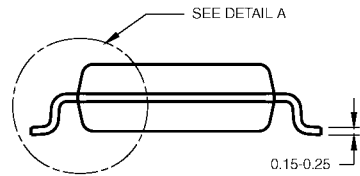
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

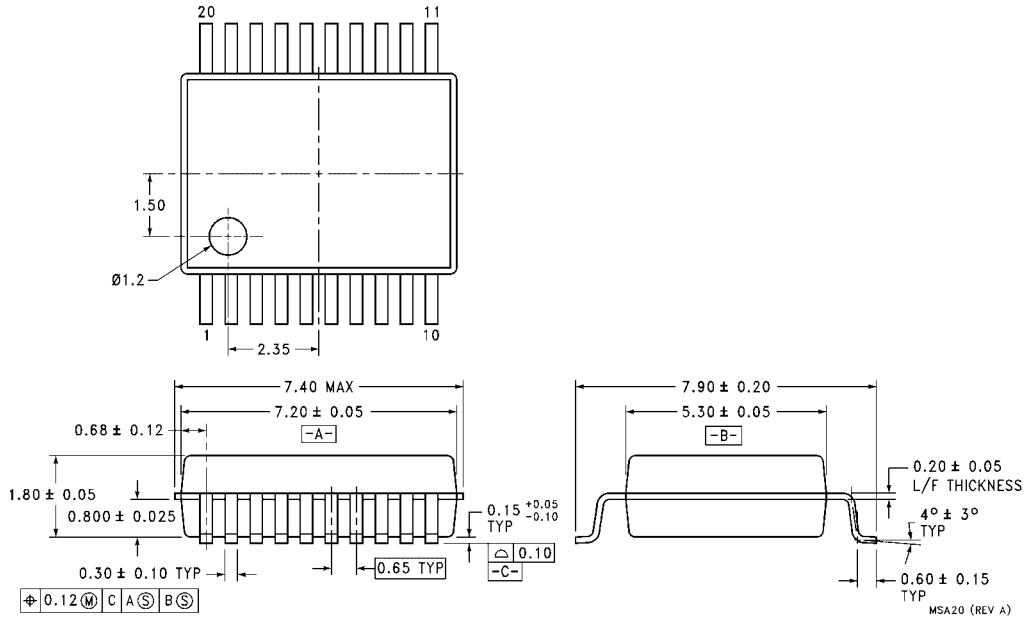
- NOTES:  
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.  
 B. DIMENSIONS ARE IN MILLIMETERS.  
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRRevB1

**Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
 Package Number M20D**

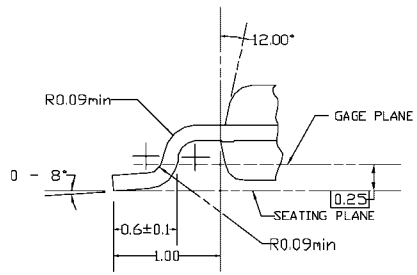
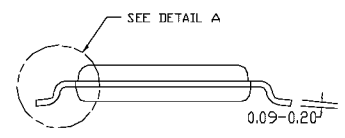
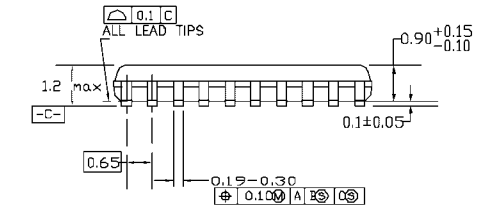
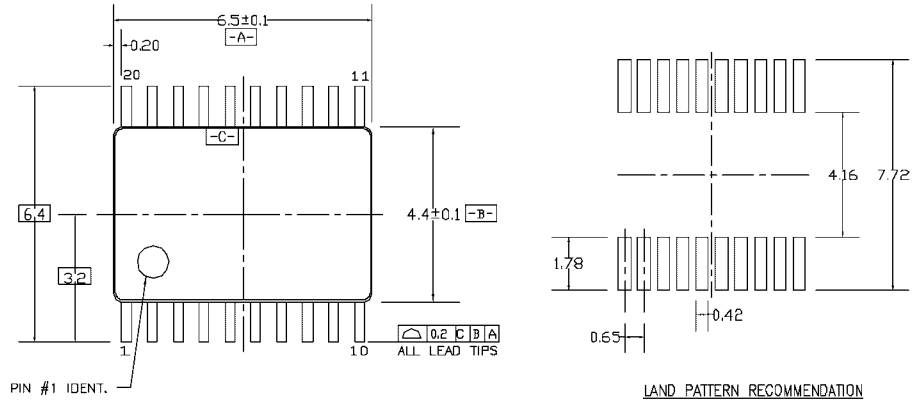


**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide  
Package Number MSA20**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



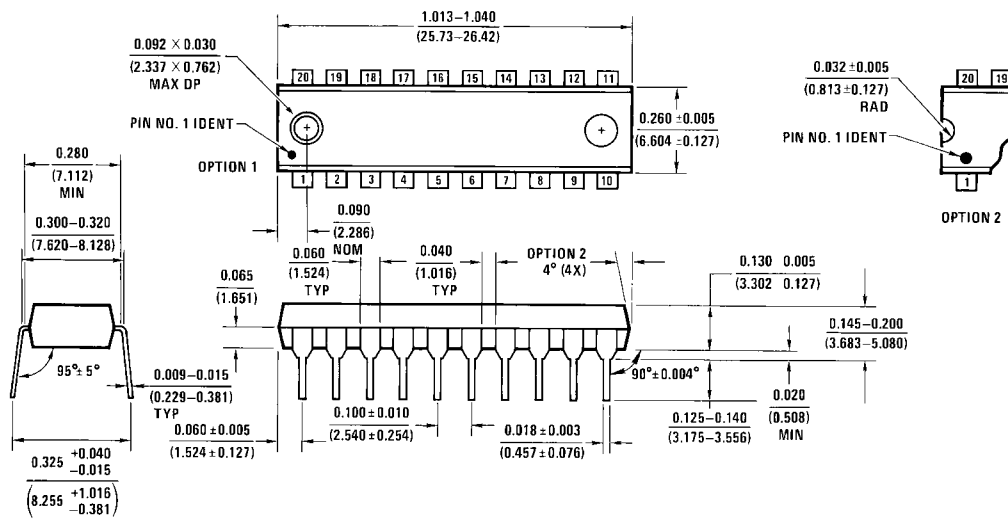
DIMENSIONS ARE IN MILLIMETERS

- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
  - D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REV D1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N20A**

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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