

April 1988 Revised July 1999

#### 74F113

## **Dual JK Negative Edge-Triggered Flip-Flop**

#### **General Description**

The 74F113 offers individual J, K, Set and Clock inputs. When the clock goes HIGH the inputs are enabled and data may be entered. The logic level of the J and K inputs may be changed when the clock pulse is HIGH and the flipflop will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is

transferred to the outputs on the falling edge of the clock pulse.

Asynchronous input:

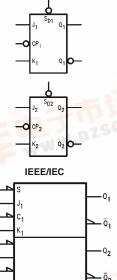
LOW input to  $\overline{S}_D$  sets Q to HIGH level Set is independent of clock

#### **Ordering Code:**

Order Number	Package Number	Package Description
74F113SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74F113SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F113PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

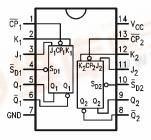
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### **Logic Symbols**



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#### **Connection Diagram**



## **Unit Loading/Fan Out**

Pin Names	Description	U.L.	Input I <sub>IH</sub> /I <sub>IL</sub>	
	Description	HIGH/LOW	Output I <sub>OH</sub> /I <sub>OL</sub>	
J <sub>1</sub> , J <sub>2</sub> , K <sub>1</sub> , K <sub>2</sub>	Data Inputs	1.0/1.0	20 μA/-0.6 mA	
$\overline{CP}_1$ , $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	1.0/4.0	20 μA/–2.4 mA	
$\overline{S}_{D1}$ , $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	1.0/5.0	20 μA/–3.0 mA	
$Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$	Outputs	50/33.3	−1 mA/20 mA	

#### **Truth Table**

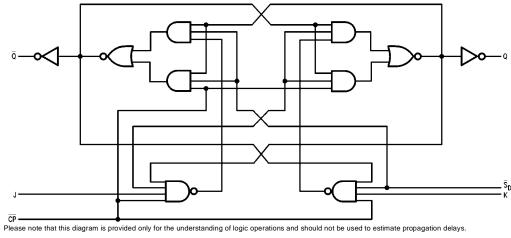
	Inpu	Out	puts		
S <sub>D</sub>	СР	J	Q	Q	
L	Х	Χ	Χ	Н	L
Н	~	h	h	$\overline{Q}_0$	$Q_0$
Н	$\sim$	I	h	L	Н
Н	~	h	1	Н	L
Н	$\sim$	I	1	$Q_0$	$\overline{Q}_0$

 $\begin{array}{l} \text{H (h) = HIGH \ Voltage \ Level} \\ \text{L (I) = LOW \ Voltage \ level} \\ \text{]} \sim = \text{HIGH-to-LOW \ Clock \ Transition} \\ \text{X = Immaterial} \\ \text{Q}_0 \ (\overline{\text{Q}}_0) = \text{Before \ HIGH-to-LOW \ Transition \ of \ Clock} \\ \end{array}$ 

Lower case letters indicate the state of the referenced input or output prior to the HIGH-to-LOW clock transition.

#### **Logic Diagram**

(One Half Shown)



### Absolute Maximum Ratings(Note 1)

Input Current (Note 2)
Voltage Applied to Output

in HIGH State (with  $V_{CC} = 0V$ )

Standard Output  $$-0.5\mbox{V}$ \ to \ \mbox{V}_{\mbox{CC}}$$ 

-30 mA to +5.0 mA

3-STATE Output -0.5V to +5.5V

Current Applied to Output

in LOW State (Max)  $\qquad \qquad \text{twice the rated I}_{\text{OL}} \, (\text{mA})$ 

# Recommended Operating Conditions

Free Air Ambient Temperature  $0^{\circ}\text{C to } +70^{\circ}\text{C}$  Supply Voltage +4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation

under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

#### **DC Electrical Characteristics**

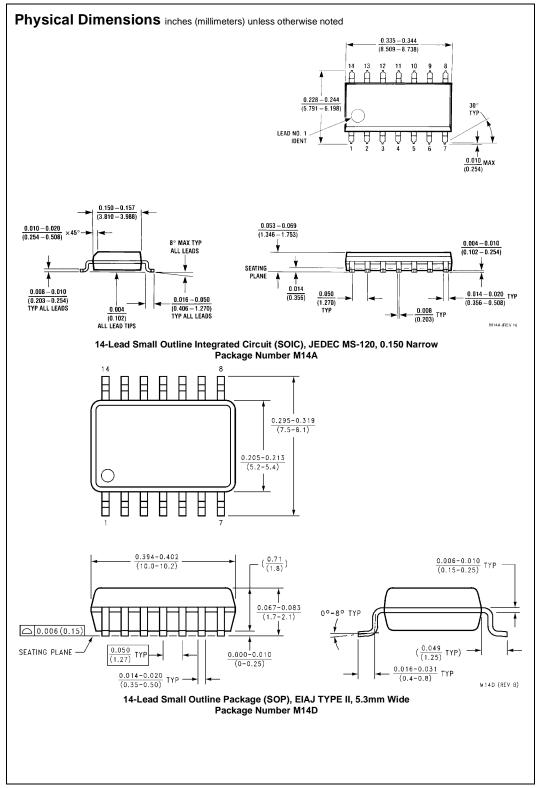
Symbol	Parameter		Min	Тур	Max	Units	v <sub>cc</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH 1	0% V <sub>CC</sub>	2.5			V	Min	I <sub>OH</sub> = -1 mA
	Voltage	5% V <sub>CC</sub>	2.7					$I_{OH} = -1 \text{ mA}$
V <sub>OL</sub>	Output LOW 1	0% V <sub>CC</sub>			0.5	V	Min	I <sub>OL</sub> = 20 mA
	Voltage							
I <sub>IH</sub>	Input HIGH				5.0	μА	Max	V <sub>IN</sub> = 2.7V
	Current				5.0	μΑ	IVIAX	v <sub>IN</sub> = 2.7 v
I <sub>BVI</sub>	Input HIGH Current				7.0	μА	Max	\/ -70\/
	Breakdown Test				7.0	μΑ	IVIAX	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH				50	μА	Max	$V_{OUT} = V_{CC}$
	Leakage Current				50	μΑ	IVIAX	
V <sub>ID</sub>	Input Leakage		4.75			V	0.0	$I_{ID} = 1.9 \mu\text{A}$
	Test		4.75					All Other Pins Grounded
I <sub>OD</sub>	Output Leakage				3.75	μА	0.0	V <sub>IOD</sub> = 150 mV
	Circuit Current				5.75	μΑ		All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current				-0.6			$V_{IN} = 0.5V (J_n, K_n)$
					-2.4	mA	Max	$V_{IN} = 0.5V (\overline{CP}_n)$
					-3.0			$V_{IN} = 0.5V (\overline{S}_{Dn})$
l <sub>ozh</sub>	Output Leakage Current				50	μΑ	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current				-50	μА	Max	V <sub>OUT</sub> = 0.5V
Ios	Output Short-Circuit Current		-60		-150	mA	Max	V <sub>OUT</sub> = 0V
Icc	Power Supply Current			12	19	mA	Max	

## **AC Electrical Characteristics**

Symbol	Parameter	$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$			$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		Units	
		Min	Тур	Max	Min	Max	1	
f <sub>MAX</sub>	Maximum Clock Frequency	85	105		80		MHz	
t <sub>PLH</sub>	Propagation Delay	2.0	4.0	6.0	2.0	7.0		
t <sub>PHL</sub>	$\overline{CP}_n$ to $Q_n$ or $\overline{Q}_n$	2.0	4.0	6.0	2.0	7.0	ns	
t <sub>PLH</sub>	Propagation Delay	2.0	4.5	6.5	2.0	7.5		
t <sub>PHL</sub>	$\overline{S}_{Dn}$ to $Q_n$ or $\overline{Q}_n$	2.0	4.5	6.5	2.0	7.5	ns	

## **AC Operating Requirements**

		$T_A = +25$ °C $V_{CC} = +5.0$ V		$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$		Units
Symbol	Parameter					
		Min	Max	Min	Max	
t <sub>S</sub> (H)	Setup Time, HIGH or LOW	4.0		5.0		
t <sub>S</sub> (L)	$J_n$ or $K_n$ to $\overline{CP}_n$	3.0		3.5		ns
t <sub>H</sub> (H)	Hold Time, HIGH or LOW	0		0		113
t <sub>H</sub> (L)	$J_n$ or $K_n$ to $\overline{CP}_n$	0		0		
t <sub>W</sub> (H)	CP <sub>n</sub> Pulse Width	4.5		5.0		ns
t <sub>W</sub> (L)	HIGH or LOW	4.5		5.0		115
t <sub>W</sub> (L)	S <sub>Dn</sub> Pulse Width, LOW	4.5		5.0		ns
t <sub>REC</sub>	S <sub>Dn</sub> to CP <sub>n</sub> Recovery Time	4.0		5.0		ns



#### Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770 (18.80 - 19.56)0.090 (2.286) 14 13 12 14 13 12 11 10 9 8 0.250 ± 0.010 $(6.350 \pm 0.254)$ PIN NO. 1 IDENT PIN NO. 1 IDENT $\frac{0.092}{(2.337)}$ DIA $\frac{0.030}{(0.762)}$ MAX DEPTH OPTION 1 OPTION 02 $0.135 \pm 0.005$ $\frac{0.300 - 0.320}{(7.620 - 8.128)}$ 0.065 0.145 - 0.2000.060 4° TYP TYP (1.651) (3.683 - 5.080)OPTIONAL 0.008 95°±5 0.020 (0.508) 0.125 - 0.150 MIN $0.075 \pm 0.015$ $\overline{(3.175 - 3.810)}$ 0.280 $(1.905 \pm 0.381)$ -(7.112)-MIN 0.014 - 0.023 0.100±0.010 TYP (0.356 - 0.584) $(2.540 \pm 0.254)$ 0.050±0.010 TYP

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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