



June 2000
Revised February 2005

74LCX10

Low Voltage Triple 3-Input NAND Gate with 5V Tolerant Inputs

General Description

The LCX10 contains three 3-input NAND gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

The 74LCX10 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

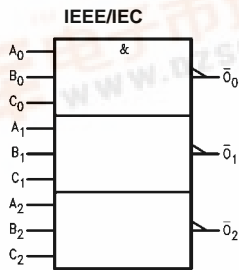
- 5V tolerant inputs
- 2.3V–3.6V V_{CC} specifications provided
- 4.9 ns t_{PD} max ($V_{CC} = 3.3V$), 10 μA I_{CC} max
- Power down high impedance inputs and outputs
- ± 24 mA output drive ($V_{CC} = 3.0V$)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V

Ordering Code:

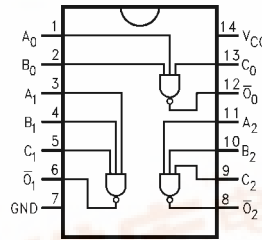
Order Number	Package Number	Package Description
74LCX10M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LCX10SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX10MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A_n, B_n, C_n	Inputs
\bar{O}_n	Outputs

Truth Table

$\bar{O}_n = A_n B_n C_n$

A_n	B_n	C_n	\bar{O}_n
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

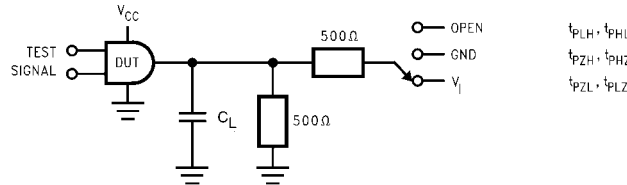
74LCX10 Low Voltage Triple 3-Input NAND Gate with 5V Tolerant Inputs



Absolute Maximum Ratings (Note 1)						
Symbol	Parameter	Value	Conditions	Units		
V_{CC}	Supply Voltage	-0.5 to +7.0		V		
V_I	DC Input Voltage	-0.5 to +7.0		V		
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	Output in HIGH or LOW State (Note 2)	V		
I_{IK}	DC Input Diode Current	-50	$V_I < GND$	mA		
I_{OK}	DC Output Diode Current	-50	$V_O < GND$	mA		
		+50	$V_O > V_{CC}$	mA		
I_O	DC Output Source/Sink Current	± 50		mA		
I_{CC}	DC Supply Current per Supply Pin	± 100		mA		
I_{GND}	DC Ground Current per Ground Pin	± 100		mA		
T_{STG}	Storage Temperature	-65 to +150		°C		
Recommended Operating Conditions (Note 3)						
Symbol	Parameter	Min	Max	Units		
V_{CC}	Supply Voltage	Operating	2.0	3.6	V	
		Data Retention	1.5	3.6		
V_I	Input Voltage	0	5.5	V		
V_O	Output Voltage	0	V_{CC}	V		
I_{OH}/I_{OL}	Output Current	$V_{CC} = 3.0V - 3.6V$		± 24	mA	
		$V_{CC} = 2.7V - 3.0V$		± 12		
		$V_{CC} = 2.3V - 2.7V$		± 8		
T_A	Free-Air Operating Temperature	-40	85	°C		
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V - 2.0V$, $V_{CC} = 3.0V$	0	10	ns/V		
<p>Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.</p> <p>Note 2: I_O Absolute Maximum Rating must be observed.</p> <p>Note 3: Unused inputs must be held HIGH or LOW. They may not float.</p>						
DC Electrical Characteristics						
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40^\circ C$ to $+85^\circ C$		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.3 - 2.7	1.7		V
			2.7 - 3.6	2.0		
V_{IL}	LOW Level Input Voltage		2.3 - 2.7		0.7	V
			2.7 - 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.3 - 3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -8 mA$	2.3	1.8		
		$I_{OH} = -12 mA$	2.7	2.2		
		$I_{OH} = -18 mA$	3.0	2.4		
		$I_{OH} = -24 mA$	3.0	2.2		
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.3 - 3.6		0.2	V
		$I_{OL} = 8 mA$	2.3		0.6	
		$I_{OL} = 12 mA$	2.7		0.4	
		$I_{OL} = 16 mA$	3.0		0.4	
		$I_{OL} = 24 mA$	3.0		0.55	
I_I	Input Leakage Current	$0 \leq V_I \leq 5.5V$	2.3 - 3.6		± 5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or $V_O = 5.5V$	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 - 3.6		10	μA
		$3.6V \leq V_I \leq 5.5V$	2.3 - 3.6		± 10	
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.3 - 3.6		500	μA

AC Electrical Characteristics								
Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}, R_L = 500\Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2V$		
		$C_L = 50\text{pF}$		$C_L = 50\text{pF}$		$C_L = 30\text{pF}$		
		Min	Max	Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.5	4.9	1.5	5.8	1.5	5.9	ns
t_{PLH}		1.5	4.9	1.5	5.8	1.5	5.9	
t_{OSHL}	Output to Output Skew (Note 4)		1.0					ns
t_{OSLH}			1.0					
<p>Note 4: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).</p>								
Dynamic Switching Characteristics								
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25^\circ\text{C}$	Unit			
				Typical				
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50\text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$	3.3	0.8	V			
		$C_L = 30\text{ pF}, V_{IH} = 2.5V, V_{IL} = 0V$	2.5	0.6				
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50\text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$	3.3	-0.8	V			
		$C_L = 30\text{ pF}, V_{IH} = 2.5V, V_{IL} = 0V$	2.5	-0.6				
Capacitance								
Symbol	Parameter	Conditions	Typical	Units				
C_{IN}	Input Capacitance	$V_{CC} = \text{Open}, V_I = 0V \text{ or } V_{CC}$	7	pF				
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}$	8	pF				
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}, f = 10\text{ MHz}$	25	pF				

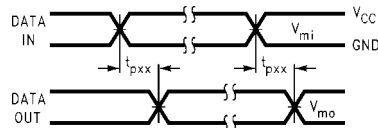
AC LOADING and WAVEFORMS Generic for LCX Family



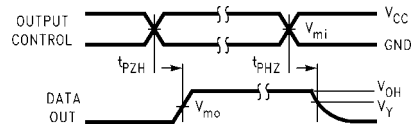
t_{PLH}, t_{PHL}
t_{PZH}, t_{PHZ}
t_{PZL}, t_{PLZ}

FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

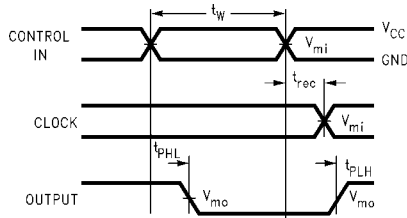
Test	Switch
t _{PLH} , t _{PHL}	Open
t _{PZL} , t _{PLZ}	6V at V _{CC} = 3.3 ± 0.3V V _{CC} × 2 at V _{CC} = 2.5 ± 0.2V
t _{PZH} , t _{PHZ}	GND



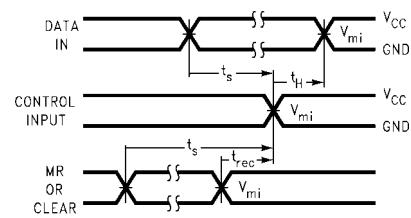
Waveform for Inverting and Non-Inverting Functions



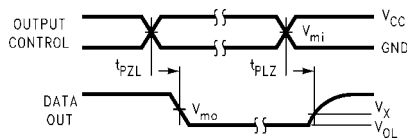
3-STATE Output High Enable and Disable Times for Logic



Propagation Delay, Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

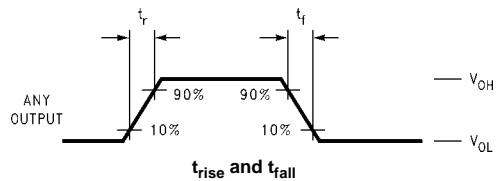
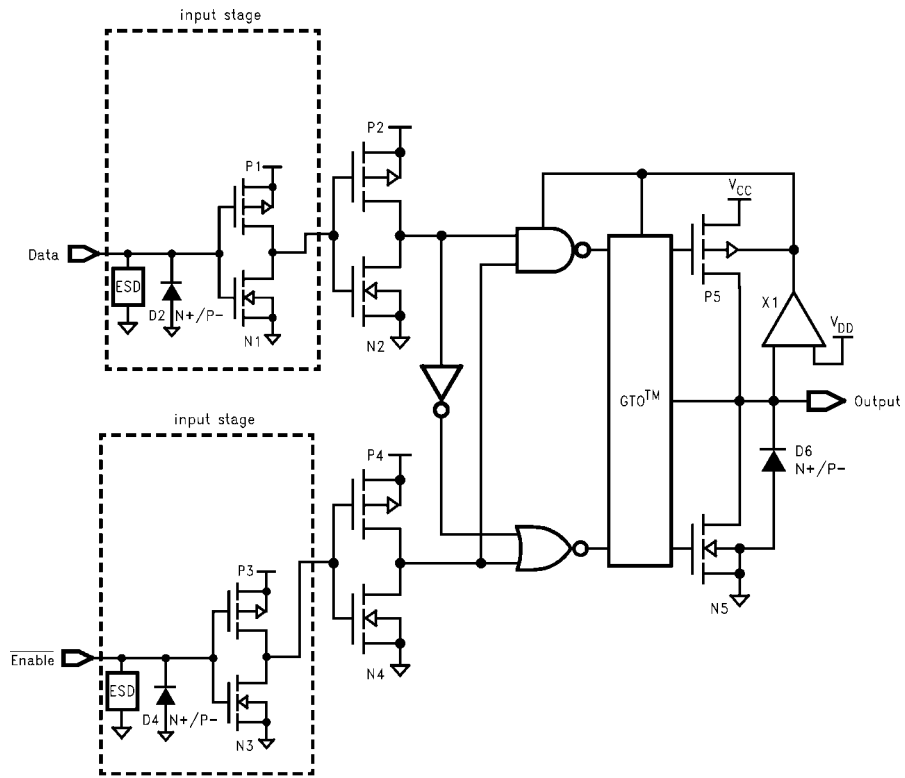


FIGURE 2. Waveforms (Input Characteristics; f = 1MHz, t_r = t_f = 3ns)

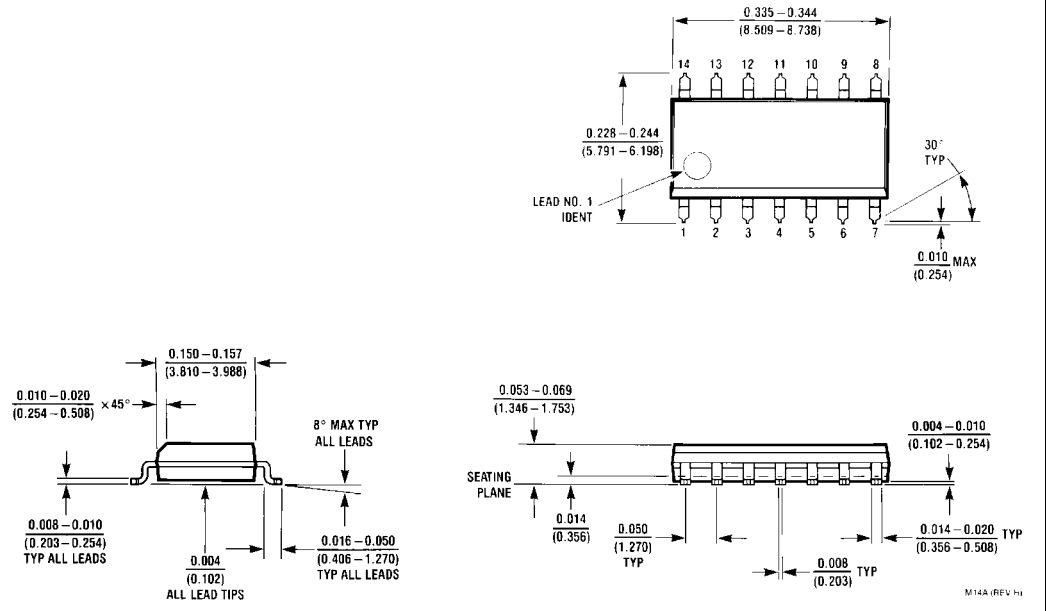
Symbol	V _{CC}		
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V
V _{mi}	1.5V	1.5V	V _{CC} /2
V _{mo}	1.5V	1.5V	V _{CC} /2
V _x	V _{OL} + 0.3V	V _{OL} + 0.3V	V _{OL} + 0.15V
V _y	V _{OH} - 0.3V	V _{OH} - 0.3V	V _{OH} - 0.15V

Schematic Diagram Generic for LCX Family



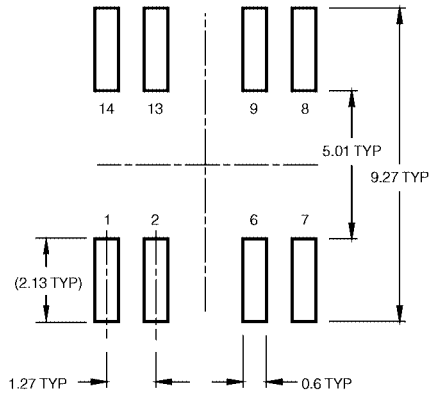
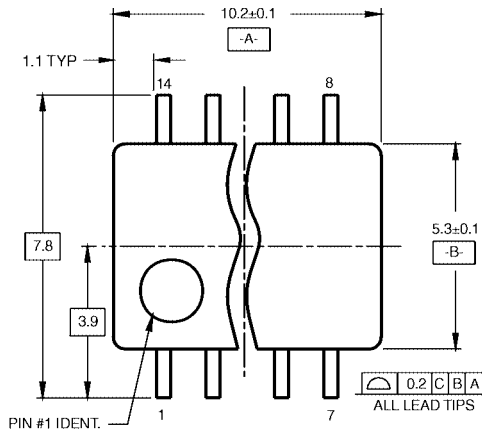
74LCX10

Physical Dimensions inches (millimeters) unless otherwise noted

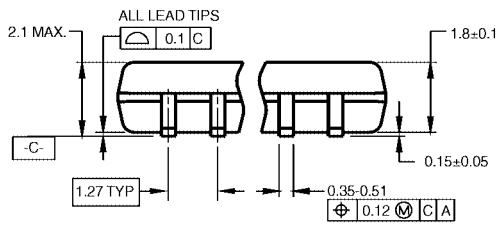


14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A

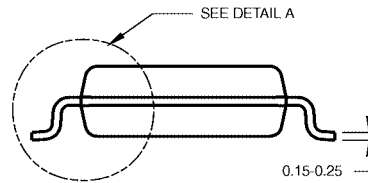
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



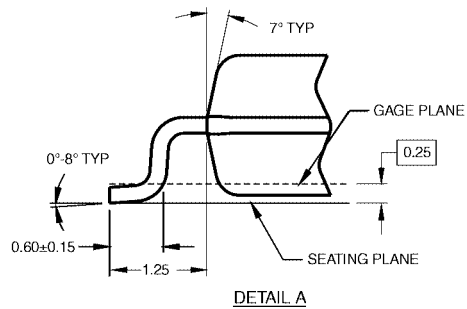
DIMENSIONS ARE IN MILLIMETERS



NOTES:

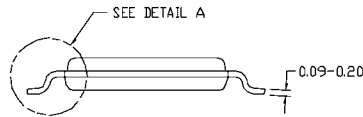
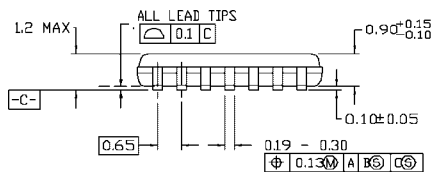
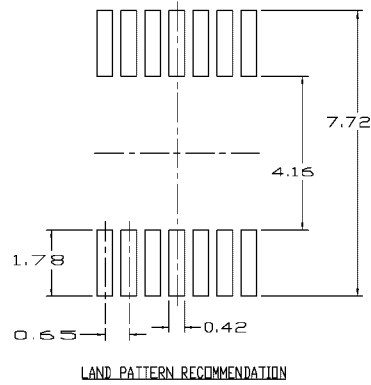
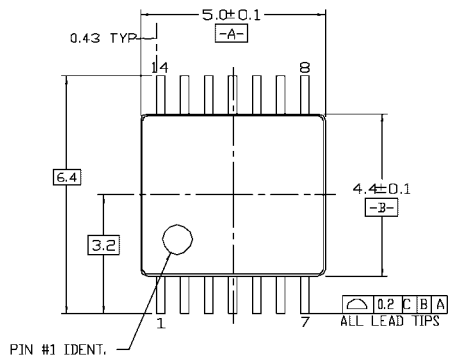
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- B. DIMENSIONS ARE IN MILLIMETERS.
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M14DRevB1



Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M14D

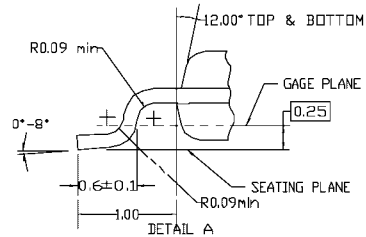
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

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- B. DIMENSIONS ARE IN MILLIMETERS
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- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD



14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

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