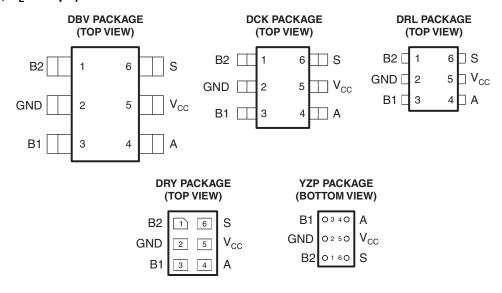
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FEATURES

- 1.65-V to 5.5-V V_{CC} Operation
- **Useful for Both Analog and Digital Applications**
- Specified Break-Before-Make Switching
- Rail-to-Rail Signal Handling
- **High Degree of Linearity**
- High Speed, Typically 0.5 ns $(V_{CC} = 3 \text{ V}, C_L = 50 \text{ pF})$

- Low On-State Resistance, Typically \approx 6 Ω $(V_{CC} = 4.5 V)$
- Latch-Up Performance Exceeds 100 mA Per JESD 78. Class II
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This single-pole, double-throw (SPDT) analog switch is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G3157 can handle both analog and digital signals. The device permits signals with amplitudes of up to V_{CC} (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74LVC1G3157YZPR	C5_
	SON - DRY	Reel of 5000	SN74LVC1G3157DRYR	C5_
-40°C to 85°C	SOT (SOT-23) - DBV	Reel of 3000	SN74LVC1G3157DBVR	CC5_
	SOT (SC-70) – DCK	Reel of 3000	SN74LVC1G3157DCKR	C5_
	SOT (SOT-553) – DRL	Reel of 4000	SN74LVC1G3157DRLR	C5_

⁽¹⁾ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

DBV/DCK/DRL/DRY: The actual top-side marking has one additional character that designates the assembly/test site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



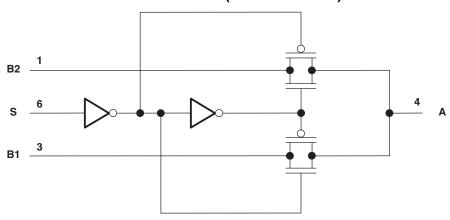
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FUNCTION TABLE

CONTROL INPUT S	ON CHANNEL
L	B1
Н	B2

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range ⁽²⁾		-0.5	6.5	V
V_{IN}	Control input voltage range ⁽²⁾⁽³⁾		-0.5	6.5	V
V _{I/O}	Switch I/O voltage range (2)(3)(4)(5)		-0.5	V _{CC} + 0.5	V
I_{IK}	Control input clamp current	V _{IN} < 0		-50	mA
I _{IOK}	I/O port diode current	V _{I/O} < 0 or V _{I/O} > V _{CC}		±50	mA
I _{I/O}	On-state switch current ⁽⁶⁾	$V_{I/O} = 0$ to V_{CC}		±128	mA
	Continuous current through V _{CC} or GNI	D		±100	mA
		DBV package		165	
		DCK package		259	
θ_{JA}	Package thermal impedance (7)	DRL package		142	°C/W
		DRY package		234	
		YZP package		123	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

All voltages are with respect to ground unless otherwise specified.

This value is limited to 5.5 V maximum.

(6)

The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

 V_{I} , V_{O} , V_{A} , and V_{Bn} are used to denote specific conditions for $V_{I/O}$. I_{I} , I_{O} , I_{A} , and I_{Bn} are used to denote specific conditions for $I_{I/O}$.

The package thermal impedance is calculated in accordance with JESD 51-7.

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Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V_{CC}			1.65	5.5	V
$V_{I/O}$			0	V_{CC}	٧
V_{IN}			0	5.5	٧
\/	Lligh level input valtage, control input	V _{CC} = 1.65 V to 1.95 V	$V_{CC} \times 0.75$		V
V_{IH}	ligh-level input voltage, control input $V_{CC} = 2.3 \text{ V to } 5.5 \text{ V}$		$V_{CC} \times 0.7$		V
\/	Low level input veltage, control input	V _{CC} = 1.65 V to 1.95 V		$V_{CC} \times 0.25$	V
V_{IL}	Low-level input voltage, control input	Voltage, control input $V_{CC} = 2.3 \text{ V to } 5.5 \text{ V}$		V _{CC} × 0.3	V
		V _{CC} = 1.65 V to 1.95 V		20	
Δt/Δν	Input transition vice or fall rate	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		20	ns/V
ΔυΔν	Input transition rise or fall rate	V _{CC} = 3 V to 3.6 V		10	IIS/V
		V _{CC} = 4.5 V to 5.5 V		10	
T _A	Operating free-air temperature		-40	85	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			V _{cc}	MIN TYP(1)	MAX	UNIT	
			$V_I = 0 V$	$I_O = 4 \text{ mA}$	1.65 V	11	20		
			V _I = 1.65 V	$I_O = -4 \text{ mA}$	1.05 V	15	50		
	r _{on} On-state switch resistance ⁽²⁾			$V_I = 0 V$	$I_O = 8 \text{ mA}$	2.3 V	8	12	
			$V_1 = 2.3 \text{ V}$	$I_O = -8 \text{ mA}$	2.3 V	11	30		
r _{on}		See Figure 1 and Figure 2	$V_I = 0 V$	I _O = 24 mA	3 V	7	9	Ω	
		l igaio _	$V_I = 3 V$	$I_O = -24 \text{ mA}$	3 V	9	20		
			$V_I = 0 V$	$I_O = 30 \text{ mA}$		6	7		
			$V_1 = 2.4 \text{ V}$	$I_O = -30 \text{ mA}$	4.5 V	7	12		
			$V_1 = 4.5 \text{ V}$	$I_O = -30 \text{ mA}$		7	15		
		$0 \le V_{Bn} \le V_{CC}$ (see Figure 1 and Figure 2)		$I_A = -4 \text{ mA}$	1.65 V		140		
-	On-state switch resistance			$I_A = -8 \text{ mA}$	2.3 V	45		Ω	
r _{range}	over signal range ⁽²⁾⁽³⁾			$I_A = -24 \text{ mA}$	3 V		18	22	
			$I_A = -30 \text{ mA}$	4.5 V		10			
			V _{Bn} = 1.15	I _A = -4 mA	1.65 V	0.5			
۸	Difference of on-state resistance between	Coo Figure 4	V _{Bn} = 1.6 V	$I_A = -8 \text{ mA}$	2.3 V	0.1		Ω	
Δr_{on}	switches ⁽²⁾⁽⁴⁾⁽⁵⁾	See Figure 1	V _{Bn} = 2.1 V	$I_A = -24 \text{ mA}$	3 V	0.1		22	
			V _{Bn} = 3.15	I _A = -30 mA	4.5 V	0.1			
				$I_A = -4 \text{ mA}$	1.65 V	110			
_	ON resistance flatness ⁽²⁾⁽⁴⁾⁽⁶⁾	0 < 1/ < 1/		$I_A = -8 \text{ mA}$	2.3 V	26		Ω	
r _{on(flat)}	ON resistance namess (2)(4)(6)	$0 \le V_{Bn} \le V_{CC}$		$I_A = -24 \text{ mA}$	3 V	9		22	
			$I_A = -30 \text{ mA}$	4.5 V	4				

⁽¹⁾ $T_A = 25^{\circ}C$

⁽²⁾ Measured by the voltage drop between I/O pins at the indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A or B) ports.

 ⁽⁴⁾ Δr_{on} = r_{on(max)} - r_{on(min)} measured at identical V_{CC}, temperature, and voltage levels
 (5) This parameter is characterized, but not tested in production.

Flatness is defined as the difference between the maximum and minimum values of ON resistance over the specified range of conditions.

SN74LVC1G3157 SINGLE-POLE, DOUBLE-THROW ANALOG SWITCH

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Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	V _{cc}	MIN TYP ⁽¹⁾	MAX	UNIT		
I _{off} ⁽⁷⁾	Off-state switch leakage		$0 \le V_I, V_O \le V_{CC}$	1.65 V to		±1	μΑ		
· · ·	current		(see Figure 3)	5.5 V	±0.05	±1 ⁽¹⁾	•		
lac s	On-state switch leakage		$V_I = V_{CC}$ or GND, $V_O = Open$	5.5 V		±1	μΑ		
I _{S(on)}	current		(see Figure 4)	3.5 V		±0.1 ⁽¹⁾	μΛ		
	Control input current 0		Control input current		$0 \le V_{IN} \le V_{CC}$	0 V to		±1	μΑ
I _{IN}			0 ≥ vIN≥ vCC	5.5 V	±0.05	±1 ⁽¹⁾	μΑ		
I _{CC}	Supply current		V _{IN} = V _{CC} or GND	5.5 V	1	10	μΑ		
ΔI_{CC}	Supply-current change		$V_{IN} = V_{CC} - 0.6 \text{ V}$	5.5 V		500	μΑ		
C _{in}	Control input capacitance	S		5 V	2.7		pF		
C _{io(off)}	Switch input/ouput capacitance	Bn		5 V	5.2		pF		
_	Switch input/ouput	Bn		5 V	17.3		pF		
C _{io(on)}	capacitance	Α		5 V	17.3		рг		

⁽⁷⁾ I_{off} is the same as $I_{\text{S(off)}}$ (off-state switch leakage current).

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Analog Switch Characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{cc}	TYP	UNIT
				1.65 V	300	
Frequency	A D -	D A	$R_L = 50 \Omega$,	2.3 V	300	N 41 1-
response ⁽¹⁾ (switch on)	A or Bn	Bn or A	f _{in} = sine wave (see Figure 6)	3 V	300	MHz
,			,	4.5 V	300	
				1.65 V	-54	
Crosstalk (2)	D4 D0	DO D4	$R_L = 50 \Omega$,	2.3 V	-54	-ID
(between switches)	B1 or B2	B2 or B1	f _{in} = 10 MHz (sine wave) (see Figure 7)	3 V	-54	dB
,	(coc i igalo i)		(cooriganor)	4.5 V	-54	
				1.65 V	– 57	dB
Feed-through	A or Bn	Bn or A	$C_L = 5 \text{ pF}, R_L = 50 \Omega,$	2.3 V	-57	
attenuation ⁽²⁾ (switch off)			f _{in} = 10 MHz (sine wave) (see Figure 8)	3 V	-57	
,			,	4.5 V	-57	
Ob (3)	0	Δ.	$C_L = 0.1 \text{ nF}, R_L = 1 \text{ M}\Omega$	3.3 V	3	0
Charge injection (3)	S	Α	(see Figure 9)	5 V	7	рС
				1.65 V	0.1	
Total harmonic	A D -	D A	$V_{I} = 0.5 \text{ Vp-p}, R_{L} = 600 \Omega,$	2.3 V	0.025	%
distortion	A or Bn Br	Bn or A	f _{in} = 600 Hz to 20 kHz (sine wave) (see Figure 10)	3 V	0.015	
				4.5 V	0.01	

⁽¹⁾ Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads -3 dB.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5 and Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1		V _{CC} = ± 0.2		V _{CC} = ± 0.3		V _{CC} =	5 V 5 V	UNIT
	(INPOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd} ⁽¹⁾	A or Bn	Bn or A		2		1.2		0.8		0.3	ns
t _{en} ⁽²⁾	c	D ₂	7	24	3.5	14	2.5	7.6	1.7	5.7	20
t _{dis} (3)	S	Bn	3	13	2	7.5	1.5	5.3	0.8	3.8	ns
t _{B-M} ⁽⁴⁾			0.5		0.5		0.5		0.5		ns

⁽¹⁾ t_{pd} is the slower of t_{PLH} or t_{PHL}. The propagation delay is calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

 ⁽²⁾ Adjust f_{in} voltage to obtain 0 dBm at input.
 (3) Specified by design

t_{en} is the slower of t_{PZL} or t_{PZH}.

t_{di}s is the slower of t_{PLZ} or t_{PHZ}.

⁽⁴⁾ Specified by design



PARAMETER MEASUREMENT INFORMATION

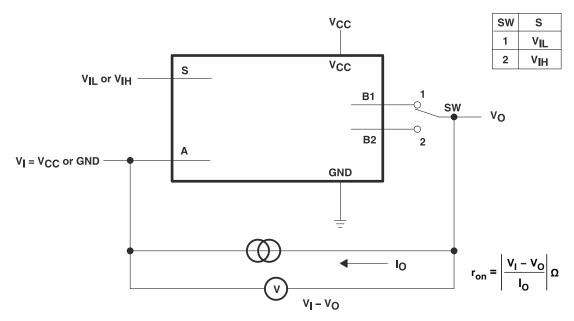


Figure 1. On-State Resistance Test Circuit

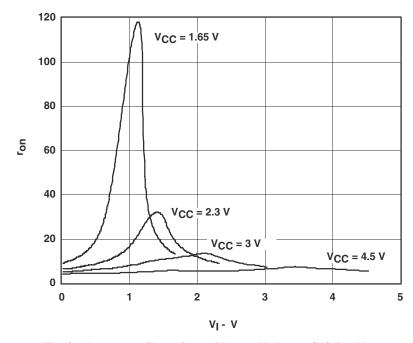
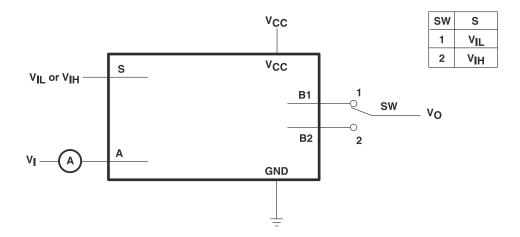


Figure 2. Typical r_{on} as a Function of Input Voltage (V_I) for $V_{I} = 0$ to V_{CC}





 $\begin{array}{l} \text{Condition 1: V_I = GND, V_O = V_{CC}} \\ \text{Condition 2: V_I = V_{CC}, V_O = GND} \end{array}$

Figure 3. Off-State Switch Leakage-Current Test Circuit

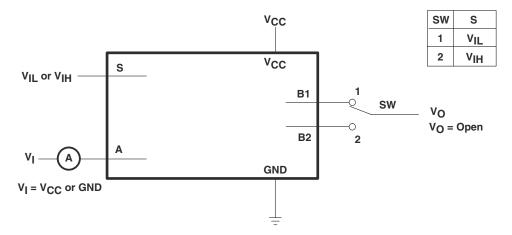
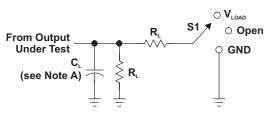


Figure 4. On-State Switch Leakage-Current Test Circuit

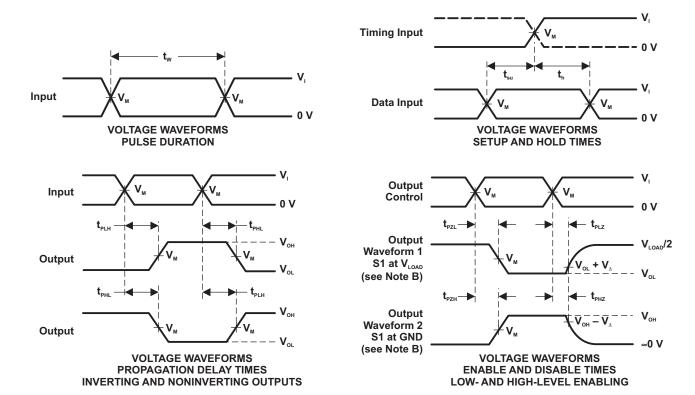




TEST	S1
t _{PLH} /t _{PHL}	Open
t_{PLZ}/t_{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCU	ш
------------	---

	INF	PUTS	.,,	.,		_	.,
V _{cc}	V,	t,/t,	V _M	V _{LOAD}	C _∟	R _L	V _A
1.8 V ± 0.15 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	50 pF	500 Ω	0.3 V
2.5 V ± 0.2 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	V _{cc}	≤2.5 ns	V _{cc} /2	2 × V _{cc}	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V _{cc}	≤2.5 ns	V _{cc} /2	2 × V _{cc}	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_o = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms



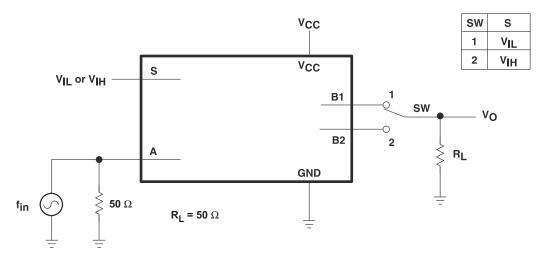


Figure 6. Frequency Response (Switch On)

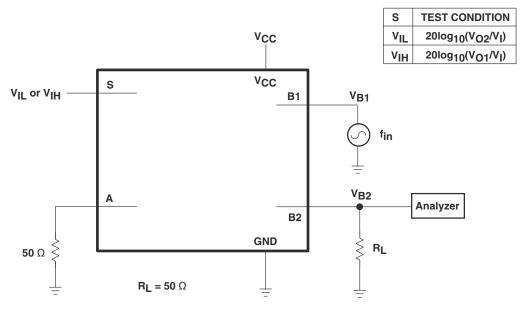


Figure 7. Crosstalk (Between Switches)



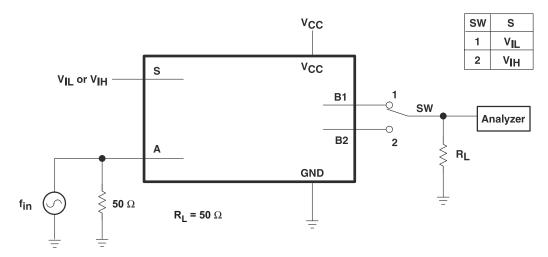


Figure 8. Feedthrough

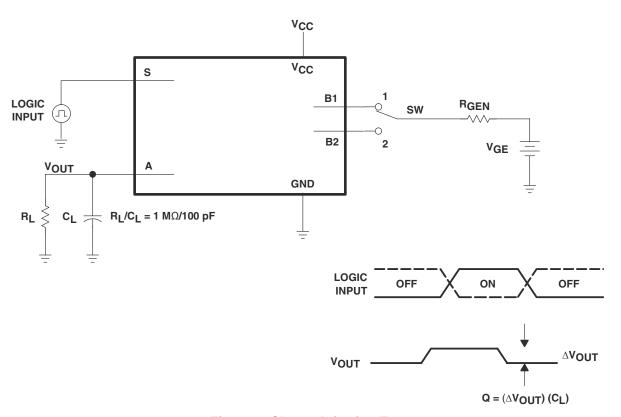


Figure 9. Charge-Injection Test



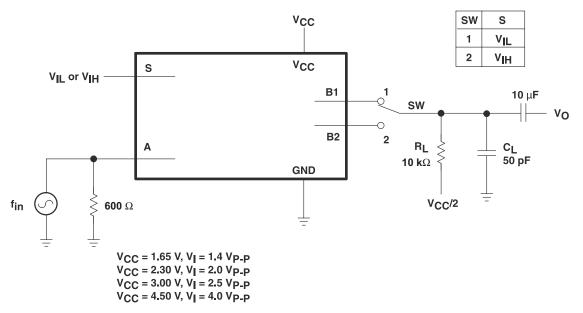


Figure 10. Total Harmonic Distortion

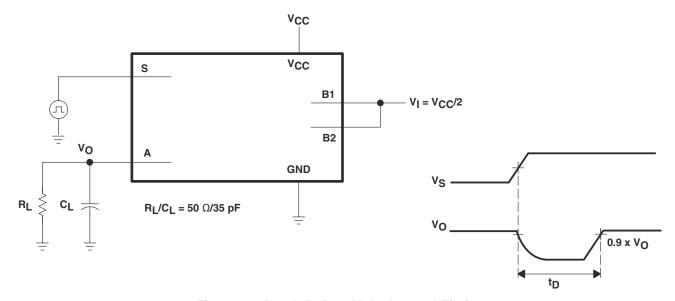


Figure 11. Break-Before-Make Internal Timing







PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Packag Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74LVC1G3157DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G3157DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G3157DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G3157DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G3157DRLRG4	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G3157DRYRG4	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G3157DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G3157DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G3157DGVR	PREVIEW	SOT-23	DBV	6		TBD	Call TI	Call TI
SN74LVC1G3157DRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G3157DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G3157YZPR	ACTIVE	WCSP	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE OPTION ADDENDUM

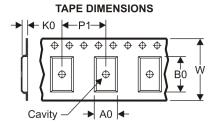
22-Oct-2007

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by to Customer on an annual basis.



TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G3157DBVR	SOT-23	DBV	6	3000	180.0	9.2	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G3157DCKR	SC70	DCK	6	3000	180.0	9.2	2.24	2.34	1.22	4.0	8.0	Q3
SN74LVC1G3157DRLR	SOT	DRL	6	4000	180.0	9.2	1.78	1.78	0.69	4.0	8.0	Q3
SN74LVC1G3157DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G3157DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74LVC1G3157DCKR	SC70	DCK	6	3000	205.0	200.0	33.0
SN74LVC1G3157DRLR	SOT	DRL	6	4000	202.0	201.0	28.0
SN74LVC1G3157DRYR	SON	DRY	6	5000	220.0	205.0	50.0

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



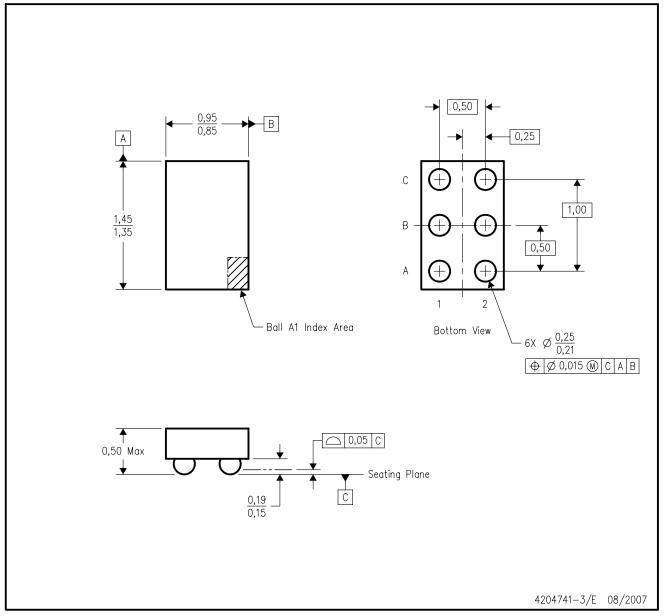
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- Falls within JEDEC MO-178 Variation AB, except minimum lead width.



YZP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY

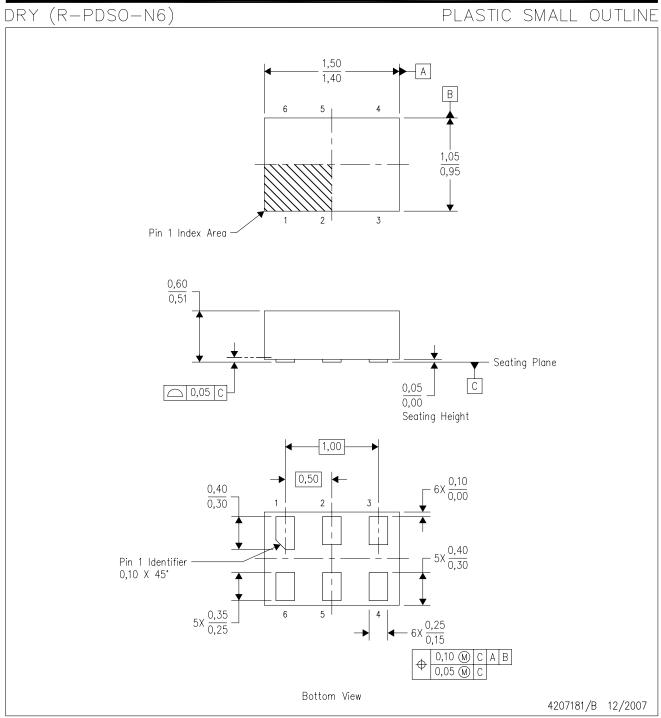


NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. NanoFree $^{\text{TM}}$ package configuration.
- D. This package is lead-free. Refer to the 6 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.





NOTES: All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
 C. SON (Small Outline No-Lead) package configuration.
 D. This package complies to JEDEC MO-287 variation UFAD.



DRL (R-PDSO-N6)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs.

 Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
- D. JEDEC package registration is pending.



DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AB.



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