

**FAIRCHILD**  
SEMICONDUCTOR™

November 1988  
Revised November 1999

## 74AC74 • 74ACT74

### Dual D-Type Positive Edge-Triggered Flip-Flop

#### General Description

The AC/ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q,  $\bar{Q}$ ) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

- LOW input to  $\bar{S}_D$  (Set) sets Q to HIGH level
- LOW input to  $\bar{C}_D$  (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both Q and  $\bar{Q}$  HIGH

#### Features

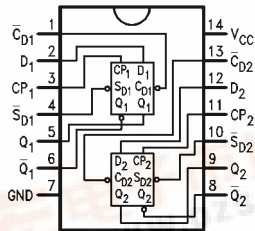
- $I_{CC}$  reduced by 50%
- Output source/sink 24 mA
- ACT74 has TTL-compatible inputs

#### Ordering Code:

Order Number	Package Number	Package Description
74AC74SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
74AC74SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC74MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC74PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT74SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
74ACT74SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT74MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT74PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

#### Connection Diagram



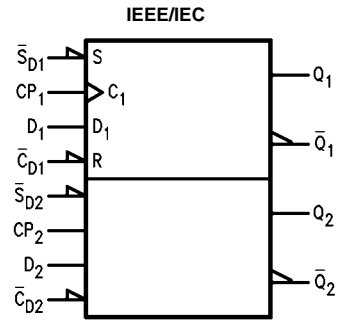
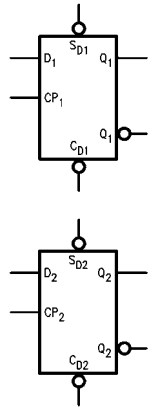
#### Pin Descriptions

Pin Names	Description
$D_1, D_2$	Data Inputs
$CP_1, CP_2$	Clock Pulse Inputs
$\bar{C}_{D1}, \bar{C}_{D2}$	Direct Clear Inputs
$\bar{S}_{D1}, \bar{S}_{D2}$	Direct Set Inputs
$Q_1, \bar{Q}_1, Q_2, \bar{Q}_2$	Outputs

FACT™ is a trademark of Fairchild Semiconductor Corporation.



### Logic Symbols



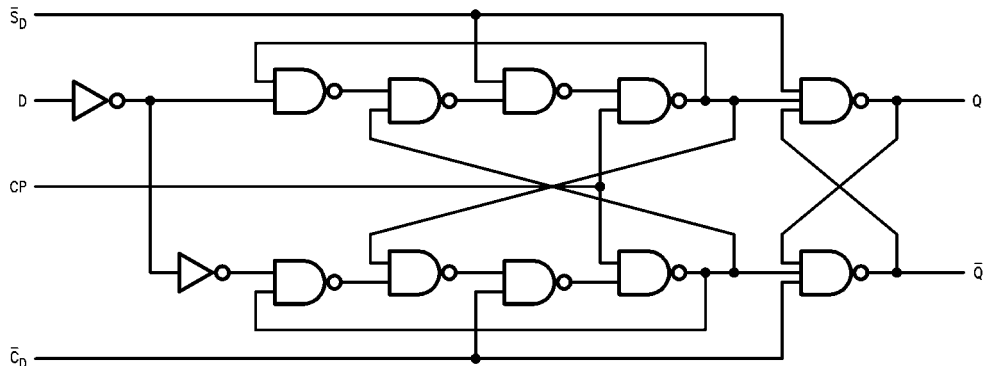
### Truth Table

(Each Half)

Inputs				Outputs	
$\bar{S}_D$	$\bar{C}_D$	CP	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↗	H	H	L
H	H	↘	L	L	H
H	H	L	X	$Q_0$	$\bar{Q}_0$

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 ↗ = LOW-to-HIGH Clock Transition  
 $Q_0$  ( $\bar{Q}_0$ ) = Previous Q ( $\bar{Q}$ ) before LOW-to-HIGH Transition of Clock

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature ( $T_J$ )	
PDIP	140°C

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
AC Devices	
$V_{IN}$ from 30% to 70% of $V_{CC}$	
$V_{CC}$ @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
ACT Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

**DC Electrical Characteristics for AC**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	Units	Conditions
			Typ	Guaranteed Limits			
$V_{IH}$	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
$V_{IL}$	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
$V_{OH}$	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu A$
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -12$ mA $I_{OH} = -24$ m $I_{OH} = -24$ m (Note 2)
		4.5		3.86	3.76		
		5.5		4.86	4.76		
$V_{OL}$	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu A$
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 12$ mA $I_{OL} = 24$ mA $I_{OL} = 24$ mA (Note 2)
		4.5		0.36	0.44		
		5.5		0.36	0.44		
$I_{IN}$ (Note 4)	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$	$\mu A$	$V_I = V_{CC}, GND$
$I_{OLD}$	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Max
$I_{OHD}$	Output Current (Note 3)	5.5			-75	mA	$V_{OHD} = 3.85V$ Min
$I_{CC}$ (Note 4)	Maximum Quiescent Supply Current	5.5		2.0	20.0	$\mu A$	$V_{IN} = V_{CC}$ or GND

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

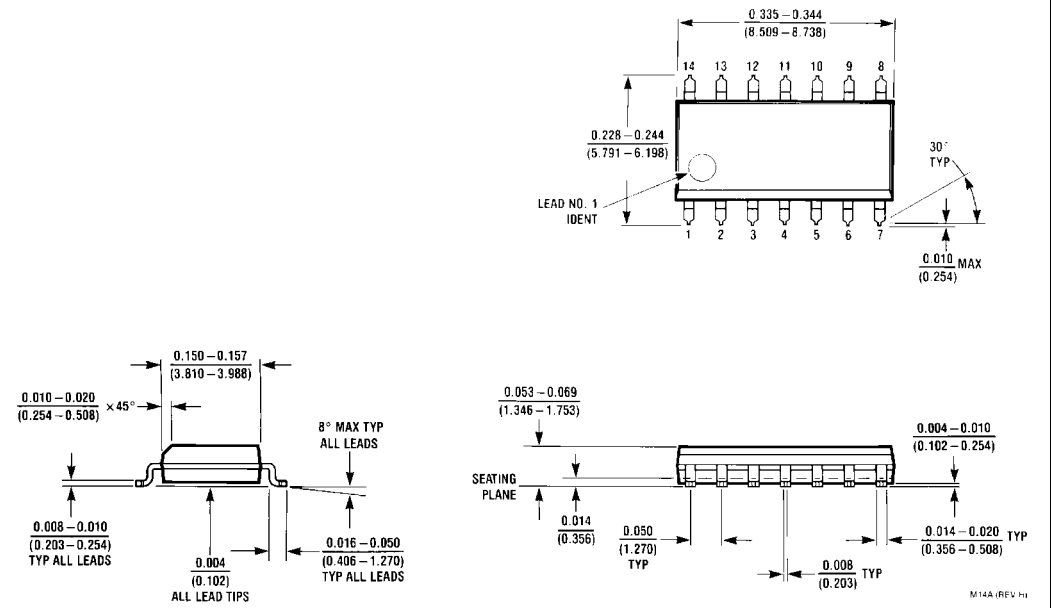
**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 4:**  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .

DC Electrical Characteristics for ACT								
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum HIGH Level	4.5	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	
	Input Voltage	5.5	1.5	2.0	2.0			
V <sub>IL</sub>	Maximum LOW Level	4.5	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	
	Output Voltage	5.5	1.5	0.8	0.8			
V <sub>OH</sub>	Minimum HIGH Level	4.5	4.49	4.4	4.4	V	I <sub>OUT</sub> = -50 μA	
	Output Voltage	5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -24 mA (Note 5)	
		5.5		4.86	4.76			
V <sub>OL</sub>	Maximum LOW Level	4.5	0.001	0.1	0.1	V	I <sub>OUT</sub> = 50 μA	
	Output Voltage	5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 24 mA (Note 5)	
		5.5		0.36	0.44			
I <sub>IN</sub>	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND	
I <sub>CCCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	0.6		1.5	mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V	
I <sub>OLD</sub>	Minimum Dynamic	5.5			75	mA	V <sub>OLD</sub> = 1.65V Max	
I <sub>OHD</sub>	Output Current (Note 6)	5.5			-75	mA	V <sub>OHD</sub> = 3.85V Min	
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		2.0	20.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	
<b>Note 5:</b> All outputs loaded; thresholds on input associated with output under test. <b>Note 6:</b> Maximum test duration 2.0 ms, one output loaded at a time.								
AC Electrical Characteristics for AC								
Symbol	Parameter	V <sub>CC</sub> (V) (Note 7)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	3.3 5.0	100 140	125 160		95 125		MHz
t <sub>PLH</sub>	Propagation Delay C <sub>Dn</sub> or S <sub>Dn</sub> to Q <sub>n</sub> or Q <sub>n</sub>	3.3 5.0	3.5 2.5	8.0 6.0	12.0 9.0	2.5 2.0	13.0 10.0	ns
	Propagation Delay C <sub>Dn</sub> or S <sub>Dn</sub> to Q <sub>n</sub> or Q <sub>n</sub>	3.3 5.0	4.0 3.0	10.5 8.0	12.0 9.5	3.5 2.5	13.5 10.5	ns
t <sub>PLH</sub>	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or Q <sub>n</sub>	3.3 5.0	4.5 3.5	8.0 6.0	13.5 10.0	4.0 3.0	16.0 10.5	ns
	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or Q <sub>n</sub>	3.3 5.0	3.5 2.5	8.0 6.0	14.0 10.0	3.5 2.5	14.5 10.5	ns
<b>Note 7:</b> Voltage Range 3.3 is 3.3V ± 0.3V Voltage Range 5.0 is 5.0V ± 0.5V								

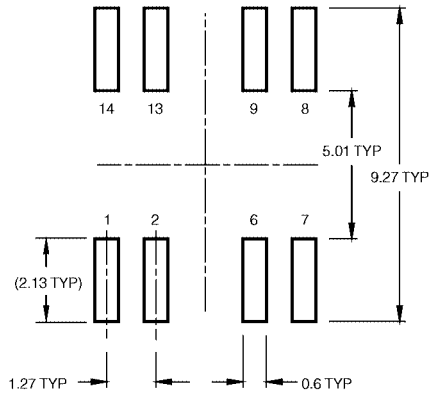
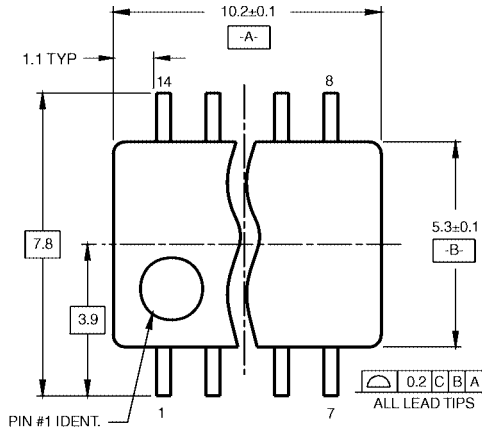
AC Operating Requirements for AC								
Symbol	Parameter	V <sub>CC</sub> (V) (Note 8)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units	
			Typ	Guaranteed Minimum				
t <sub>S</sub>	Set-up Time, HIGH or LOW D <sub>n</sub> to CP <sub>n</sub>	3.3	1.5	4.0	4.5		ns	
			5.0	1.0	3.0	3.0		
t <sub>H</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP <sub>n</sub>	3.3	-2.0	0.5	0.5		ns	
			5.0	-1.5	0.5	0.5		
t <sub>W</sub>	CP <sub>n</sub> or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	3.3	3.0	5.5	7.0		ns	
			5.0	2.5	4.5	5.0		
t <sub>rec</sub>	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	3.3	-2.5	0	0		ns	
			5.0	-2.0	0	0		
<b>Note 8:</b> Voltage Range 3.3 is 3.3V ± 0.3V Voltage Range 5.0 is 5.0V ± 0.5V								
AC Electrical Characteristics for ACT								
Symbol	Parameter	V <sub>CC</sub> (V) (Note 9)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	5.0	145	210		125	MHz	
t <sub>PLH</sub>	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q <sub>n</sub> or $\overline{Q}_n$	5.0	3.0	5.5	9.5	2.5	10.5	ns
t <sub>PHL</sub>	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q <sub>n</sub> or $\overline{Q}_n$	5.0	3.0	6.0	10.0	3.0	11.5	ns
t <sub>PLH</sub>	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or $\overline{Q}_n$	5.0	4.0	7.5	11.0	4.0	13.0	ns
t <sub>PHL</sub>	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or $\overline{Q}_n$	5.0	3.5	6.0	10.0	3.0	11.5	ns
<b>Note 9:</b> Voltage Range 5.0 is 5.0V ± 0.5V								
AC Operating Requirements for ACT								
Symbol	Parameter	V <sub>CC</sub> (V) (Note 10)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units	
			Typ	Guaranteed Minimum				
t <sub>S</sub>	Set-up Time, HIGH or LOW D <sub>n</sub> to CP <sub>n</sub>	5.0	1.0	3.0	3.5		ns	
			5.0	-0.5	1.0	1.0		
t <sub>H</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP <sub>n</sub>	5.0	-0.5	1.0	1.0		ns	
			5.0	3.0	5.0	6.0		
t <sub>W</sub>	CP <sub>n</sub> or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	5.0	3.0	5.0	6.0		ns	
			5.0	-2.5	0	0		
t <sub>rec</sub>	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	5.0	-2.5	0	0		ns	
			5.0	-2.5	0	0		
<b>Note 10:</b> Voltage Range 5.0 is 5.0V ± 0.5V								
Capacitance								
Symbol	Parameter	Typ	Units	Conditions				
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN				
C <sub>PD</sub>	Power Dissipation Capacitance	35.0	pF	V <sub>CC</sub> = 5.0V				

**Physical Dimensions** inches (millimeters) unless otherwise noted

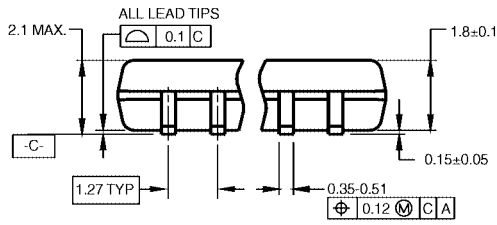


**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body  
Package Number M14A**

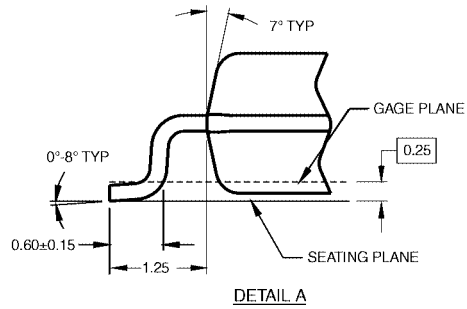
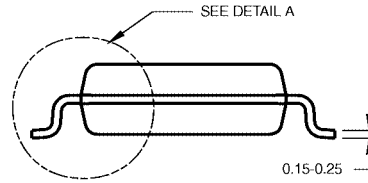
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

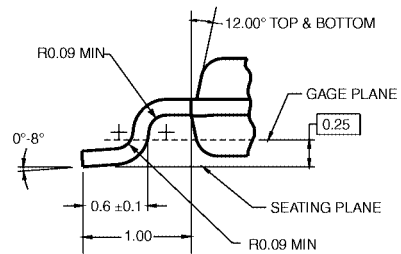
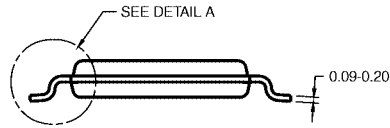
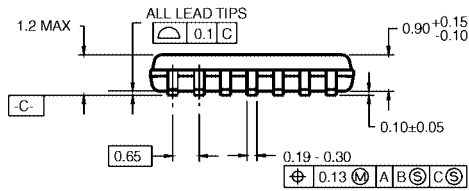
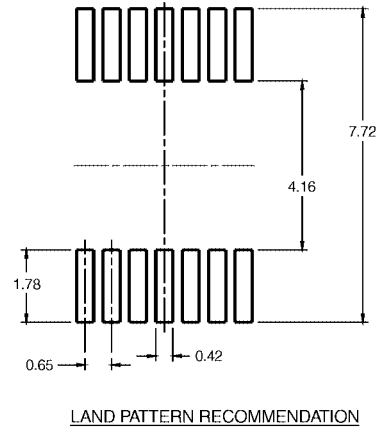
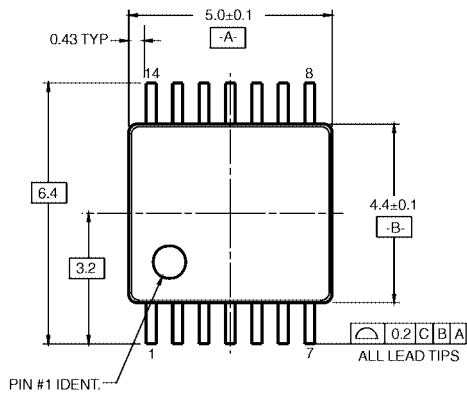
NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M14D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
  - D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

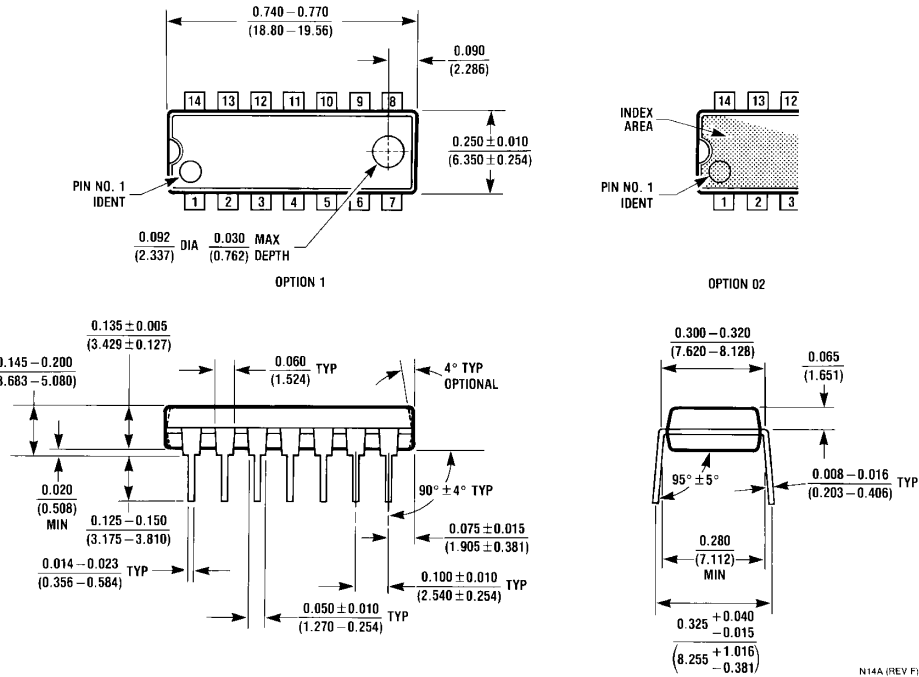
MTC14RevC3

DETAIL A

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14**



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A**

N14A (REV P)

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)