

INTEGRATED CIRCUITS

DATA SHEET

74AHC74; 74AHCT74

Dual D-type flip-flop with set and reset; positive-edge trigger

Product specification
Supersedes data of 1999 Aug 05
File under Integrated Circuits, IC06

1999 Sep 23

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74AHC74; 74AHCT74

FEATURES

- ESD protection:
HBM EIA/JESD22-A114-A
exceeds 2000 V
MM EIA/JESD22-A115-A
exceeds 200 V
- Balanced propagation delays
- Inputs accepts voltages higher than V_{CC}
- For AHC only:
operates with CMOS input levels
- For AHCT only:
operates with TTL input levels
- Output capability: standard
- I_{CC} category: flip-flops
- Specified from
-40 to +85 and +125 °C.

DESCRIPTION

The 74AHC/AHCT74 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7A.

The 74AHC/AHCT74 dual positive-edge triggered, D-type flip-flops with individual data (D) inputs, clock (CP) inputs, set (\overline{S}_D) and reset (\overline{R}_D) inputs; also complementary Q and \overline{Q} outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ °C}$; $t_r = t_f \leq 3.0\text{ ns}$.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			AHC	AHCT	
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n \overline{Q}	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	3.7	3.3	ns
	n \overline{S}_D , n \overline{R}_D to nQ, n \overline{Q}		3.7	3.7	ns
f_{max}	max. clock frequency		130	100	MHz
C_I	input capacitance	$V_I = V_{CC}$ or GND	4.0	4.0	pF
C_{PD}	power dissipation capacitance	$C_L = 50\text{ pF}$; $f = 1\text{ MHz}$; notes 1 and 2	12	16	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; f_o = output frequency in MHz;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in Volts.
2. The condition is $V_I = \text{GND}$ to V_{CC} .

FUNCTION TABLES

Table 1 See note 1

INPUT				OUTPUT	
n \overline{S}_D	n \overline{R}_D	nCP	nD	nQ	n \overline{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

Table 2 See note 1

INPUT				OUTPUT	
n \overline{S}_D	n \overline{R}_D	nCP	nD	n Q_{n+1}	n \overline{Q}_{n+1}
H	H	↑	L	L	H
H	H	↑	H	H	L

Note to Tables 1 and 2

1. H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
↑ = LOW-to-HIGH CP transition;
 Q_{n+1} = state after the next LOW-to-HIGH CP transition.

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ORDERING INFORMATION

OUTSIDE NORTH AMERICA	NORTH AMERICA	PACKAGE				
		TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74AHC74D	74AHC74D	-40 to +85 °C	14	SO	plastic	SOT108-1
74AHC74PW	74AHC74PW DH		14	TSSOP	plastic	SOT402-1
74AHCT74D	74AHCT74D		14	SO	plastic	SOT108-1
74AHCT74PW	74AHCT74PW DH		14	TSSOP	plastic	SOT402-1

PINNING

PIN	SYMBOL	DESCRIPTION
1 and 13	$1\bar{R}_D$ and $2\bar{R}_D$	asynchronous reset-direct input (active LOW)
2 and 12	1D and 2D	data inputs
3 and 11	1CP and 2CP	clock input (LOW-to-HIGH, edge-triggered)
4 and 10	$1\bar{S}_D$ and $2\bar{S}_D$	asynchronous set-direct input (active LOW)
5 and 9	1Q and 2Q	true flip-flop outputs
6 and 8	$1\bar{Q}$ and $2\bar{Q}$	complement flip-flop outputs
7	GND	ground (0 V)
14	V _{CC}	DC supply voltage

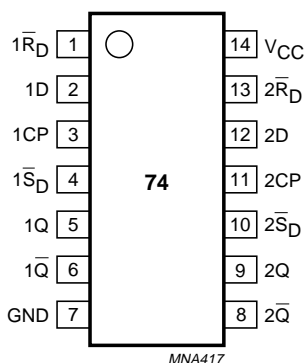


Fig.1 Pin configuration.

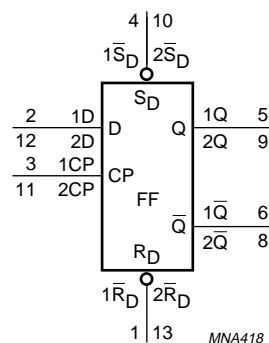
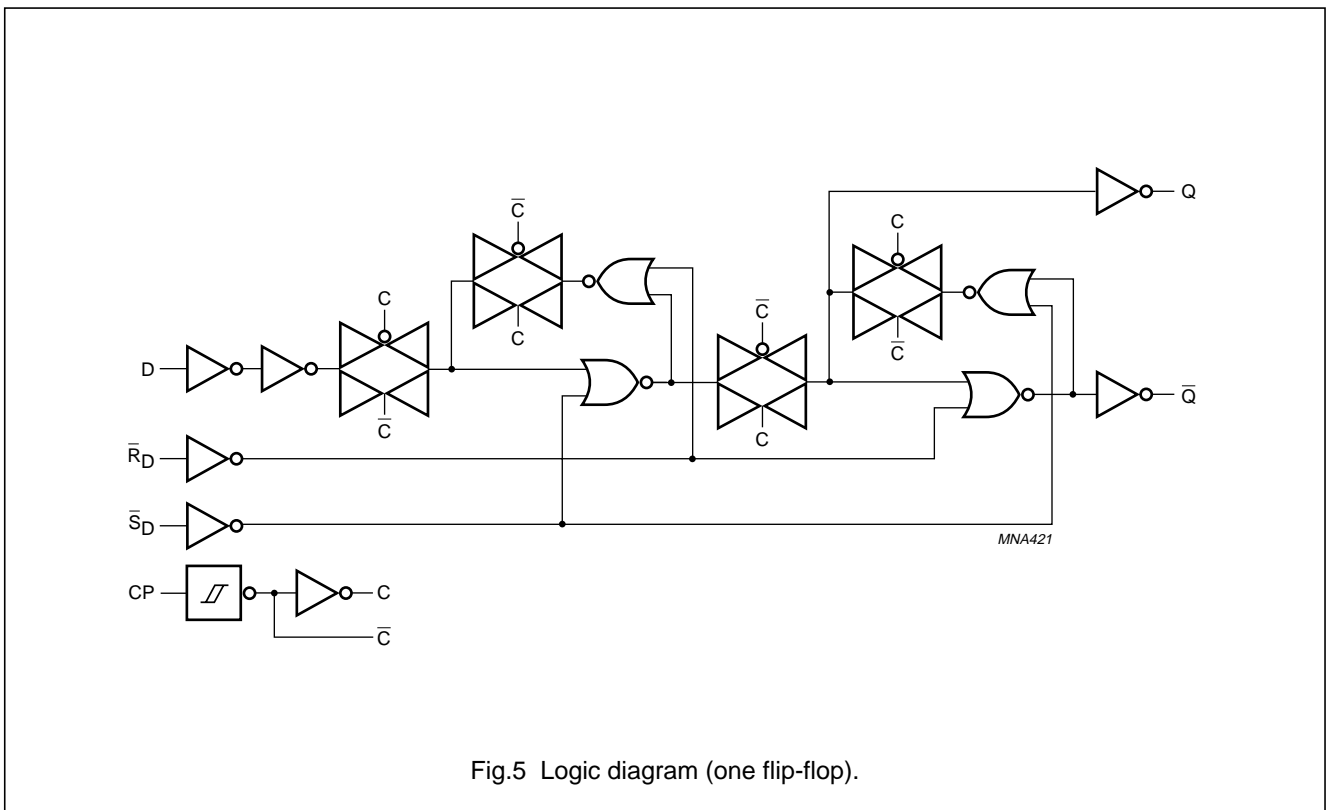
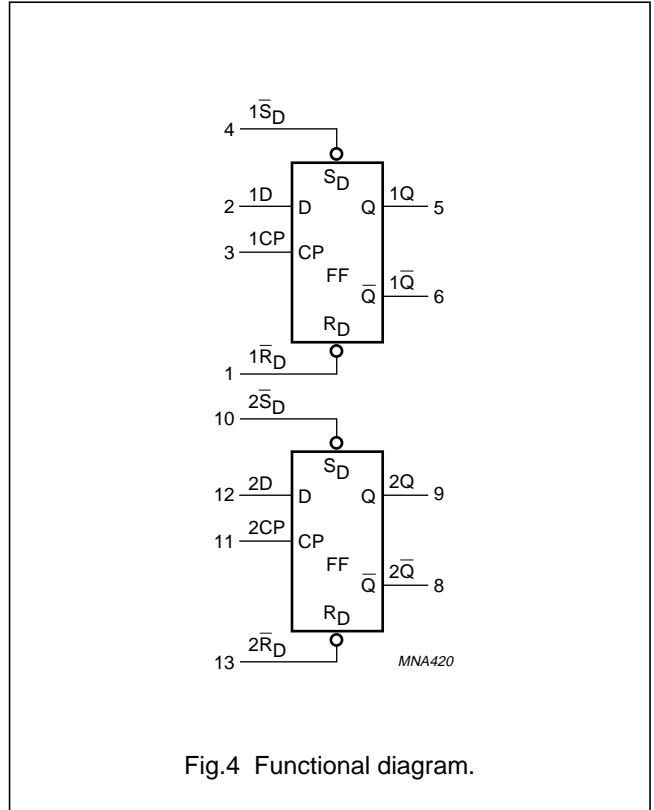
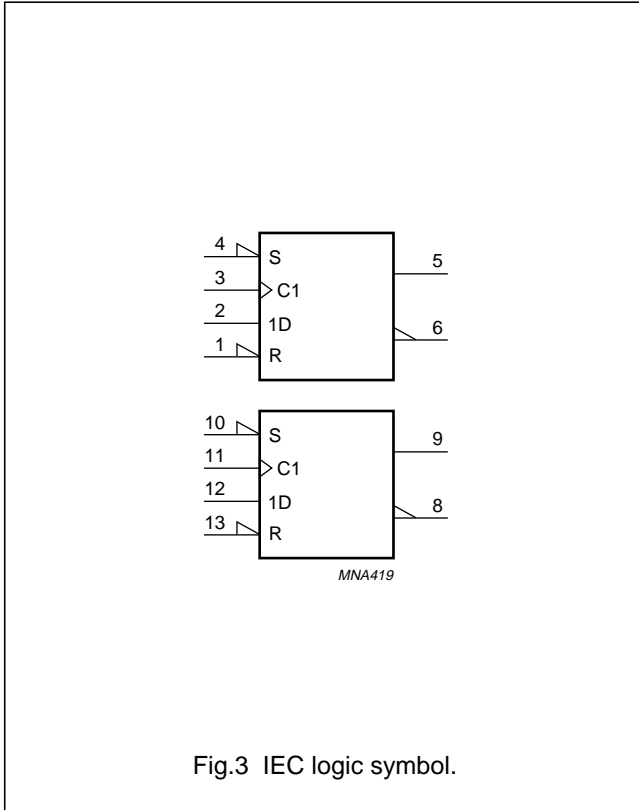


Fig.2 Logic diagram.

Dual D-type flip-flop with set and reset;
positive-edge trigger

74AHC74; 74AHCT74



Dual D-type flip-flop with set and reset; positive-edge trigger

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC			74AHCT			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V _{CC}	DC supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V _I	input voltage		0	–	5.5	0	–	5.5	V
V _O	output voltage		0	–	V _{CC}	0	–	V _{CC}	V
T _{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+85	–40	+25	+85	°C
			–40	+25	+125	–40	+25	+125	°C
t _r , t _f (Δt/Δf)	input rise and fall rates	V _{CC} = 3.3 V ±0.3 V	–	–	100	–	–	–	ns/V
		V _{CC} = 5 V ±0.5 V	–	–	20	–	–	20	

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CC}	DC supply voltage		–0.5	+7.0	V
V _I	input voltage		–0.5	+7.0	V
I _{IK}	DC input diode current	V _I < –0.5 V; note 1	–	–20	mA
I _{OK}	DC output diode current	V _O < –0.5 V or V _O > V _{CC} + 0.5 V; note 1	–	±20	mA
I _O	DC output source or sink current	–0.5 V < V _O < V _{CC} + 0.5 V	–	±25	mA
I _{CC}	DC V _{CC} or GND current		–	±75	mA
T _{stg}	storage temperature		–65	+150	°C
P _D	power dissipation per package	for temperature range: –40 to +85 °C; note 2	–	500	mW

Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- For SO packages: above 70 °C the value of P_D derates linearly with 8 mW/K.
For TSSOP packages: above 60 °C the value of P_D derates linearly with 5.5 mW/K.

Dual D-type flip-flop with set and reset; positive-edge trigger

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DC CHARACTERISTICS

74AHC family

Over recommended operating conditions; voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	T _{amb} (°C)								UNIT	
			OTHER	V _{CC} (V)	25			-40 to +85		-40 to +125		
					MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
V _{IH}	HIGH-level input voltage		2.0	1.5	–	–	1.5	–	1.5	–	V	
			3.0	2.1	–	–	2.1	–	2.1	–		
			5.5	3.85	–	–	3.85	–	3.85	–		
V _{IL}	LOW-level input voltage		2.0	–	–	0.5	–	0.5	–	0.5	V	
			3.0	–	–	0.9	–	0.9	–	0.9		
			5.5	–	–	1.65	–	1.65	–	1.65		
V _{OH}	HIGH-level output voltage; all outputs	V _I = V _{IH} or V _{IL} ; I _O = -50 μA	2.0	1.9	2.0	–	1.9	–	1.9	–	V	
			3.0	2.9	3.0	–	2.9	–	2.9	–		
			4.5	4.4	4.5	–	4.4	–	4.4	–		
	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; I _O = -4.0 mA	3.0	2.58	–	–	2.48	–	2.40	–	V	
			4.5	3.94	–	–	3.8	–	3.70	–		
V _{OL}	LOW-level output voltage; all outputs	V _I = V _{IH} or V _{IL} ; I _O = 50 μA	2.0	–	0	0.1	–	0.1	–	0.1	V	
			3.0	–	0	0.1	–	0.1	–	0.1		
			4.5	–	0	0.1	–	0.1	–	0.1		
	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; I _O = 4 mA	3.0	–	–	0.36	–	0.44	–	0.55	V	
			4.5	–	–	0.36	–	0.44	–	0.55		
I _I	input leakage current	V _I = V _{CC} or GND	5.5	–	–	0.1	–	1.0	–	2.0	μA	
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	5.5	–	–	±0.25	–	±2.5	–	±10.0	μA	
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	2.0	–	20	–	40	μA	
C _I	input capacitance		–	–	3	10	–	10	–	10	pF	

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74AHCT family

Over recommended operating conditions; voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T _{amb} (°C)							UNIT
		OTHER	V _{CC} (V)	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	2.0	–	2.0	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	–	0.8	–	0.8	V
V _{OH}	HIGH-level output voltage; all outputs	V _I = V _{IH} or V _{IL} ; I _O = -50 µA	4.5	4.4	4.5	–	4.4	–	4.4	–	V
	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; I _O = -8.0 mA	4.5	3.94	–	–	3.8	–	3.70	–	V
V _{OL}	LOW-level output voltage; all outputs	V _I = V _{IH} or V _{IL} ; I _O = 50 µA	4.5	–	0	0.1	–	0.1	–	0.1	V
	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; I _O = 8 mA	4.5	–	–	0.36	–	0.44	–	0.55	V
I _I	input leakage current	V _I = V _{IH} or V _{IL}	5.5	–	–	0.1	–	1.0	–	2.0	µA
I _{oz}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND per input pin; other inputs at V _{CC} or GND; I _O = 0	5.5	–	–	±0.25	–	±2.5	–	±10.0	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	2.0	–	20	–	40	µA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = V _{CC} - 2.1 V other inputs at V _{CC} or GND; I _O = 0	4.5 to 5.5	–	–	1.35	–	1.5	–	1.5	mA
C _I	input capacitance		–	–	3	10	–	10	–	10	pF

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AC CHARACTERISTICS

Type 74AHC74

GND = 0 V; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)						UNIT	
		WAVEFORMS	C_L	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
$V_{CC} = 3.0$ to 3.6 V; note 1											
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n \bar{Q}	see Figs 6 and 8	15 pF	–	5.2	11.9	1.0	14.0	1.0	15.0	ns
	propagation delay n \bar{S}_D n \bar{R}_D to nQ, n \bar{Q}	see Figs 7 and 8		–	5.4	12.3	1.0	14.5	1.0	15.5	ns
f_{max}	maximum clock pulse frequency			80	125	–	45	–	45	–	ns
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n \bar{Q}	see Figs 6 and 8	50 pF	–	7.4	15.4	1.0	17.5	1.0	19.5	ns
	propagation delay n \bar{S}_D n \bar{R}_D to nQ, n \bar{Q}	see Figs 7 and 8		–	7.7	15.8	1.0	18.0	1.0	20.0	ns
t_W	clock pulse width HIGH or LOW	see Figs 6 and 8		6.0	–	–	7.0	–	7.0	–	ns
	set or reset pulse width LOW	see Figs 7 and 8	6.0	–	–	7.0	–	7.0	–	ns	
t_{rem}	removal time set or reset		5.0	–	–	5.0	–	5.0	–	ns	
t_{su}	set-up time nD to nCP	see Figs 6 and 8	6.0	–	–	7.0	–	7.0	–	ns	
t_h	hold time nD to nCP		0.5	–	–	0.5	–	0.5	–	ns	
f_{max}	maximum clock pulse frequency		50	75	–	70	–	70	–	ns	

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SYMBOL	PARAMETER	TEST CONDITIONS		T _{amb} (°C)						UNIT	
		WAVEFORMS	C _L	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
V_{CC} = 4.5 to 5.5 V; note 2											
t _{PHL} /t _{PLH}	propagation delay nCP to nQ, nQ̄	see Figs 6 and 8	15 pF	–	3.7	7.3	1.0	8.5	1.0	9.5	ns
	propagation delay nS _D nR _D to nQ, nQ̄	see Figs 7 and 8		–	3.7	7.7	1.0	9.0	1.0	10.0	ns
f _{max}	maximum clock pulse frequency			130	170	–	110	–	110	–	ns
t _{PHL} /t _{PLH}	propagation delay nCP to nQ, nQ̄	see Figs 6 and 8	50 pF	–	5.2	9.3	1.0	10.5	1.0	12.0	ns
	propagation delay nS _D to nQ, nQ̄	see Figs 7 and 8		–	5.3	9.7	1.0	11.0	1.0	12.5	ns
t _w	clock pulse width HIGH or LOW	see Figs 6 and 8		5.0	–	–	5.0	–	5.0	–	ns
	set or reset pulse width LOW	see Figs 7 and 8		5.0	–	–	5.0	–	5.0	–	ns
t _{rem}	removal time set or reset			3.0	–	–	3.0	–	3.0	–	ns
t _{su}	set-up time nD to nCP			5.0	–	–	5.0	–	5.0	–	ns
t _h	hold time nD to nCP			0.5	–	–	0.5	–	0.5	–	ns
f _{max}	maximum clock pulse frequency			90	115	–	75	–	75	–	ns

Notes

1. Typical values at V_{CC} = 3.3 V.
2. Typical values at V_{CC} = 5.0 V.

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Type 74AHCT74

GND = 0 V; $t_r = t_f \leq 3.0$ ns.

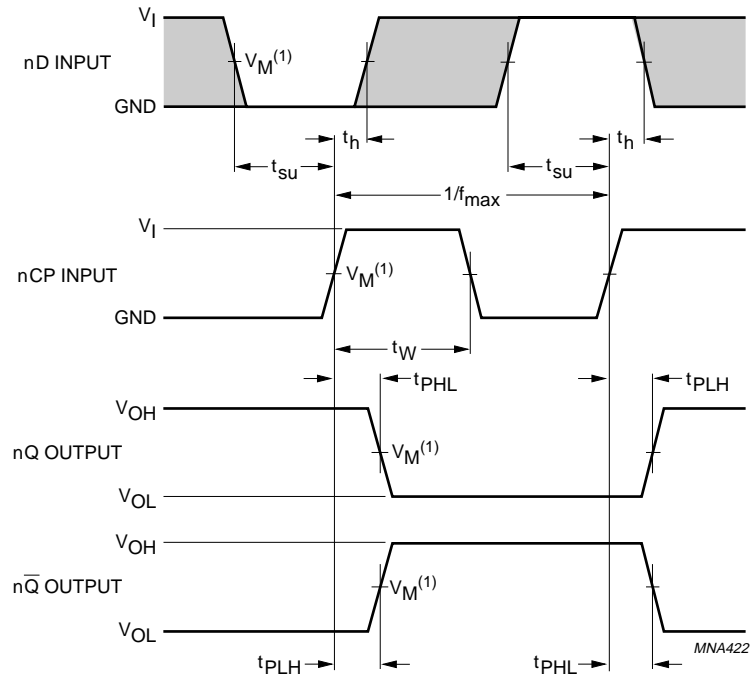
SYMBOL	PARAMETER	TEST CONDITIONS		T _{amb} (°C)						UNIT	
		WAVEFORMS	C _L	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
V_{CC} = 4.5 to 5.5 V; note 1											
t _{PHL} /t _{PLH}	propagation delay nCP to nQ, n \bar{Q}	see Figs 6 and 8	15 pF	–	3.3	7.8	1.0	9.0	1.0	10.0	ns
	propagation delay n \bar{S}_D n \bar{R}_D to nQ, n \bar{Q}	see Figs 7 and 8		–	3.7	10.4	1.0	12.0	1.0	13.0	ns
f _{max}	maximum clock pulse frequency			100	160	–	80	–	80	–	ns
t _{PHL} /t _{PLH}	propagation delay nCP to nQ, n \bar{Q}	see Figs 6 and 8	50 pF	–	4.8	8.8	1.0	10.0	1.0	11.0	ns
	propagation delay n \bar{S}_D n \bar{R}_D to nQ, n \bar{Q}	see Figs 7 and 8		–	5.3	11.4	1.0	13.0	1.0	14.5	ns
t _W	clock pulse width HIGH or LOW	see Figs 6 and 8		5.0	–	–	5.0	–	5.0	–	ns
t _{W(st)(rst)}	set or reset pulse width LOW	see Figs 7 and 8		5.0	–	–	5.0	–	5.0	–	ns
t _{rem}	removal time set or reset			3.5	–	–	3.5	–	3.5	–	ns
t _{su}	set-up time nD to nCP	see Figs 6 and 8		5.0	–	–	5.0	–	5.0	–	ns
t _h	hold time nD to nCP			0	–	–	0	–	0	–	ns
f _{max}	maximum clock pulse frequency			80	140	–	65	–	65	–	ns

Note1. Typical values at V_{CC} = 5.0 V.

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AC WAVEFORMS



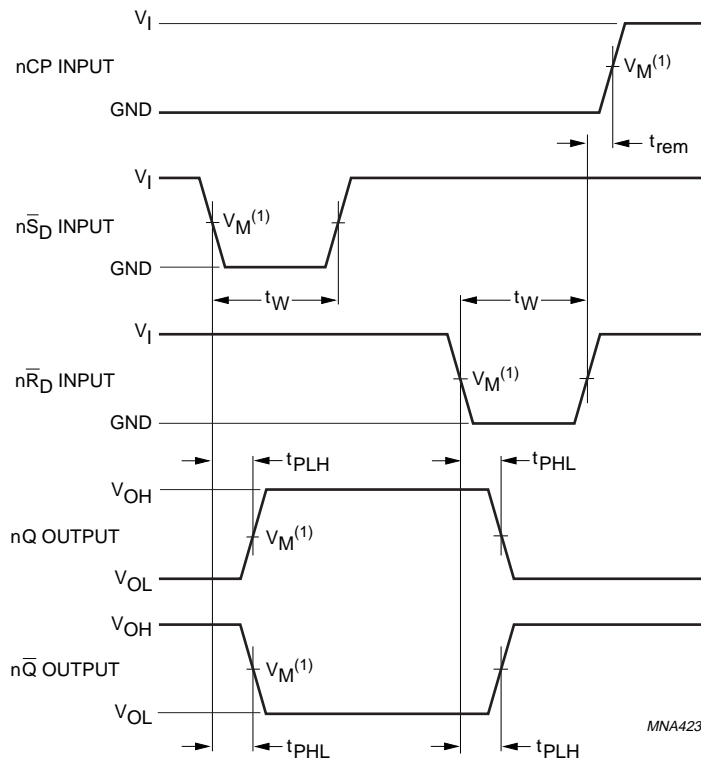
FAMILY	V _I INPUT REQUIREMENTS	V _M ⁽¹⁾ INPUT	V _M ⁽¹⁾ OUTPUT
AHC	GND to V _{CC}	50% V _{CC}	50% V _{CC}
AHCT	GND to 3.0 V	1.5 V	50% V _{CC}

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.6 The clock (nCP) to output (nQ, nQ-bar) propagation delays, the clock pulse width, the nD to nCP set-up, the nCP to nD hold times, the output transition times and the maximum clock pulse frequency.

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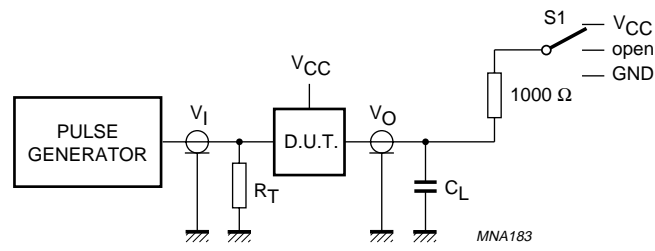


FAMILY	VI INPUT REQUIREMENTS	VM(1) INPUT	VM(1) OUTPUT
AHC	GND to VCC	50% VCC	50% VCC
AHCT	GND to 3.0 V	1.5 V	50% VCC

Fig.7 The set ($n\bar{S}_D$) and reset ($n\bar{R}_D$) input to output (nQ , $n\bar{Q}$) propagation delays, the set and reset pulse widths and the $n\bar{R}_D$ to nCP removal time.

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TEST	S ₁
t _{PLH} /t _{PHL}	open
t _{PLZ} /t _{PZL}	V _{CC}
t _{PHZ} /t _{PZH}	GND

Fig.8 Load circuitry for switching times.

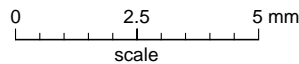
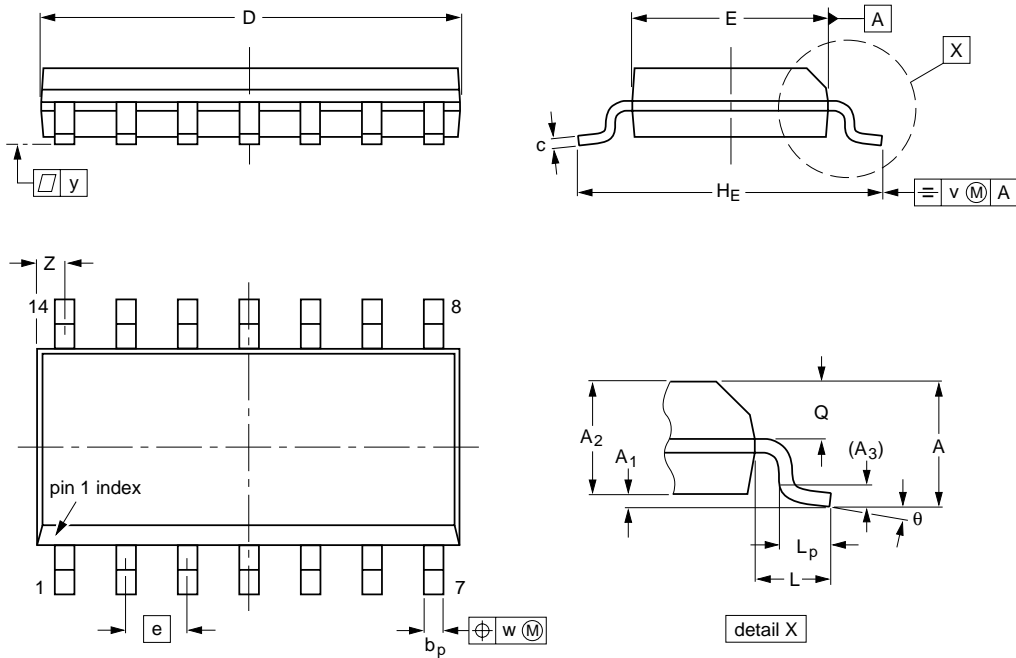
Dual D-type flip-flop with set and reset;
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PACKAGE OUTLINES

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

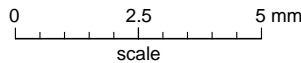
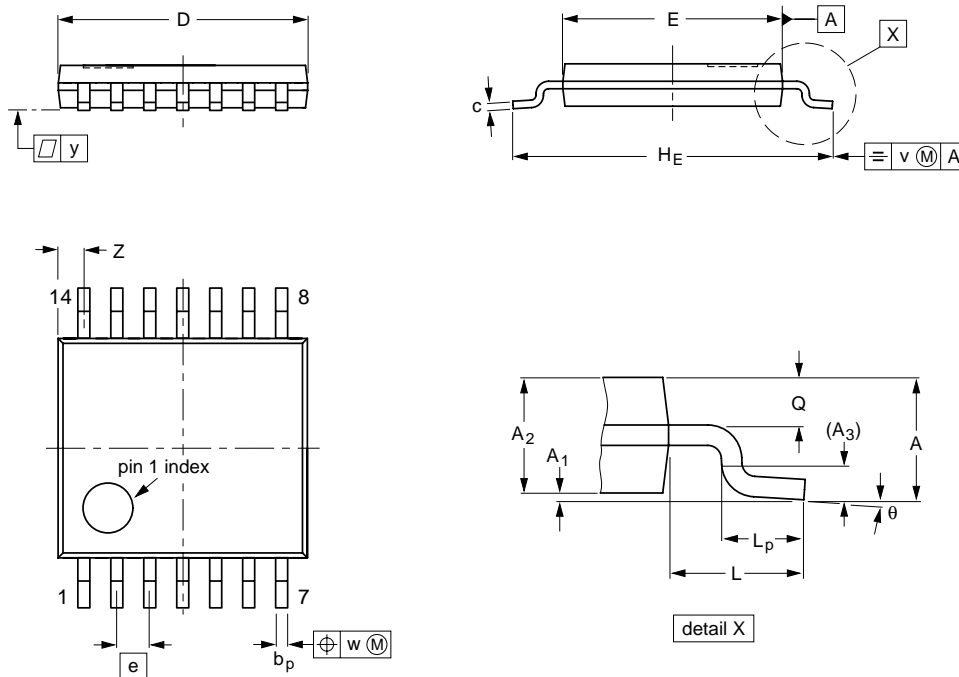
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
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SOT108-1	076E06S	MS-012AB			95-01-23 97-05-22

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				94-07-12- 95-04-04

Dual D-type flip-flop with set and reset; positive-edge trigger

74AHC74; 74AHCT74

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW ⁽¹⁾
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable ⁽²⁾	suitable
PLCC ⁽³⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽³⁾⁽⁴⁾	suitable
SSOP, TSSOP, VSO	not recommended ⁽⁵⁾	suitable

Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Dual D-type flip-flop with set and reset;
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NOTES

Dual D-type flip-flop with set and reset;
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