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NEC Electronics Inc.

μPD7527A/28A/75CG28E

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4-Bit, Single-Chip CMOS Microcomputers With FIP® Driver

Description

The μPD7527A, μPD7528A, and μPD75CG28E are 4-bit, single-chip CMOS microcomputers with the μPD7500 architecture and FIP direct-drive capability.

The μPD7527A contains a 2048 x 8-bit ROM and a 128 x 4-bit RAM. The μPD7528A contains a 4096 x 8-bit ROM and 160 x 4-bit RAM.

The μPD7527A/28A contains two 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater depth and flexibility. The μPD7527A/28A typically executes 67 instructions with a 5 μs instruction cycle time.

The μPD7527A/28A has one external and two internal edge-triggered hardware-vectorized interrupts. It also contains an 8-bit timer/event counter and an 8-bit serial interface to help reduce software requirements.

Thirty-one high-voltage lines are organized into the 3-bit output port 2, the 4-bit output ports 3, 8, and 9, and the 4-bit I/O ports 4, 5, 10, and 11.

The low power consumption CMOS process allows the use of a power supply between 2.7 and 6.0 V. Current consumption is less than 3.0 mA maximum, and can be further reduced in the halt and stop power-down modes.

The μPD75CG28E is a piggyback EPROM version of the μPD7527A/28A. Pin-compatible and function-compatible with the final, masked versions of the μPD7527A/28A, the μPD75CG28E is used for prototyping and for aiding in program development.

Features

- 67 instructions
- Instruction cycle:
 - Internal clock: 3.3 μs/600 kHz, 5 V
 - External clock: 3.3 μs/600 kHz, 5 V
- Upwardly compatible with the μPD7500 series product family
- 4,096 x 8-bit ROM (μPD7528A/75CG28E)
2,048 x 8-bit ROM (μPD7527A)
- 160 x 4-bit RAM (μPD7528A/75CG28E)
128 x 4-bit RAM (μPD7527A)
- 35 I/O lines
- 31 high-voltage output lines that can directly drive a vacuum fluorescent display (FIP)
- Can select either a pull-down resistor or open-drain output per 31 high-voltage outputs (mask optional)

- Vectored interrupts: one external, two internal
- 8-bit timer/event counter
- 8-bit serial interface
- Standby function (HALT, STOP)
- Data retention mode
- Zero-cross detector on P0₀/INT0 input (mask optional)
- System clock (μPD7527A/7528A/75CG28E): on-chip RC oscillator
- CMOS technology
- Low power consumption
- Single power supply
 - μPD7527A/7528A: 2.7 to 6.0 V
 - μPD75CG28E: 5.0 V

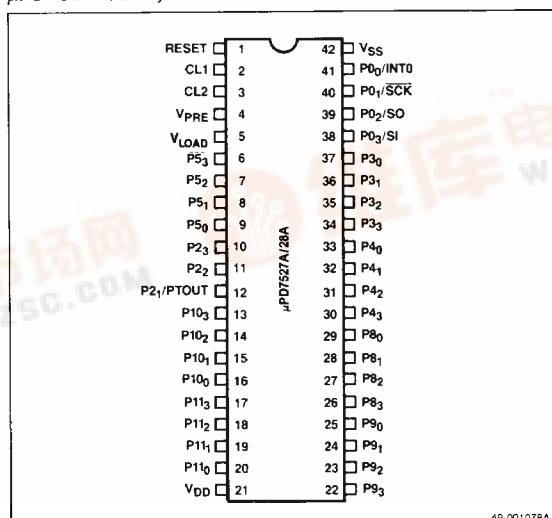
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Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD7527AC / 28AC	42-pin plastic DIP	610 kHz
μPD7527ACU / 28ACU	42-pin plastic shrink DIP	610 kHz
μPD75CG28E	42-pin ceramic piggyback DIP	500 kHz

Pin Configurations

μPD7527A/28A, 42-Pin Plastic DIP or Shrink DIP



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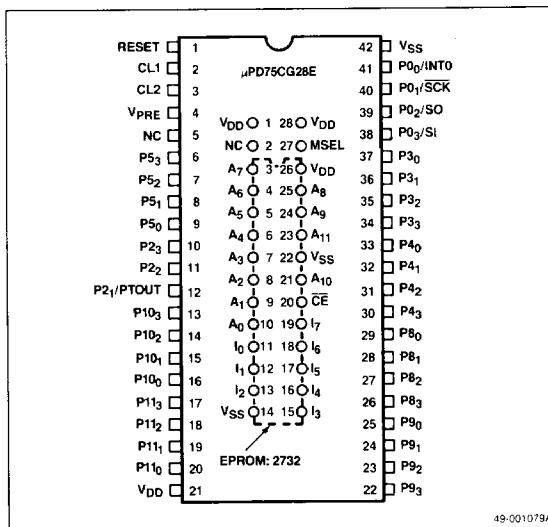
FIP is the registered trademark for NEC's fluorescent indicator panel (vacuum fluorescent display).

μPD7527A/28A/75CG28E

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Pin Configurations (cont)

μPD75CG28E, 42-Pin Ceramic Piggyback DIP



Pin Identification

μPD7527A/28A and μPD75CG28E

No.	Symbol	Function
1	RESET	Reset input
2, 3	CL1, CL2	Clock pins
4	V _{PRE}	High-voltage predriver supply
5	V _{LOAD}	High-voltage option resistor supply 7527A / 28A only
6-9	P5 ₀ -P5 ₃	High-voltage I/O port 5
10, 12	P2 ₃ , P2 ₂ , P2 ₁ /PTOUT	High-voltage output port 2, and output port from timer / event counter (PTOUT)
13-16	P10 ₀ -P10 ₃	High-current, high-voltage I/O port 10
17-20	P11 ₀ -P11 ₃	High-voltage, high-current I/O port 11
21	V _{DD}	Positive power supply
22-25	P9 ₀ -P9 ₃	High-voltage, high-current output port 9
26-29	P8 ₀ -P8 ₃	High-voltage, high-current output port 8
30-33	P4 ₀ -P4 ₃	High-voltage I/O port 4
34-37	P3 ₀ -P3 ₃	High-voltage output port 3
38	P0 ₃ /SI	4-bit input of port 0; or serial data input (SI), serial data output (SO), serial clock
39	P0 ₂ /SO	1/0 (SCK), and external interrupt input (INT0) or zero-cross detect input (P0 ₀)
40	P0 ₁ /SCK	
41	P0 ₀ /INT0	
42	V _{SS}	Ground

μPD75CG28E EPROM

No.	Symbol	Function
1	V _{DD}	Connection to pin 21 of μPD75CG28E
2	NC	No connection
3-10, 21, 24, 25	A ₀ -A ₁₀	EPROM address output
11-13, 15-19	I ₀ -I ₇	Data read input from the EPROM
14	V _{SS}	Connection to EPROM GND pin
20	CE	Chip enable output
22	V _{SS}	Supplies EPROM OE signal
23	A ₁₁	Program counter MSB output
26	V _{DD}	Supplies V _{CC} to the EPROM
27	MSEL	Mode select input
28	V _{DD}	Supplies high-level signal to MSEL

Note:

- (1) Output drivers on ports 2-5 and 8-11 are mask-optional. Accordingly, either an open-drain output or a pull-down resistor can be selected. V_{LOAD} is suitable for an output driver with a pull-down resistor.
- (2) Ports 2-5 are suitable as FIP segment signal outputs, and ports 8-11 are suitable for FIP digit signal outputs.
- (3) Ports 8-11 have high-current drive capability and can drive an LED directly.

Pin Functions, μPD7527A/28A and μPD75CG28E

RESET

System reset (input).

CL1, CL2

Connection to the RC oscillator. CL1 is the external clock input.

V_{PRE}

Negative power supply for high-voltage output pre-drivers (for ports 2-5, 8-11).

V_{LOAD}

Negative power supply for optional load resistors (pull-down resistors) of high-voltage output drivers (for ports 2-5, 8-11). This pin is only on the μPD7527A/28A.

P5₃-P5₀

4-bit, high-voltage I/O port 5.

P2₁-P2₃

3-bit, high-voltage output port 2.

PTOUT

Output port from the timer/event counter.

P10₃-P10₀

4-bit, high-voltage, high-current I/O port 10. Capable of bit set/reset by SPBL/RPBL instructions.

P11₃-P11₀

4-bit, high-voltage, high-current I/O port 11. Capable of bit set/reset by SPBL/RPBL instructions.

V_{DD}

Positive power supply.

P9₃-P9₀

4-bit, high-voltage, high-current output port 9. Capable of bit set/reset by SPBL/RPBL instructions.

P8₃-P8₀

4-bit, high-voltage, high-current output port 8. Capable of bit set/reset by SPBL/RPBL instructions.

P4₃-P4₀

4-bit, high-voltage I/O port 4.

P3₃-P3₀

4-bit, high-voltage output port 3.

P0₀-P0₃

4-bit input port 0. P0₀ is also used as the zero-cross detection input.

SI

Serial data input.

SO

Serial data output.

SCK

I/O serial clock.

INT0

External interrupt input.

V_{SS}

Ground.

Pin Functions, μPD75CG28E EPROM**MSEL**

Changes the addressing area of the external EPROM and the on-chip RAM (with a pull-down resistor). Connecting a jumper between socket pins 27 (MSEL) and 28 (V_{DD}) selects μPD7527A mode (2-Kbyte EPROM, 128 × 4-bit RAM). Leaving MSEL open selects μPD7528A mode (4-Kbyte EPROM, 160 × 4-bit RAM).

A₀-A₁₀

Output the low-order 11 bits of the program counter (PC₀-PC₁₀). Used as EPROM address signals.

A₁₁

When MSEL is high level, A₁₁ outputs high-level signals. When MSEL is open, A₁₁ outputs the MSB of the PC, which is used as the most significant address signal of the 4-Kbyte EPROM 2732.

I₀-I₇

Input data read from the EPROM.

CE

Outputs the chip enable signal to the EPROM.

V_{DD}

Pin 26 is electrically equivalent to the bottom V_{DD} pin and is used to supply V_{CC} to the EPROM. Pin 28 is electrically equivalent to the bottom V_{DD} pin and is used to supply the high level signal to MSEL. Pin 1 connects to pin 21 of μPD75CG28E.

V_{SS}

Pin 14 is electrically equivalent to the bottom V_{SS} pin in voltage, and is connected to the EPROM GND pin. Pin 22 is electrically equivalent to the bottom V_{SS} pin and is used to supply the OE signal to the EPROM.

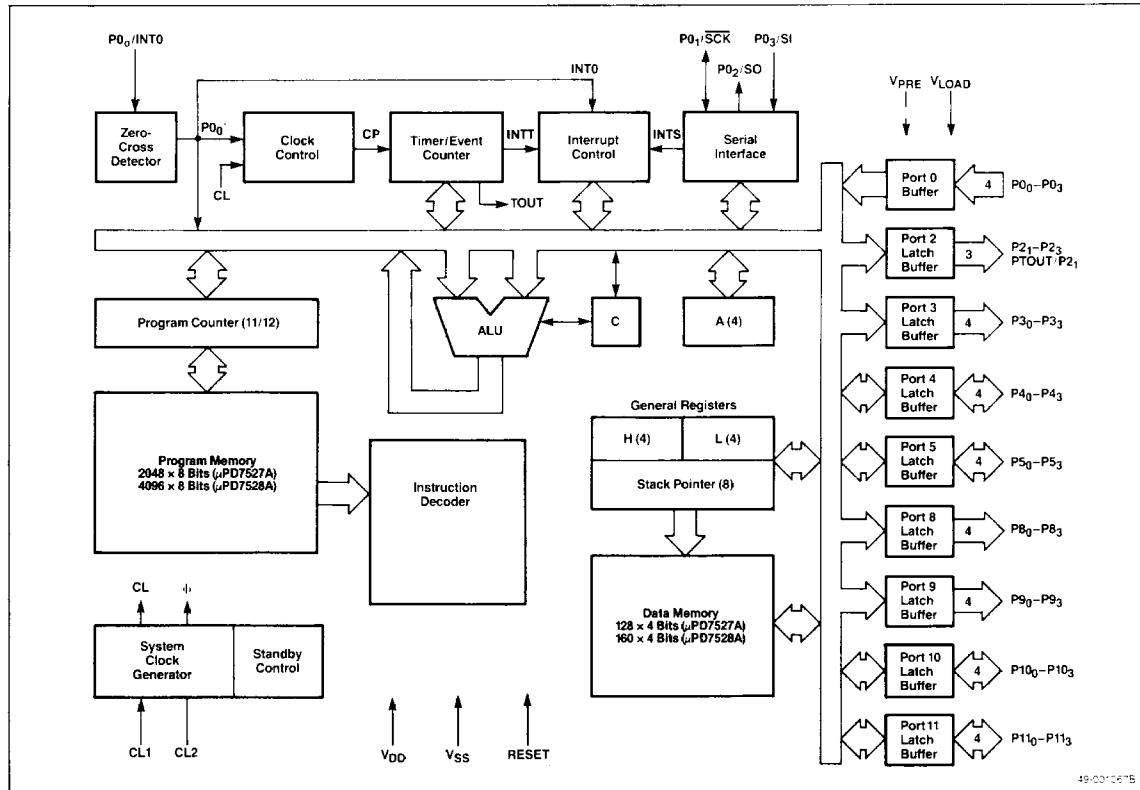
Instruction Set

Refer to the User's Manual. The instruction set appears also as subset A4 in the data sheet for the μPD7500 series of single-chip microcomputers.

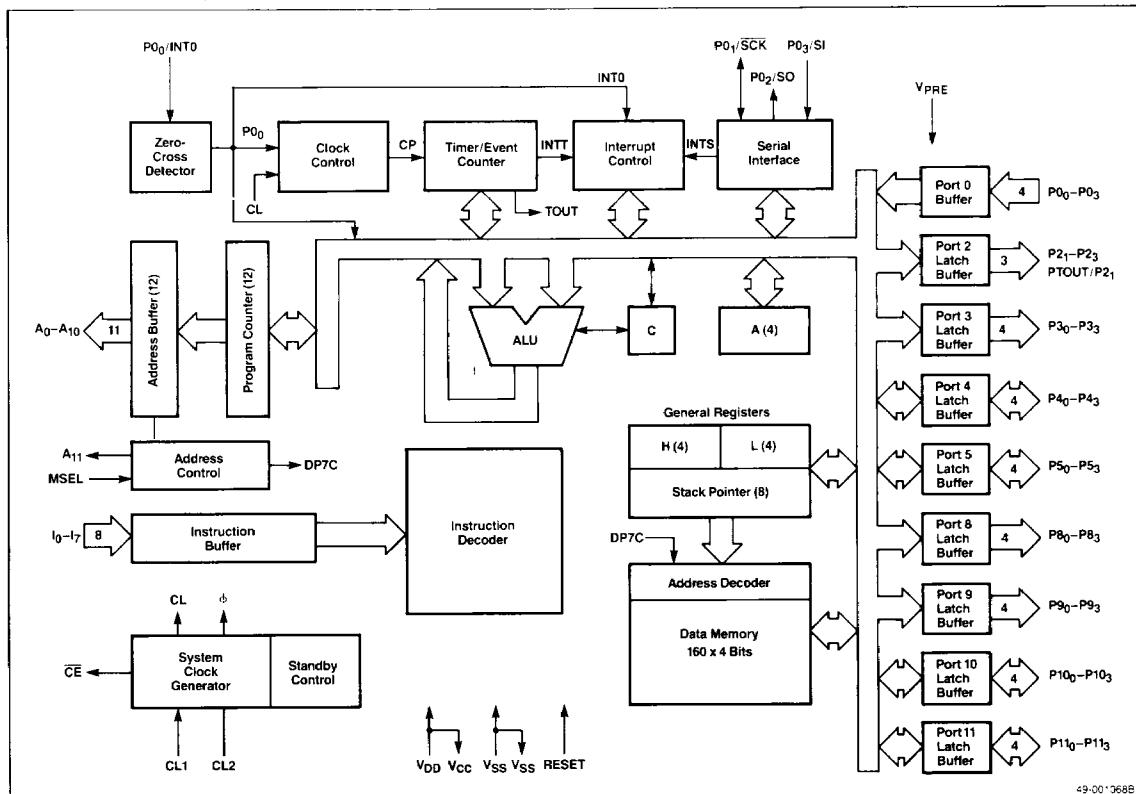
μ PD7527A/28A/75CG28E

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Block Diagram, μ PD7527A/28A



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Block Diagram, μPD75CG28E**Absolute Maximum Ratings** $T_A = 25^\circ\text{C}$

Power supply voltage, V_{DD}	-0.3 to $+7\text{ V}$	-55 mA
Power supply voltage, V_{LOAD} ($\mu\text{PD7527A} / 28\text{A}$)	$V_{DD} - 40\text{ V}$ to $V_{DD} + 0.3\text{ V}$	-55 mA
Power supply voltage, V_{PRE}	$V_{DD} - 12\text{ V}$ to $V_{DD} + 0.3\text{ V}$	15 mA
Input voltage, except ports 4, 5, 10, 11, V_{IN}	-0.3 V to $V_{DD} + 0.3\text{ V}$	15 mA
Input voltage, ports 4, 5, 10, 11, V_{IN}	$V_{DD} - 40\text{ V}$ to $V_{DD} + 0.3\text{ V}$	-10°C to $+70^\circ\text{C}$
Output voltage, except ports 2-5, 8-11, V_O	-0.3 V to $V_{DD} + 0.3\text{ V}$	-65°C to $+150^\circ\text{C}$
Output voltage, ports 2-5, 8-11, V_O	$V_{DD} - 40\text{ V}$ to $V_{DD} + 0.3\text{ V}$	
Output current high, per pin: P0 ₁ , P0 ₂ ; I_{OH}	-15 mA	
Output current high, per pin: ports 2-5, 8-11; I_{OH}	-30 mA	

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

μPD7527A/28A

T_A = -10°C to +70°C, V_{DD} = +2.7V to 6.0V

Parameter	Symbol	Limits			Test Conditions
		Min	Typ	Max	
Input voltage, low	V _{IL1}	0	0.3	V _{DD}	V Port 0, RESET
	V _{IL2}	0	0.5	V	CL1
	V _{IL3}	V _{DD} -35	0.3	V _{DD}	V Ports 4, 5, 10, 11
Input voltage, high	V _{IH1}	0.7	V _{DD}	V _{DD}	V Port 0, RESET
	V _{IH2}	V _{DD} -0.5	V _{DD}	V	CL1
	V _{IH3}	0.7	V _{DD}	V _{DD}	V Ports 4, 5, 10, 11; 4.5V ≤ V _{DD} ≤ 6.0V
		V _{DD} -0.5	V _{DD}	V	V Ports 4, 5, 10, 11; 2.7V ≤ V _{DD} ≤ 4.5V
Output voltage, low	V _{OL}	0.4	V	P0 ₁ , P0 ₂ ; 4.5V ≤ V _{DD} ≤ 6.0V; I _{OL} =1.6mA	
		0.5	V	P0 ₁ , P0 ₂ ; I _{OL} =400μA	
Output voltage, high	V _{OH}	V _{DD} -2.0	V	Ports 2-5, I _{OH} =-4mA (Note 1)	
		V _{DD} -2.0	V	Ports 8-11, I _{OH} =-10mA (Note 1)	
		V _{DD} -2.0	V	Ports 2-5, I _{OH} =-2mA (Note 2)	
		V _{DD} -2.0	V	Ports 8-11, I _{OH} =-5mA (Note 2)	
		V _{DD} -1.0	V	P0 ₁ , P0 ₂ ; I _{OH} =-1mA (Note 3)	
Input leakage current, low	I _{LIL1}	-3	μA	V _{IN} =0V; P0 ₀ -P0 ₃ (Note 4)	
	I _{LIL2}	-40	μA	V _{IN} =0V; P0 ₀ (Note 5)	
	I _{LIL3}	-10	μA	V _{IN} =0V; CL1	
	I _{LIL4}	-10	μA	V _{IN} =V _{DD} -35V; ports 4, 5, 10, 11	
Input leakage current, high	I _{LIH1}	3	μA	V _{IN} =V _{DD} ; P0 ₀ -P0 ₃ (Note 4)	
	I _{LIH2}	40	μA	V _{IN} =V _{DD} ; P0 ₀ (Note 5)	
	I _{LIH3}	10	μA	V _{IN} =V _{DD} ; CL1	
	I _{LIH4}	80	μA	V _{IN} =V _{DD} ; ports 4, 5, 10, 11	

Parameter	Symbol	Limits			Test Conditions
		Min	Typ	Max	
Output leakage current, low	I _{LOL1}			-3	μA V ₀ =0V; P0 ₁ , P0 ₂
	I _{LOL2}			-10	μA V ₀ =V _{DD} -35V; ports 2-5, 8-11
Output leakage current, high	I _{LOH1}			3	μA V ₀ =V _{DD} ; except ports 4, 5, 10, 11
	I _{LOH2}			80	μA V ₀ =V _{DD} ; ports 4, 5, 10, 11
Supply current, normal operation	I _{DD1}		1.0	3.0	mA V _{DD} =5V ± 10%, R=39kΩ
			0.4	1.0	mA V _{DD} =3V, R=82kΩ
Supply current, HALT mode (Note 6)	I _{DD2}		200	600	μA V _{DD} =5V ± 10%, R=39kΩ (Note 4)
			60	200	μA V _{DD} =3V, R=82kΩ (Note 4)
			210	640	μA V _{DD} =5V ± 10%, R=39kΩ (Note 5)
Supply current, STOP mode (Note 6)			67	230	μA V _{DD} =3V, R=82kΩ (Note 5)
	I _{DD3}		0.1	10	μA V _{DD} =3V (Note 4)
			10	40	μA V _{DD} =5V ± 10% (Note 5)
On-chip pull-down resistance	R _L	80	140	220	kΩ V _{DD} -V _{LOAD} =35V

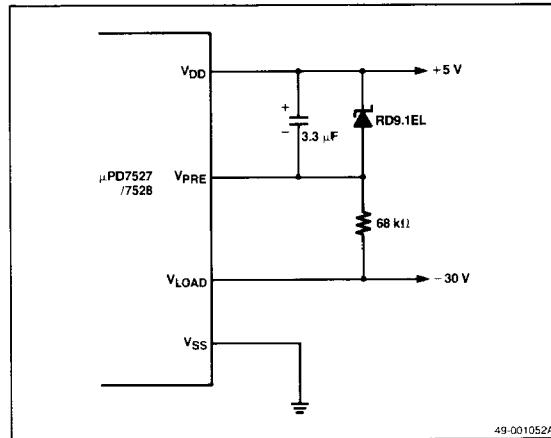
Note:

- (1) V_{PRE} = V_{DD}-9V ± 1V. The circuit in figure 5 is recommended.
- (2) V_{PRE} = 0V. V_{DD} = 4.5V to 6.0V.
- (3) V_{DD} = 4.5V to 6.0V.
- (4) Without zero-cross detector.
- (5) With zero-cross detector.
- (6) Ports 4, 5, 10, 11 are low level output or low level input.

DC Characteristics (cont)

 μ PD75CG28E $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = +5\text{ V} \pm 10\%$

Parameter	Symbol	Limits			Test Conditions
		Min	Typ	Max	
Input voltage, low	V_{IL1}	0	$0.3V_{DD}$	V	Port 0, RESET
	V_{IL2}	0	0.5	V	CL1
	V_{IL3}	$V_{DD}-35$	$0.3V_{DD}$	V	Ports 4, 5, 10, 11
Input voltage, high	V_{IH1}	$0.7V_{DD}$	V_{DD}	V	Port 0, RESET
	V_{IH2}	$V_{DD}-0.5$	V_{DD}	V	CL1
	V_{IH3}	$0.7V_{DD}$	V_{DD}	V	Ports 4, 5, 10, 11
Output voltage, low	V_{OL}	0.4	V	$P0_1, P0_2$; $I_{OL}=1.6\text{ mA}$	
		0.5	V	$P0_1, P0_2$; $I_{OL}=400\text{ }\mu\text{A}$	
Output voltage, high	V_{OH}	$V_{DD}-2.0$	V	Ports 2-5, $I_{OH}=-4\text{ mA}$ (1)	
		$V_{DD}-2.0$	V	Ports 8-11, $I_{OH}=-10\text{ mA}$ (1)	
		$V_{DD}-2.0$	V	Ports 2-5, $I_{OH}=-2\text{ mA}$ (2)	
		$V_{DD}-2.0$	V	Ports 8-11, $I_{OH}=-5\text{ mA}$ (2)	
		$V_{DD}-1.0$	V	$P0_1, P0_2$; $I_{OH}=-1\text{ mA}$	
Input current, low (I_{OL})	I_{IL}	-200	μA	$V_{IN}=0\text{ V}$	
Input current, high (MSEL)	I_{IH}	300	μA	$V_{IN}=V_{DD}$	

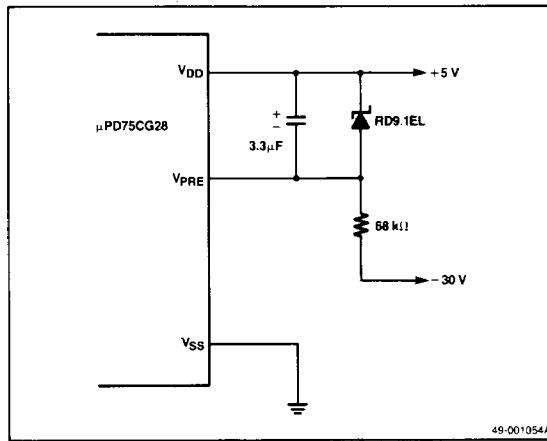
Figure 1. Recommended Circuit, μ PD7527A/7528A

Parameter	Symbol	Limits			Test Conditions
		Min	Typ	Max	
Input leakage current, low	I_{LIL1}	-3	μA	$V_{IN}=0\text{ V}; P0_0-P0_3$	
	I_{LIL2}	-40	μA	$V_{IN}=0\text{ V}; P0_0$	
	I_{LIL3}	-10	μA	$V_{IN}=0\text{ V}; CL1$	
	I_{LIL4}	-10	μA	$V_{IN}=V_{DD}-35\text{ V};$ ports 4, 5, 10, 11	
Input leakage current, high	I_{LIH1}	3	μA	$V_{IN}=V_{DD};$ $P0_0-P0_3$	
	I_{LIH2}	40	μA	$V_{IN}=V_{DD}; P0_0$	
	I_{LIH3}	10	μA	$V_{IN}=V_{DD}; CL1$	
	I_{LIH4}	80	μA	$V_{IN}=V_{DD};$ ports 4, 5, 10, 11	
Output leakage current, low	I_{LOL1}	-3	μA	$V_0=0\text{ V}; P0_1, P0_2$	
	I_{LOL2}	-10	μA	$V_0=V_{DD}-35\text{ V};$ ports 2-5, 8-11	
Output leakage current, high	I_{LOH1}	3	μA	$V_0=V_{DD};$ except ports 4, 5, 10, 11	
	I_{LOH2}	80	μA	$V_0=V_{DD};$ ports 4, 5, 10, 11	
Supply current, normal operation	I_{DP1}	1.0	3.0	mA	$R=39\text{ k}\Omega$
Supply current, HALT mode(3)	I_{DP2}	210	630	μA	$R=39\text{ k}\Omega$
Supply current, STOP mode(3)	I_{DP3}	10	50	μA	

Note:

(1) $V_{PRE}=V_{DD}-9\text{ V}+1\text{ V}$. The circuit in figure 6 is recommended.(2) $V_{PRE}=0\text{ V}$

(3) Ports 4, 5, 10, 11 are output off or low input.

Figure 2. Recommended Circuit, μ PD75CG28E

μPD7527A/28A/75CG28E

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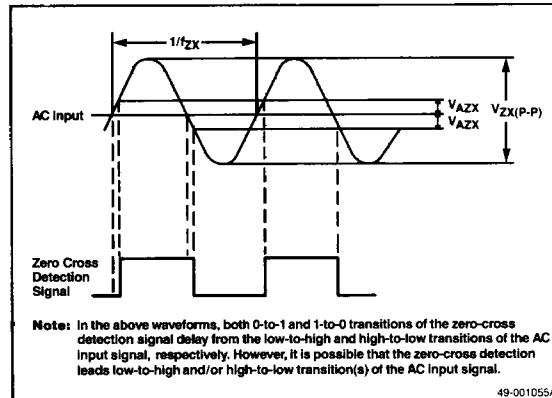
Zero-Cross Detection Characteristics

$\mu\text{PD7527A/28A}$: $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = 4.5\text{ V}$ to 6.0 V

$\mu\text{PD75CG28E}$: $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = +5\text{ V} \pm 10\%$

Parameter	Symbol	Limits				Test Conditions
		Min	Typ	Max	Unit	
Zero-cross detection input voltage	$V_{ZX(P-P)}$	1		3	$\text{V}_{\text{p-p}}$	AC coupled, $C = 0.1\text{ }\mu\text{F}$
Zero-cross accuracy	V_{AZX}		± 100	mV	50 Hz to 60 Hz sine wave	
Zero-cross detection input frequency	f_{ZX}	45		1000	Hz	

Zero-Cross Detection Waveform



Capacitance

$T_A = 25^\circ\text{C}$, $V_{DD} = 0\text{ V}$, $f = 1.0\text{ MHz}$, Unmeasured pins returned to GND

Parameter	Symbol	Limits				Test Conditions
		Min	Typ	Max	Unit	
Input capacitance	C_I		15	pF	P_{0_0}, P_{0_3}	
Output capacitance	C_O		15	pF	Port 2	
			35	pF	Ports 3, 8, 9	
I/O capacitance	C_{IO}		15	pF	P_{0_1}, P_{0_2}	
			35	pF	Ports 4, 5, 10, 11	

AC Characteristics

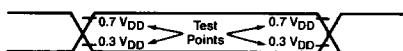
$\mu\text{PD7527A/28A}$

$T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = +2.7\text{ V}$ to 6.0 V

Parameter	Symbol	Limits				Test Conditions
		Min	Typ	Max	Unit	
Cycle time (Note 1)	t_{CY}	3.3		200	μs	$V_{DD} = 4.5\text{ V}$ to 6.0 V
		6.9		200	μs	
P_{0_0} event input frequency	f_{P0}	0		610	kHz	$V_{DD} = 4.5\text{ V}$ to 6.0 V
		0		290	kHz	
P_{0_0} input rise time	t_{POR}				0.1	μs
P_{0_0} input fall time	t_{POF}				0.1	μs
P_{0_0} input pulse width, low	t_{POL}		1.63		μs	
P_{0_0} input pulse width, high	t_{POH}		0.72		μs	$V_{DD} = 4.5\text{ V}$ to 6.0 V
SCK cycle time	t_{KCY}	3.0			μs	Input; $V_{DD} = 4.5\text{ V}$ to 6.0 V
		3.3			μs	Output; $V_{DD} = 4.5\text{ V}$ to 6.0 V
		6.9			μs	Input
		8.0			μs	Output
SCK pulse width, low	t_{KL}	3.35			μs	Input
		3.9			μs	Output
SCK pulse width, high	t_{KH}	1.4			μs	Input; $V_{DD} = 4.5\text{ V}$ to 6.0 V
		1.55			μs	Output; $V_{DD} = 4.5\text{ V}$ to 6.0 V
SI set-up time (to rising-edge of SCK)	t_{SIK}	300				ns
SI hold time (after rising-edge of SCK)	t_{KSI}	450				ns
SO output delay time (after falling-edge of SCK)	t_{KS0}			850	ns	$V_{DD} = 4.5\text{ V}$ to 6.0 V
				1200	ns	
INTO pulse width, high, low	t_{IOH}	10			μs	
	t_{IOL}					
RESET pulse width, high, low	t_{RSH}	10			μs	
	t_{RSL}					

AC Characteristics (cont)**μPD75CG28E** $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = +5\text{ V} \pm 10\%$

Parameter	Symbol	Limits				Test Conditions
		Min	Typ	Max	Unit	
Cycle time (Note 1)	t_{CY}	4.0		200	μs	
P0 ₀ event input frequency	f_{P0}	0		500	kHz	
P0 ₀ input rise time	t_{POR}			0.2	μs	
P0 ₀ input fall time	t_{POF}			0.2	μs	
P0 ₀ input pulse width, high, low	t_{POH}, t_{POL}	0.8			μs	
SCK cycle time	t_{KCY}	3.0			μs	Input
		4.0			μs	Output
SCK pulse width, low	t_{KL}	1.8			μs	Output
SCK pulse width, high	t_{KH}	1.3			μs	Input
SI set-up time (to rising-edge of SCK)	t_{SIK}	300			ns	
SI hold time (after rising-edge of SCK)	t_{KSI}	450			ns	
SO output delay time (after falling-edge of SCK)	t_{KSO}		850		ns	
INTO pulse width, high, low	t_{IOH}, t_{IOL}	10			μs	
RESET pulse width, high, low	t_{RSH}, t_{RSL}	10			μs	
Data input delay time from address	t_{ACC}		700		ns	
Data input delay time from \overline{CE}	t_{CE}		700		ns	
Input hold time after address	t_{IH}	0			ns	

Note:(1) $t_{CY} = 2/f_{CC}$ or $2/f_C$ **AC Waveform Measurement Points (Except CL1)**

49-001056A

Oscillation Characteristics**μPD7527A/28A** $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = 2.7\text{ V}$ to 6.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
System clock oscillation frequency (Note 1)	f_{CC}	300	400	500	kHz	$R = 39\text{ k}\Omega \pm 2\%$ $V_{DD} = 4.5\text{ V}$ to 6.0 V
System clock CL1 input frequency (Note 2)	f_C	10		610	kHz	$V_{DD} = 4.5\text{ V}$ to 6.0 V
CL1 input rise time (Note 2)	t_{CR}			0.1	μs	
CL1 input fall time (Note 2)	t_{CF}			0.1	μs	
CL1 input pulse width, low (Note 2)	t_{CL}	0.7		50	μs	
CL1 input pulse width, high (Note 2)	t_{CH}	1.63		50	μs	$V_{DD} = 4.5\text{ V}$ to 6.0 V

μPD75CG28E $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = 5\text{ V} \pm 10\%$

Parameter	Symbol	Limits				Test Conditions
		Min	Typ	Max	Unit	
System clock oscillation frequency (Note 1)	f_{CC}	300	400	500	kHz	$R = 39\text{ k}\Omega \pm 2\%$
		110	150	190	kHz	$R = 110\text{ k}\Omega \pm 2\%$
System clock CL1 input frequency (Note 2)	f_C	10		500	kHz	
CL1 input rise time (Note 2)	t_{CR}		0.2		μs	
CL1 input fall time (Note 2)	t_{CF}		0.2		μs	
CL1 input pulse width, high, low	t_{CH}, t_{CL}	0.8		50	μs	

Note:

(1) R, C (see figure 3). (2) External clock (see figure 4).

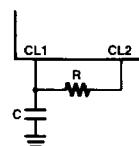
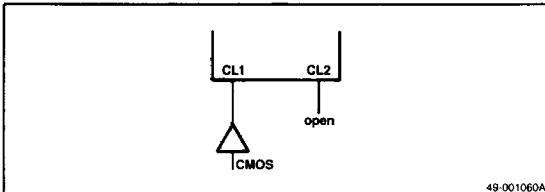
Figure 3. Recommended RC Oscillator Circuit $C = 33\text{ pF} \pm 5\%$ $|\Delta C| \leq 60\text{ ppm}/^\circ\text{C}$

Figure 4. Recommended External Clock Circuit



Stop Mode Low Voltage Data Retention Characteristics

μPD7527A/28A

T_A = -10°C to +70°C

Parameter	Symbol	Limits			Test Conditions
		Min	Typ	Max	
Data retention supply voltage	V _{DDDR}	2.0		6.0	V
Data retention supply current	I _{DDDR}	0.3	10	μA	V _{DDDR} =2V (Note 1)
		7	30	μA	V _{DDDR} =2V (Note 2)
Data retention RESET input voltage high	V _{IHDR}	0.9 V _{DDDR}		V _{DDDR} +0.2	V
RESET set-up time	t _{SRS}	0			μs
RESET hold time	t _{HRS}	0			μs

μPD75CG28E

T_A = -10°C to +70°C

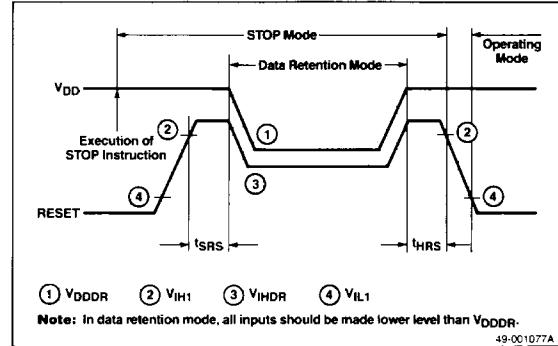
Parameter	Symbol	Limits			Test Conditions
		Min	Typ	Max	
Data retention supply voltage	V _{DDDR}	2.0		5.5	V
Data retention supply current	I _{DDDR}	7	30	μA	V _{DDDR} =2V
Data retention RESET input voltage high	V _{IHDR}	0.9 V _{DDDR}		V _{DDDR} +0.2	V
RESET set-up time	t _{SRS}	0			μs
RESET hold time	t _{HRS}	0			μs

Note:

(1) Without zero-cross detector

(2) With zero-cross detector

Data Retention Mode Timing



μPD75CG28E EPROM Interface

A 4-Kbyte EPROM (2732) plugs into socket pins on top of the μPD75CG28E. A high input to MSEL selects μPD7527A mode and fixes the A₁₁ output high level in order to access the upper 2-Kbytes of the 4-Kbyte EPROM. When MSEL is open, μPD7528A mode is selected. All EPROM addresses can be accessed because A₁₁ functions as the MSB of the address. Figure 5 shows the address control unit. Figures 6 and 7 show the μPD75CG28E connected with the 2732.

Figure 8 shows the EPROM read timing. Data is read into the instruction buffer at the end of the T4 state. The chip enable (CE) signal is made active during 2 states (T3, T4) in order to decrease the power consumption of the EPROM.

Figure 5. Address Control Unit

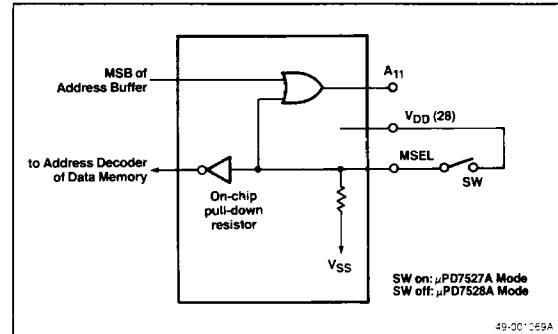


Figure 6. Connection with the 2732 (μ PD7527A Mode)

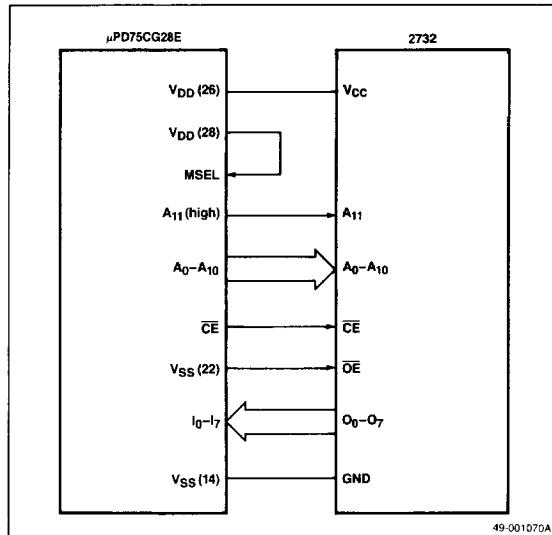
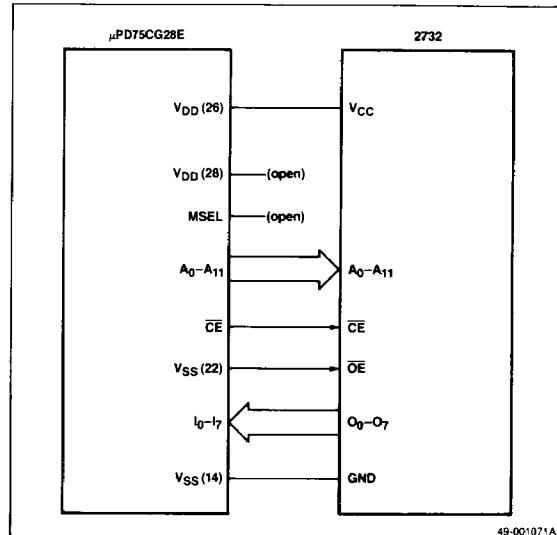
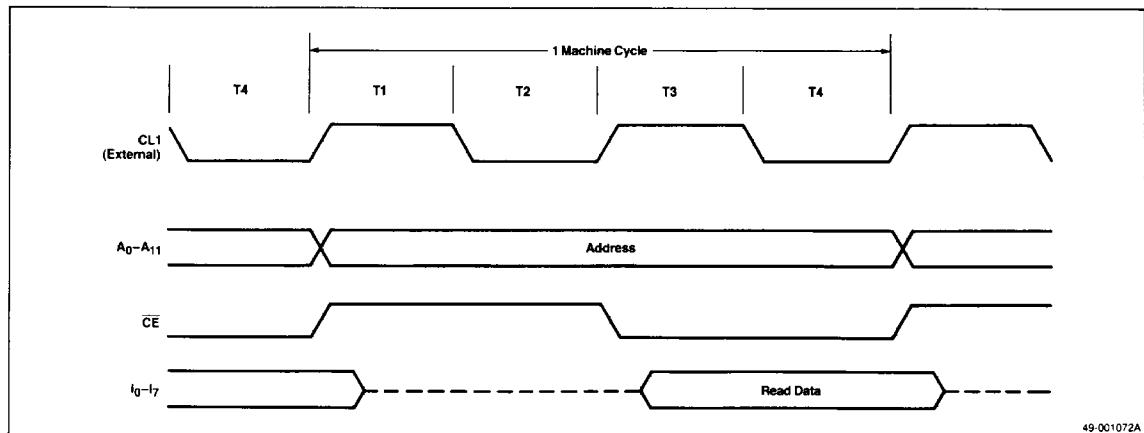


Figure 7. Connection with the 2732 (μ PD7528A Mode)



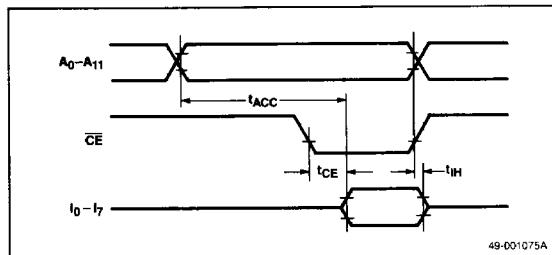
3

Figure 8. EPROM Read Timing

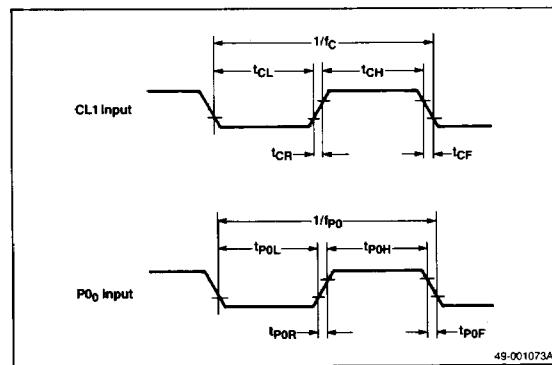


Timing Waveforms

EPROM (μPD75CG28E only)



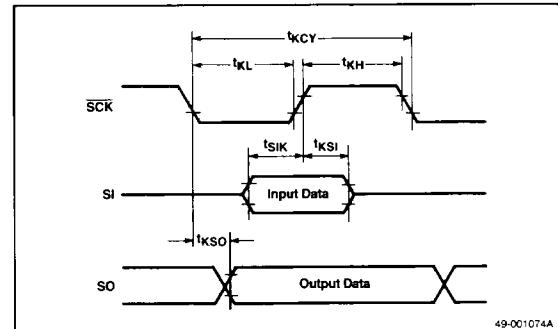
Clock



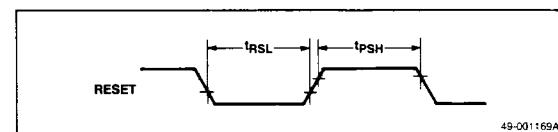
**Differences Among the
μPD7527A/28A/CQ28E**

	μPD75CG28E	μPD7527A	μPD7528A
Program memory	4 Kbyte EPROM (2732) connectable on top	On-chip 2 Kbyte ROM	On-chip 4 Kbyte ROM
Data memory (RAM)	160 × 4	128 × 4	160 × 4
High-voltage output lines	All open-drain outputs	On-chip load capacitor or open drain output (bit by bit, mask optional)	
V _{LOAD} pin	No		
Zero-cross detection	Yes	Mask optional	
Package	42-pin ceramic piggyback DIP bottom pin compatible with μPD7527A / 28A	42-pin plastic DIP 42-pin plastic shrink DIP	
Power supply	5 V	2.7 V to 6.0 V	

Serial Interface



Interrupt Input



Reset Input

