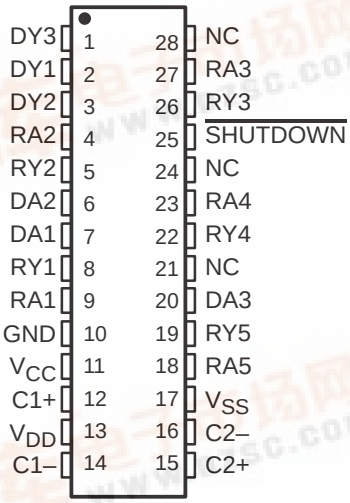
SN75LBC187
MULTICHANNEL EIA-232 DRIVER/RECEIVER WITH CHARGE PUMP

SLLS130C – SEPTEMBER 1991 – REVISED MAY 1995

- **Single IC and Single 5-V Supply Interface for Serial Communication Ports**
- **Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-232-E-1991, EIA/TIA-562, and ITU Recommendation V.28**
- **Switched-Capacitor Voltage Converter Eliminates Need for ±12-V Supplies**
- **Voltage Converter Operates With Low Capacitance . . . 0.1 μF Min**
- **Designed for Data Rates up to 120 kb/s Over 3-m Cable**
- **Available in Shrink Small-Outline 25-mil-Pitch Package**
- **Shutdown Mode to Save Power When Not in Use**
- **±30-V Receiver Input Voltage Range**
- **LinBiCMOS™ Process Technology**
- **Applications**
  - **Laptop or Notebook Computers**
  - **Portable Terminals**
  - **Single-Board Computers**
  - **Portable Test Equipment**

DB PACKAGE
(TOP VIEW)



NC – No internal connection

description

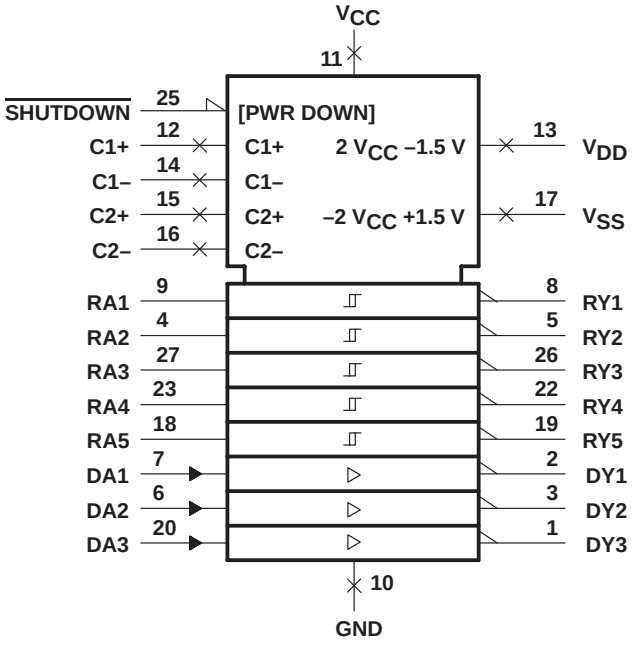
The SN75LBC187 is a low-power LinBiCMOS™ device containing three drivers, five receivers, and a switched-capacitor voltage converter. The SN75LBC187 provides a single chip and single 5-V supply interface between the asynchronous communications element and the serial port connector of the data terminal equipment (DTE). This device has been designed to conform to ANSI Standards EIA/TIA-232-E, EIA/TIA-562, and ITU recommendation V.28.

The switched-capacitor voltage converter of the SN75LBC187 uses four small external capacitors to generate the positive and negative voltages required by EIA/TIA-232-E (and V.28) line drivers from a single 5-V input. The drivers feature output slew-rate limiting to eliminate the need for external filter capacitors. The receivers can accept ±30 V without damage. The device also features a reduced power or shutdown mode that cuts the quiescent power to the IC when not transmitting data between the CPU and peripheral.

The SN75LBC187 has been designed using LinBiCMOS™ technology and cells contained in the Texas Instruments LinASIC™ library. The SN75LBC187 is characterized for operation from 0°C to 70°C.

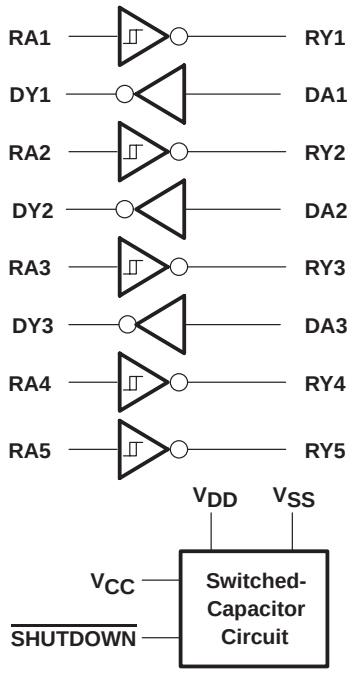
NOTE:
This device includes circuit designs and process technologies that have patents pending.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) . . . . . 0.3 V to 6 V
Positive output supply voltage range, V_{DD} . . . . . V_{CC} –0.3 V to 15 V
Negative output supply voltage range, V_{SS} . . . . . 0.3 V to –15 V
Input voltage range, V_I: RA . . . . . ±30 V
All other inputs . . . . . –0.3 V to V_{CC} + 3 V
Output voltage range, V_O: DY . . . . . –2 V_{CC} + 1.2 V to 2 V_{CC} – 1.2 V
All other outputs . . . . . –0.3 V to V_{CC} + 3 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DB	1025 mW	8.2 mW/°C	656 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}	DA	2			V
	RA, $\overline{\text{SHUTDOWN}}$	2.4			
Low-level input voltage, V_{IL}	RA, DA, $\overline{\text{SHUTDOWN}}$			0.8	V
Receiver input voltage, V_I		–25		25	V
High-level output current, I_{OH}	RY			–1	mA
Low-level output current, I_{OL}	RY			3.2	mA
Output current, I_O	V_{DD}			±10	µA
	V_{SS}			±10	µA
C1, C2, C3, C4 charge pump capacitors		0.1	0.47		µF
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	Receiver	I_O = –1 mA		3.5			V
		Driver	R_L = 3 kΩ to GND		5	7		
V_{OL}	Low-level output voltage	Receiver	I_O = 3.2 mA				0.4	V
		Driver	R_L = 3 kΩ to GND			–7	–5	
V_{IT+}	Receiver positive-going input voltage threshold					1.7	2.4	V
$V_{IT–}$	Receiver negative-going input voltage threshold				0.8	1.2		V
V_{hys}	Receiver input hysteresis voltage ($V_{IT+} – V_{IT–}$)					0.5	1	V
r_i	Receiver input resistance		V_{CC} = 5 V,	T_A = 25°C	3	5	7	kΩ
r_o	Driver output resistance		V_{CC} = 0,	V_O = ±2 V	300			Ω
I_I	Input current (DA, $\overline{\text{SHUTDOWN}}$)		V_I = 0 to V_{CC}				±50	µA
I_{OS}	Driver output short-circuit current		V_O = 0		±10			mA
I_{CC}	Supply current	Normal operation	All outputs open, $\overline{\text{SHUTDOWN}}$ at 2.4 V			15	30	mA
		Shutdown mode	All outputs open, $\overline{\text{SHUTDOWN}}$ at 0.1 V				10	µA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

switching characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Receiver	R_L = 5 kΩ, See Figure 1	C_L = 50 pF,		1.25	µs
		Driver	R_L = 3 kΩ, See Figure 2	C_L = 1200 pF,		1.25	µs
t_{PHL}	Propagation delay time, high- to low-level output	Receiver	R_L = 5 kΩ, See Figure 1	C_L = 50 pF,		1.25	µs
		Driver	R_L = 3 kΩ, See Figure 2	C_L = 1200 pF,		1.25	µs
t_r	Rise time, driver output		R_L = 3 kΩ, V_O = –3 V to 3 V,	C_L = 50 pF, See Note 2	200		ns
			R_L = 3 kΩ, V_O = –3.3 V to 3.3 V,	C_L = 2500 pF, See Note 3		1.5	µs
t_f	Fall time, driver output		R_L = 3 kΩ, V_O = 3 V to –3 V	C_L = 50 pF,	200		ns
			R_L = 3 kΩ, V_O = 3.3 V to –3.3 V	C_L = 2500 pF,		1.5	µs

NOTES: 2. The 200 ns for the output to change from –3 V to 3 V (or vice versa) corresponds to the 30 V/µs maximum slew rate of EIA/TIA-232-E, EIA/TIA-562, and ITU Recommendation V.28.

3. The more stringent requirement for transition times comes from the EIA/TIA-562, which requires the rise and fall times to be measured from 3.3 V.

PARAMETER MEASUREMENT INFORMATION

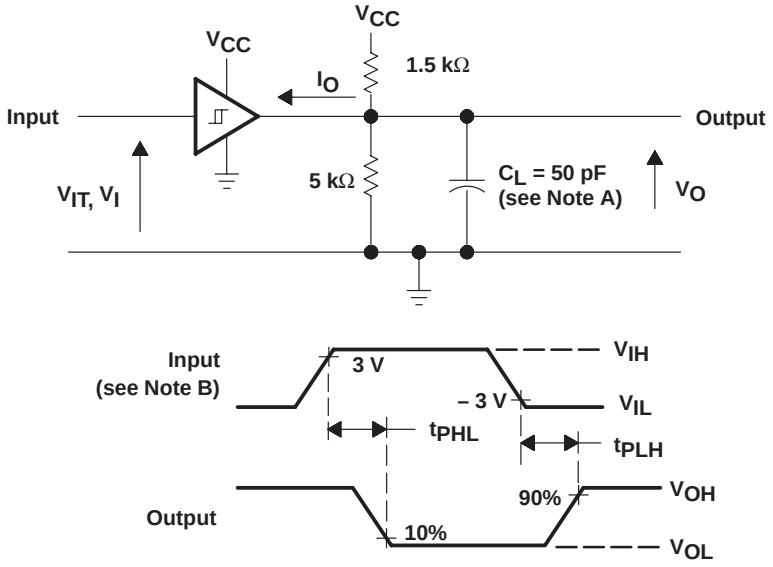
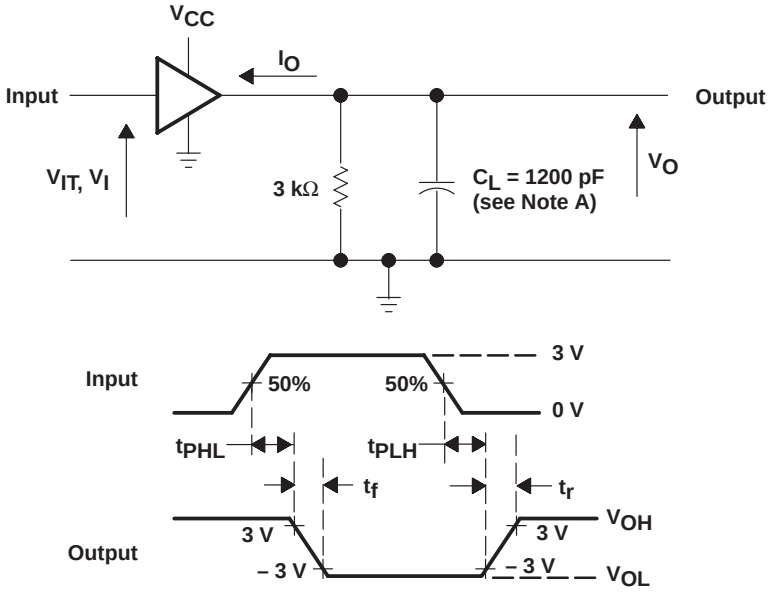


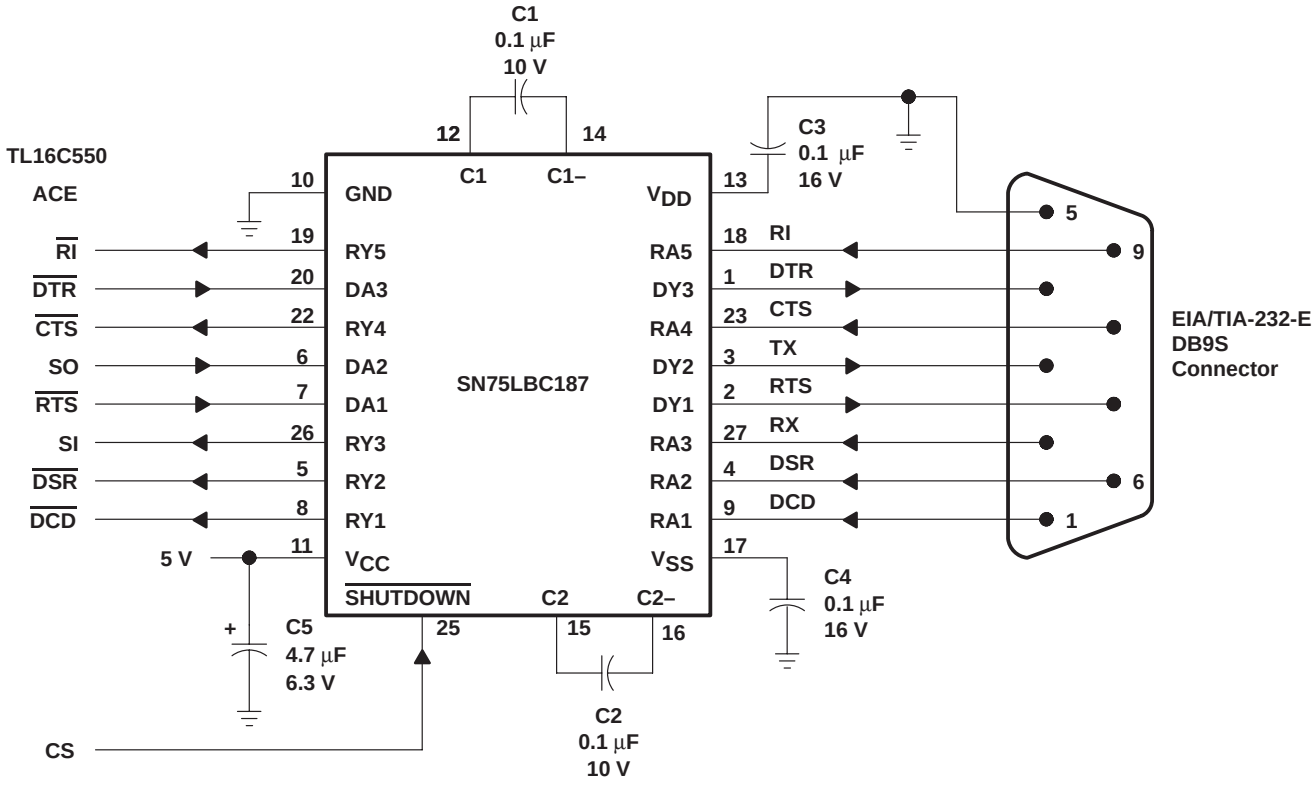
Figure 1. Receiver Test Circuit and Waveforms



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: t_w = 8.33 µs, PRR = 60 kHz, $t_r = t_f \leq 50$ ns.

Figure 2. Driver Test Circuit and Waveforms

APPLICATION INFORMATION



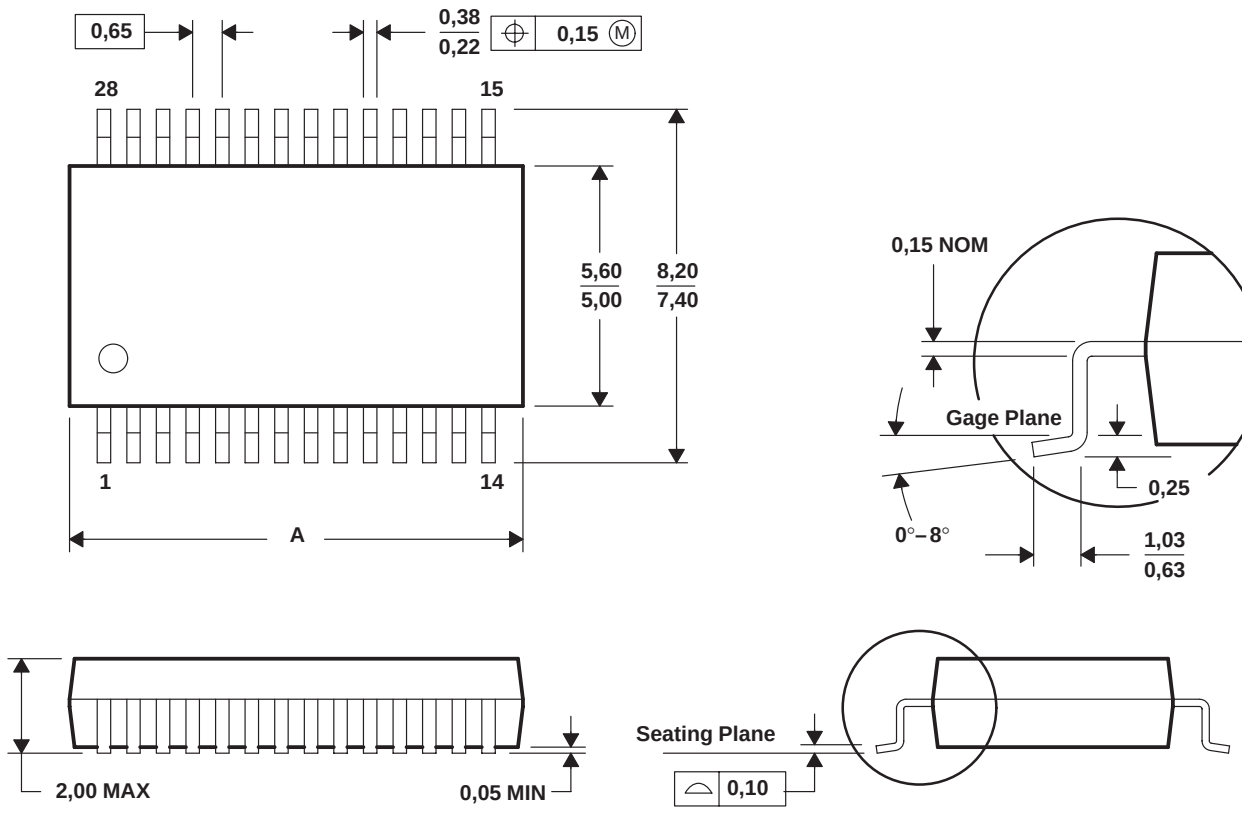
NOTE: C1, C2, C3, and C4 are Z5U-type ceramic-chip capacitors.

Figure 3. Typical SN75LBC187 Connection

MECHANICAL DATA

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

28 PIN SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 / D 02/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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