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Ordering number : EN5691

CMOS LSI

LC7851E

QPSK Demodulation and Audio Signal-Processing IC for Satellite Broadcast Reception

Overview

The LC7851E demodulates the QPSK (quadrature phase shift keying) modulated audio data broadcast by the Japanese BS and CS broadcast satellites and converts that data to an analog audio signal. This IC integrates on a single chip the audio system signal processing required for BS and CS receivers from QPSK demodulation to analog audio reproduction. The main functions provided by the LC7851E include QPSK demodulation, differential decoding conversion, descrambling, deinterleaving, and error correction. It also generates a PCM audio signal. The PCM audio signal is converted to an analog audio signal by on-chip digital filters and A/D converters.

Features

- QPSK demodulator, PCM decoder, digital filters, D/A converters, and operational amplifiers integrated on a single chip.
- The number of required external components has been reduced and adjustment-free operation achieved in the QPSK demodulator by implementing that block as a digital circuit on a single chip.
- CPU interface using an I²C bus
- Interface circuits for CORTEC and SkyPort descramblers

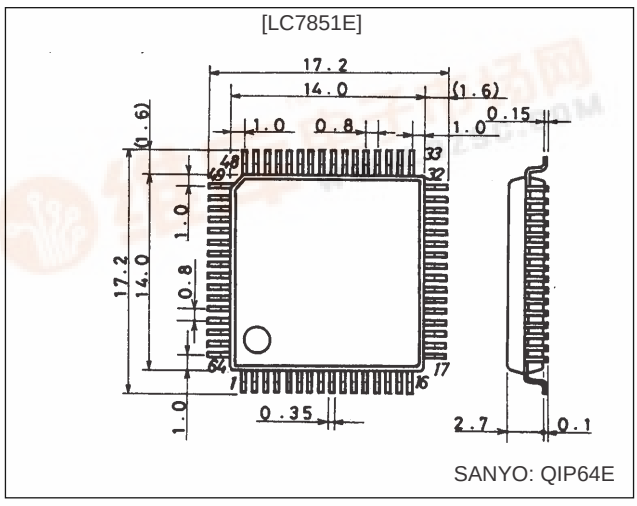
Functions

- QPSK demodulation
- Bit timing clock recovery
- Differential decoding conversion and parallel-to-serial conversion
- Frame synchronization (forward protection: 8 cycles, back protection: 3 cycles): Frame synchronized/not synchronized detection flag output provided.
- Tenth-order M-series descrambling
- Deinterleaving
- BCH (63, 56) error correction and dual error detection: Single error detected flag output provided.
- Support for both interpolation and previous data hold when a dual error is detected.
  Control bit majority judgment protection every 16 frames
- Register data previous value hold when dual errors are detected using BCH(7,3)
- Ten to 14 bit expansion of audio data during A mode broadcasts.
- Data protection using majority control for the upper bits of the audio data during B mode broadcasts
- Full complement of muting functions
  - — Audio suppression provided (bit 16 of the post-majority decision control bits)
  - — Non-audio signal suppression (bits 2 to 5 of the post-majority decision control bits)
  - — Forced muting
  - — Muting when not synchronized
  - — Muting when large numbers of errors are detected (modifiable conditions)
  - — Channel switching
  - — Charged (pay-per-view) program flag muting
  - — Mute detection output provided.
- General-purpose ports (2 input ports and 8 output ports)
- EIAJ digital audio interface output
- 8× oversampling digital filters
- Multi-bit D/A converter (with built-in output operational amplifiers)
- 5 V single-voltage power supply
- QFP (QIP) 64E package

Package Dimensions

unit: mm

3195-QFP64E



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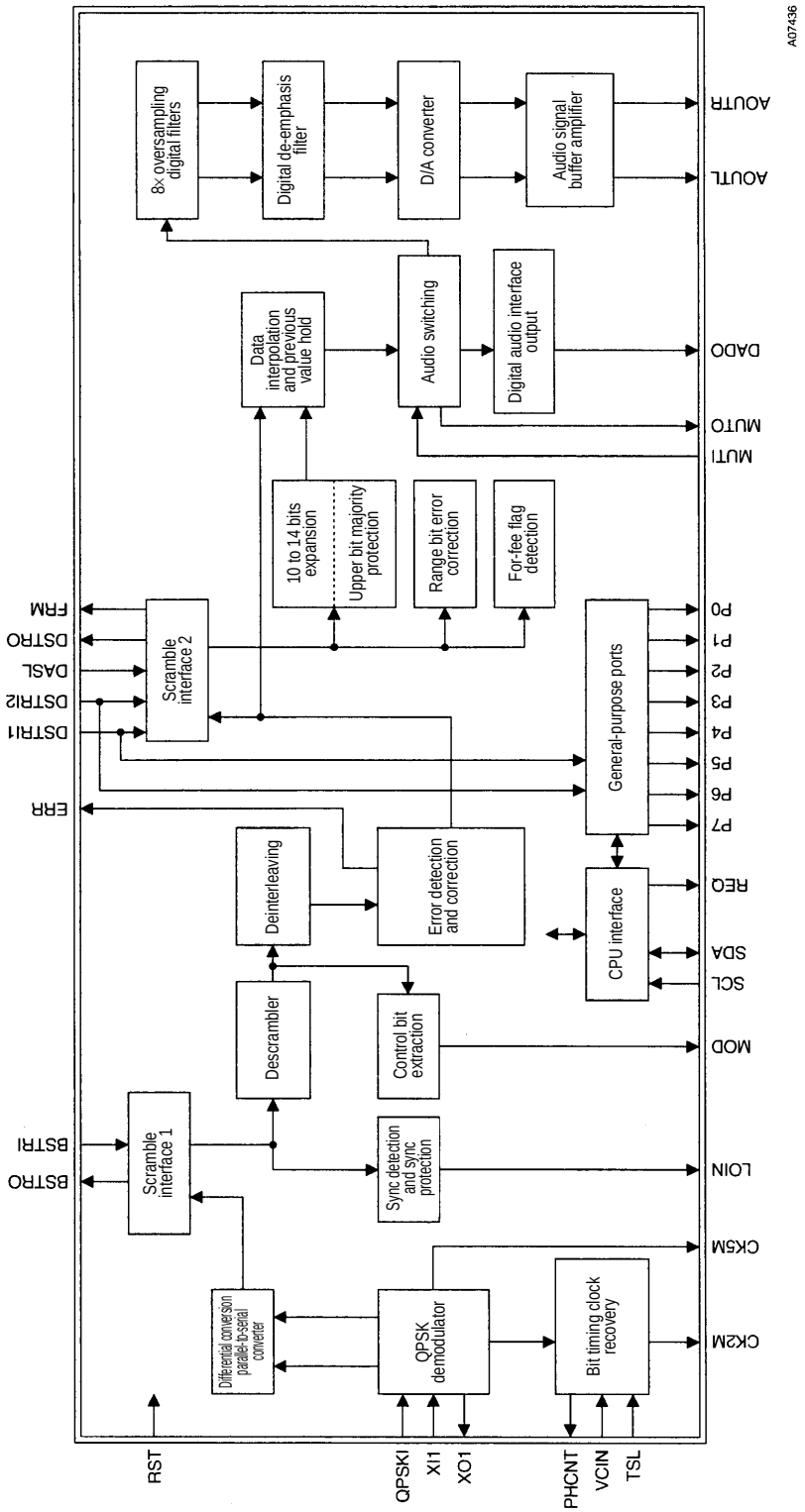
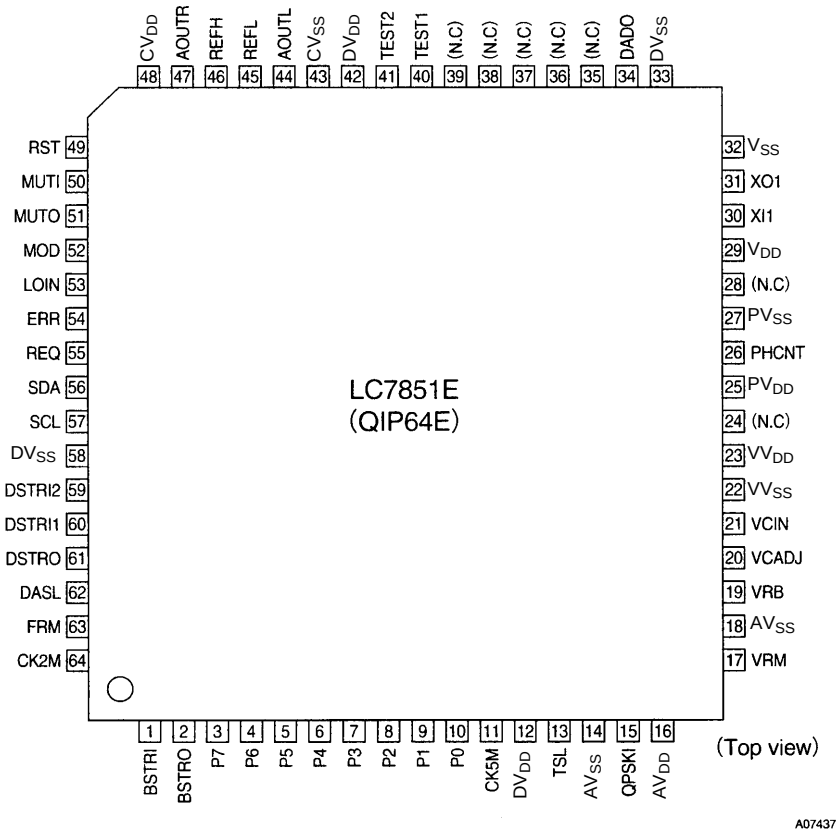
Block Diagram



Pin Assignment



Pin Functions

Pin No.	Pin	I/O	Function
1	BSTRI	I	Bit stream input
2	BSTRO	O	Bit stream output
3	P7	O	General-purpose output port
4	P6	O	General-purpose output port
5	P5	O	General-purpose output port
6	P4	O	General-purpose output port
7	P3	O	General-purpose output port
8	P2	O	General-purpose output port
9	P1	O	General-purpose output port
10	P0	O	General-purpose output port
11	CK5M	O	Filter adjustment clock output (5.7272 MHz)
12	DV_{DD}	I	Digital system power supply
13	TSL	I	Output control for the state when reset by the PHCNT pin (Low: high-impedance, high: 50% duty pulse output)
14	AV_{SS}	I	Internal A/D converter ground
15	QPSKI	I	QPSK modulated signal input
16	AV_{DD}	I	Internal A/D converter power supply
17	VRM	O	Internal A/D converter reference (center) output
18	AV_{SS}	I	Internal A/D converter ground
19	VRB	O	Internal A/D converter reference (low) output
20	VCADJ		Connection for internal VCO adjustment external resistor
21	VCIN	I	Internal VCO control input

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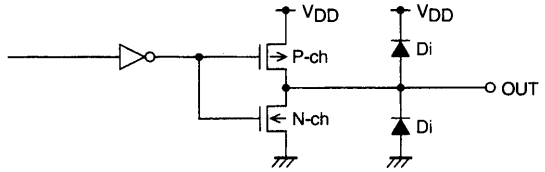
Pin No.	Pin	I/O	Function
22	VV_{SS}	I	Internal VCO ground
23	VV_{DD}	I	Internal VCO power supply
24	(N.C)		
25	PV_{DD}	I	Phase comparator power supply
26	PHCNT	O	Phase comparator output
27	PV_{SS}	I	Phase comparator ground
28	(N.C)		
29	V_{DD}	I	Oscillator circuit power supply
30	XI1	I	Crystal oscillator (22.909088 MHz) input
31	XO1	O	Crystal oscillator (22.909088 MHz) output
32	V_{SS}	I	Oscillator circuit ground
33	DV_{SS}	I	Digital system ground
34	DADO	O	Digital audio interface output
35	(N.C)		
36	(N.C)		
37	(N.C)		
38	(N.C)		
39	(N.C)		
40	TEST1	I	Test pin
41	TEST2	I	Test pin
42	DV_{DD}	I	Digital system power supply
43	CV_{SS}	I	Internal D/A converter ground
44	AOUTL	O	Left channel audio data output
45	REFL	O	Internal D/A converter reference voltage: low
46	REFH	O	Internal D/A converter reference voltage: high
47	AOUTR	O	Right channel audio data output
48	CV_{DD}	I	Internal D/A converter power supply
49	RST	I	Reset input
50	MUTI	I	Forced muting input
51	MUTO	O	Mute detection output (When muting detected: high)
52	MOD	O	Audio mode detection output (A mode: low, B mode: high)
53	LOIN	O	Frame synchronization detection output (When synchronized: low)
54	ERR	O	Error detection output (Error detected: high)
55	REQ	O	Host CPU readout request signal
56	SDA	I/O	I^2C bus data I/O
57	SCL	I	I^2C bus clock input
58	DV_{SS}	I	Digital system ground
59	DSTRI2	I	Data stream input 2/general-purpose I/O port
60	DSTRI1	I	Data stream input 1/general-purpose I/O port
61	DSTRO	O	Data stream output (post-error correction data)
62	DASL	I	Descrambler interface switching
63	FRM	O	Frame synchronization signal
64	CK2M	O	Bit stream clock (2.048 MHz)

Caution: All NC pins must be left open.

Pin Input and Output Circuit Diagrams

- Output pins (Output pins other than P0 to P7, SDA, PHCNT, CK5M, VRM, VRB, REFH, REFL, AOUTR, and AOUTL)



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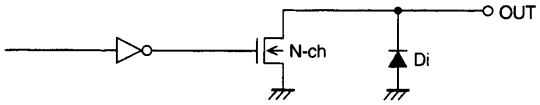
- Output pins: P0 to P7



These are n-channel open drain outputs.

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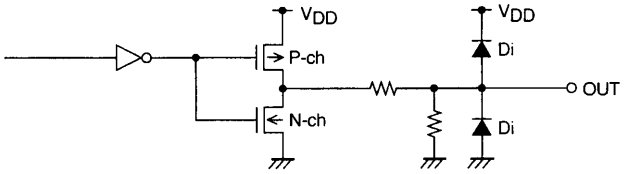
- Output pin: CK5M



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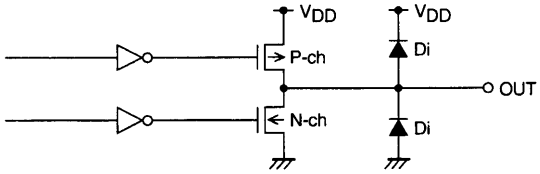
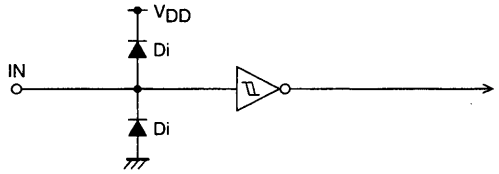
- Output pin: PHCNT



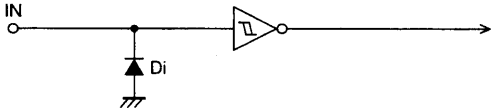
A07441

- Input pins (Input pins other than QPSKI, SCL, SDA, DSTRI1, DSTRI2, and VCIN)



A07442

- Input pins: SCL, DSTRI1, and DSTRI2



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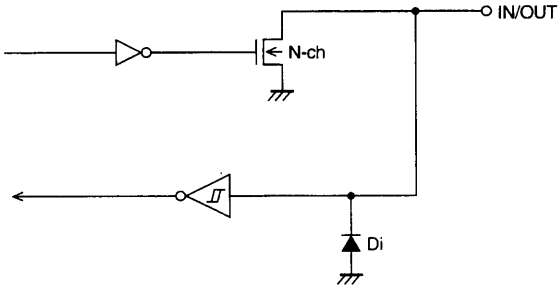
- I/O pin: SDA



A07444

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +7.0	V
Input voltage	V_I1	Pins other than SCL and SDA	–0.3 to V_{DD}+0.3	V
	V_I2	SCL and SDA	–0.3 to +5.3	V
Output voltage	V_O		–0.3 to VDD +0.3	V
Allowable power dissipation	Pd max	Ta = –20 to +75°C	360	mW
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input high-level voltage	V_{IH}		0.75 V_{DD}		V_{DD}	V
Input low-level voltage	V_{IL}		0		0.25 V_{DD}	V
QPSKI input voltage	V_{QPSKI}		0.7	0.9	1.1	V

DC Characteristics at Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5 V, GND = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{DD}			68	98	mA
Output high-level current	$I_{OH}1$	V_{OH} = V_{DD} – 0.4 V ; V_{OH} = V_{DD} – 0.4 V, CMOS output pins:PHCNT, LOIN, MOD, DSTRO, FRM, ERR, CK2M, BSTRO, MUTO, DADO, REQ, SYCKO	1.0			mA
	$I_{OH}2$	V_{OH} = V_{CK5MH} – 25 mV, CK5M	–350		–100	µA
Output low-level current 1	$I_{OL}1$	V_{OL} = 0.4 V ; CMOS output pins: PHCNT, LOIN, MOD, DSTRO, FRM, ERR, CK2M, BSTRO, MUTO, DADO, REQ, SYCKO	1.0			mA
	$I_{OL}2$	V_{OL} = 0.4 V, open drain output Pin 1: P0 to P7	1.0			mA
	$I_{OL}3$	V_{OL} = 0.4 V, open drain output Pin 2: SDA	4.0			mA
	$I_{OL}4$	V_{OL} = V_{CK5ML} + 25 mV, CK5M	100		350	µA
Output amplitude level	V_{CK5M}	I_{OH} = 30 µA, CK5M	236	295	354	mV
Input high-level current	I_{IH}	V_I = V_{DD}, Schmitt inputs: TSL, RST, TEST1, TEST2, BSTRI, DSTRI1, DSTRI2, DASL, MUTI, SCL, SDA, P0 to P7			10	µA
Input low-level current	I_{IL}	V_I = V_{SS}, Schmitt inputs: TSL, RST, TEST1, TEST2, BSTRI, DSTRI1, DSTRI2, DASL, MUTI, SCL, SDA, P0 to P7	–10			µA
Output load resistance	R_L	AOUTL and AOUTR	5.0			kΩ

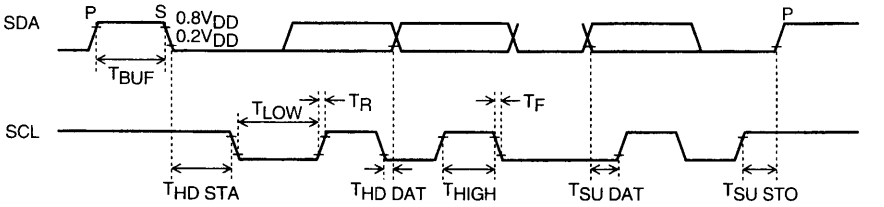
D/A Converter Characteristics at Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5 V, GND = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Resolution	RES	1 kHz 0 dB		16		Bits
Total harmonic distortion	THD1	1 kHz A mode, FS - 18 dB *		0.08		%
	THD2	1 kHz B mode, FS - 18 dB *		0.05		%
Signal-to-noise ratio	S/N	1 kHz 0 dB *		105		dB
Crosstalk	C. T	1 kHz 0 dB *		95		dB
Full scale output voltage	VFS		2.8	3.0	3.2	Vp-p

Note: *Values when measured in the Sanyo evaluation board and with a QPSK modulated signal (1 kHz sine wave) input.

I²C Bus Interface at Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5 V, GND = 0 V

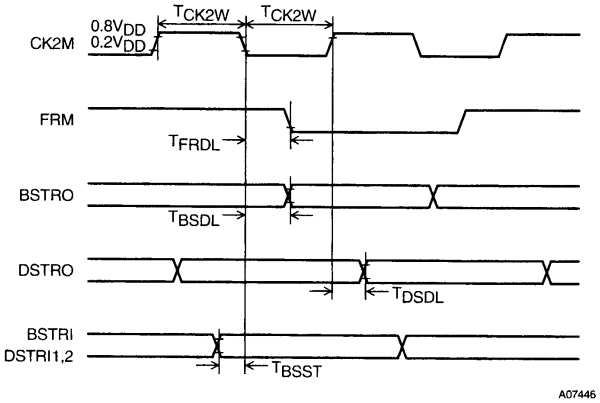
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
SCL frequency	f_{SCL}				100	kHz
Bus release time	T_{BUF}		4.7			µs
Start hold time	$T_{HD\ STA}$		4.0			µs
SCL low time	T_{LOW}		4.7			µs
SCL high time	T_{HIGH}		4.0			µs
Data hold time	$T_{HD\ DAT}$		0			ns
Data setup time	$T_{SU\ DAT}$		250			ns
Rise time	T_R				1000	ns
Fall time	T_F				300	ns
Stop setup time	$T_{SU\ STO}$		4.0			µs



S: Start condition
P: Stop condition

Descrambler Interface at Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5 V, GND = 0 V

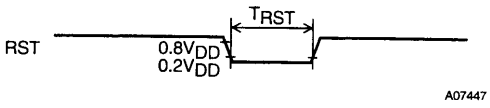
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Clock pulse width	T_{CK2M}		244			ns
BSTRO pin output delay time	T_{BSDL}				15	ns
DSTRO pin output delay time	T_{DSDL}				15	ns
BSTRI and DSTRI1 two-pin input setup time	T_{BSST}		10			ns



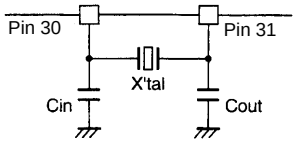
Reset Timing at Power on at Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5 V, GND = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Reset time	T_{RST}	TSL pin high; The LC7851E must be used with the TSL pin (pin 13) high.	200			ms

The LC7851E must be reset with the following timing when power is first applied.



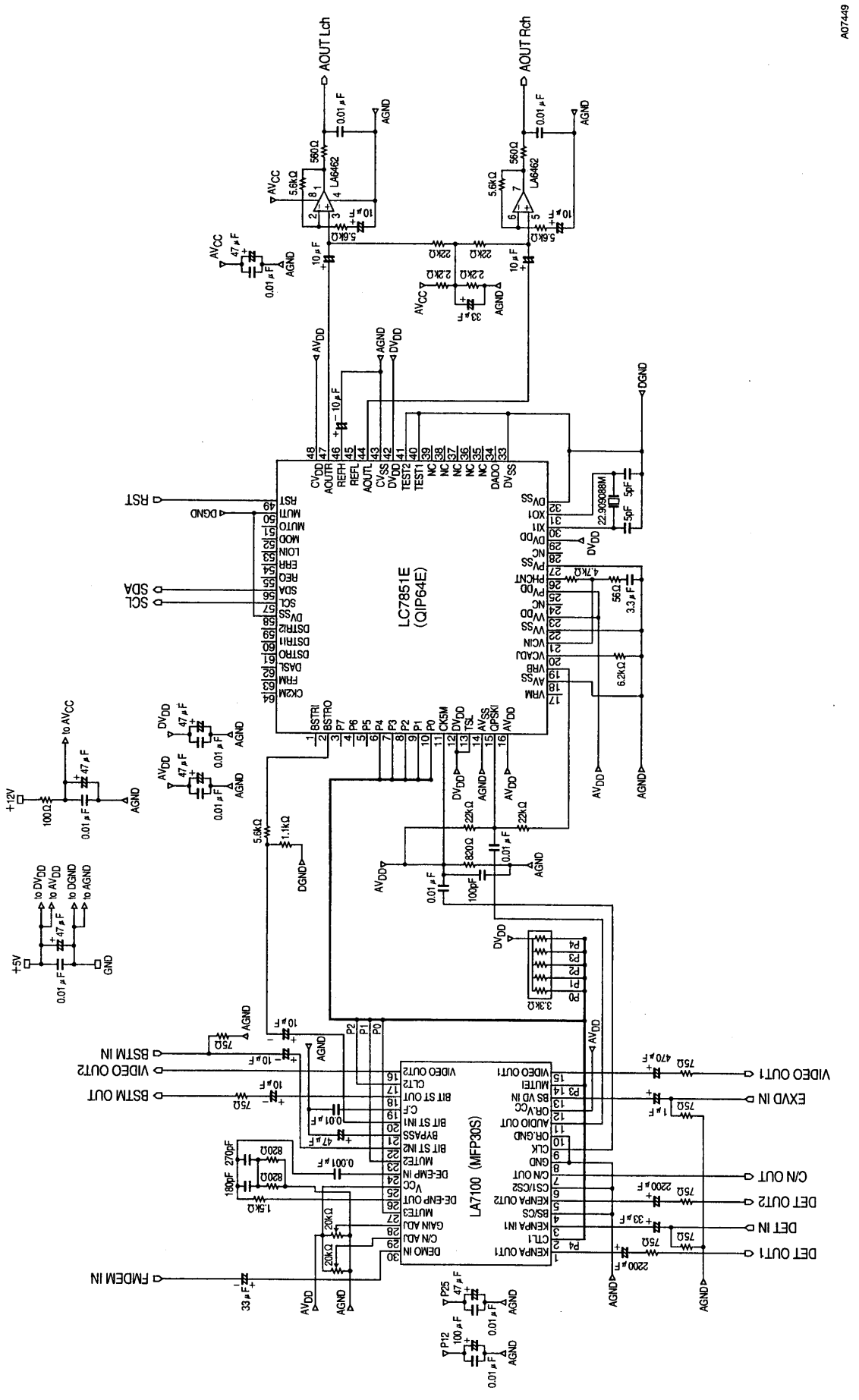
Pin I/O Circuit



Recommended Crystal Oscillator Constants

Supplier	Oscillator element	Cin/Cout
Citizen Watch Co., Ltd.	CSA-309 (22.909088 MHz)	5pF (Cin = Cout)

Application Circuit Diagram



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