LC²MOS Complete 12-Bit 100 kHz Sampling ADC with DSP Interface

AD7878

FEATURES

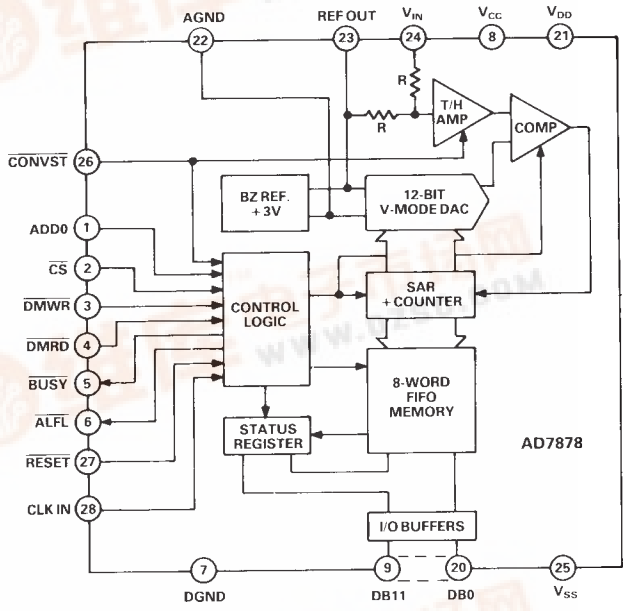
Complete ADC with DSP Interface, Comprising:
- Track/Hold Amplifier with 2 μs Acquisition Time
- 7 μs A/D Converter
- 3 V Zener Reference
- 8-Word FIFO and Interface Logic

72 dB SNR at 10 kHz Input Frequency
Interfaces to High Speed DSP Processors, e.g., ADSP-2100, TMS32010, TMS32020
41 ns max Data Access Time
Low Power, 60 mW typ

APPLICATIONS

Digital Signal Processing
Speech Recognition and Synthesis
Spectrum Analysis
High Speed Modems
DSP Servo Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7878 is a fast, complete, 12-bit A/D converter with a versatile DSP interface consisting of an 8-word, first-in, first-out (FIFO) memory and associated control logic.

The FIFO memory allows up to eight samples to be digitized before the microprocessor is required to service the A/D converter. The eight words can then be read out of the FIFO at maximum microprocessor speed. A fast data access time of 41 ns allows direct interfacing to DSP processors and high speed 16-bit microprocessors.

An on-chip status/control register allows the user to program the effective length of the FIFO and contains the FIFO out of range, FIFO empty and FIFO word count information.

The analog input of the AD7878 has a bipolar range of ±3 V. The AD7878 can convert full power signals up to 50 kHz and is fully specified for dynamic parameters such as signal-to-noise ratio and harmonic distortion.

The AD7878 is fabricated in Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in four package styles, 28-pin plastic and hermetic dual-in-line package (DIP), leadless ceramic chip carrier (LCCC) or plastic leaded chip carrier (PLCC).

PRODUCT HIGHLIGHTS

1. Complete A/D Function with DSP Interface
   The AD7878 provides the complete function for digitizing ac signals to 12-bit accuracy. The part features an on-chip track/hold, on-chip reference and 12-bit A/D converter. The additional feature of an 8-word FIFO reduces the high software overheads associated with servicing interrupts in DSP processors.
2. Dynamic Specifications for DSP Users
   The AD7878 is fully specified and tested for ac parameters, including signal-to-noise ratio, harmonic distortion and intermodulation distortion. Key digital timing parameters are also tested and specified over the full operating temperature range.
3. Fast Microprocessor Interface
   Data access time of 41 ns is the fastest ever achieved in a monolithic A/D converter, and makes the AD7878 compatible with all modern 16-bit microprocessors and digital signal processors.

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AD7878–SPECIFICATIONS (V_{DD} = +5 V ± 5%, V_{CC} = +5 V ± 5%, V_{SS} = –5 V ± 5%, AGND = DGND = 0 V, f_{CLK} = 8 MHz. All Specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	J, A Versions[1]	K, L, B Versions	S Version	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]					
Signal-to-Noise Ratio (SNR)[3] @ 25°C	70	72	70	dB min	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz
T_{MIN} to T_{MAX}	70	71	70	dB min	Typically 71.5 dB for 0 < V_{IN} < 50 kHz
Total Harmonic Distortion (THD)	–80	–80	–78	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz Typically –86 dB for 0 < V_{IN} < 50 kHz
Peak Harmonic or Spurious Noise	–80	–80	–78	dB max	V_{IN} = 10 kHz, f_{SAMPLE} = 100 kHz Typically –86 dB for 0 < V_{IN} < 50 kHz
Intermodulation Distortion (IMD)					
Second Order Terms	–80	–80	–78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	–80	–80	–78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Track/Hold Acquisition Time	2	2	2	µs max	See Throughput Rate Section
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution for Which No Missing Codes are Guaranteed	12	12	12	Bits	
Relative Accuracy	±1/2	±1/4	±1/2	LSB typ	
Differential Nonlinearity	±1/2	±1/2	±1/2	LSB typ	
Bipolar Zero Error	±6	±6	±6	LSB max	
Positive Full-Scale Error[4]	±6	±6	±6	LSB max	
Negative Full-Scale Error[4]	±6	±6	±6	LSB max	
ANALOG INPUT					
Input Voltage Range	±3	±3	±3	Volts	
Input Current	±550	±550	±550	µA max	
REFERENCE OUTPUT[5]					
REF OUT	3	3	3	V nom	
REF OUT Error @ 25°C	±10	±10	±10	mV max	
T_{MIN} to T_{MAX}	±15	±15	±15	mV max	
Reference Load Sensitivity (ΔREF OUT/ΔI)	±1	±1	±1	mV max	Reference Load Current Change (0 µA–500 µA). Reference Load Should Not Be Changed During Conversion
LOGIC INPUTS					
Input High Voltage, V_{INH}	+2.4	+2.4	+2.4	V min	V_{CC} = +5 V ± 5%
Input Low Voltage, V_{INL}	+0.8	+0.8	+0.8	V max	V_{CC} = +5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	µA max	V_{IN} = 0 to V_{CC}
Input Capacitance, C_{IN}[6]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	+2.7	+2.7	+2.7	V min	I_{SOURCE} 40 µA
Output Low Voltage, V_{OL}	+0.4	+0.4	+0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0					
Floating State Leakage Current	±10	±10	±10	±10	µA max
Floating State Output Capacitance[6]	15	15	15	15	pF max
CONVERSION TIME					
	7/7.125	7/7.125	7/7.125	µs min/µs max	Assuming No External Read/Write Operations
	7/9.250	7/9.250	7/9.250	µs min/µs max	Assuming 17 External Read/Write Operations See Internal Comparator Timing Section
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{CC}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	–5	–5	–5	V nom	±5% for Specified Performance
I_{DD}	13	13	13	mA max	$\overline{CS}$ = $\overline{DMWR}$ = $\overline{DMRD}$ = 5 V
I_{CC}	100	100	100	µA max	$\overline{CS}$ = $\overline{DMWR}$ = $\overline{DMRD}$ = 5 V
I_{SS}	6	6	6	mA max	$\overline{CS}$ = $\overline{DMWR}$ = $\overline{DMRD}$ = 5 V
Power Dissipation	95.5	95.5	95.5	mW max	Typically 60 mW

NOTES

[1]Temperature range as follows: J, K, L versions: 0°C to +70°C; A, B versions: –25°C to +85°C; S version: –55°C to +125°C.

[2]V_{IN} = ±3 V. See Dynamic Specifications section.

[3]SNR calculation includes distortion and noise components.

[4]Measured with respect to the Internal Reference.

[5]For capacitive loads greater than 50 pF a series resistor is required (see Internal Reference section).

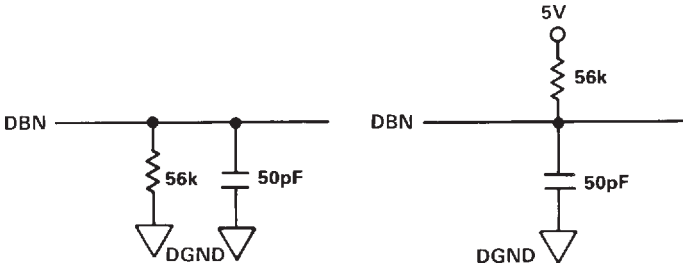
[6]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = 5 V ± 5%, V_{CC} = 5 V ± 5%, V_{SS} = –5 V ± 5%)

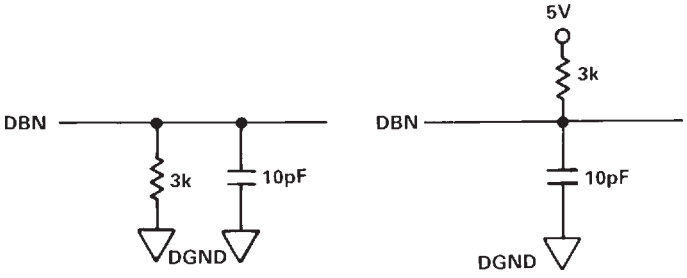
Parameter	Limit at T_{MIN}, T_{MAX} (L Grade)	Limit at T_{MIN}, T_{MAX} (J, K, A, B Grades)	Limit at T_{MIN}, T_{MAX} (S Grade)	Units	Conditions/Comments
t_1	65	65	75	ns max	CLK IN to $\overline{BUSY}$ Low Propagation Delay
t_2	65	65	75	ns max	CLK IN to $\overline{BUSY}$ High Propagation Delay
t_3	2 CLK IN Cycles	2 CLK IN Cycles	2 CLK IN Cycles	min	$\overline{CONVST}$ Pulse Width
t_4	0	0	0	ns min	$\overline{CS}$ to $\overline{DMRD}$/REGISTER ENABLE Setup Time
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{DMRD}$/ REGISTER ENABLE Hold Time
t_6	**45**	**60**	**60**	ns min	$\overline{DMRD}$ Pulse Width
	50	50	50	µs max	
t_7	**16**	**16**	**16**	ns min	ADD0 to $\overline{DMRD}$/REGISTER ENABLE Setup Time
t_8	0	0	0	ns min	ADD0 to $\overline{DMRD}$/REGISTER ENABLE Hold Time
t_9[2]	**41**	**57**	**57**	ns min	Data Access Time after $\overline{DMRD}$
t_{10}[3]	5	5	5	ns min	Bus Relinquish Time
	45	**45**	**45**	ns max	
t_{11}	**42**	**42**	**55**	ns min	REGISTER ENABLE Pulse Width
	50	50	50	µs max	
t_{12}	**20**	**20**	**30**	ns min	Data Valid to REGISTER ENABLE Setup Time
t_{13}	10	10	10	ns min	Data Hold Time after REGISTER ENABLE
t_{14}[2]	41	57	57	ns min	Data Access Time after BUSY
t_{RESET}	2 CLK IN Cycles	2 CLK IN Cycles	2 CLK IN Cycles	min	RESET Pulse Width

NOTES
[1]Timing Specifications in **bold** print are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]t_9 and t_{14} are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[3]t_{10} is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.



a. High-Z to V_{OH} *b. High-Z to V_{OL}*

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 2. Load Circuits for Output Float Delay

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

V_{DD} to DGND . . . . . –0.3 V to +7 V
V_{CC} to DGND . . . . . –0.3 V to +7 V
V_{SS} to DGND . . . . . +0.3 V to –7 V
V_{DD} to V_{CC} . . . . . –0.3 V to +0.3 V
AGND to DGND . . . . . –0.3 V to V_{DD} +0.3 V
V_{IN} to AGND . . . . . –15 V to +15 V
REF OUT to AGND . . . . . 0 to V_{DD}
Digital Inputs to DGND
  CLK IN, $\overline{DMWR}$, $\overline{DMRD}$, $\overline{RESET}$,
  $\overline{CS}$, $\overline{CONVST}$, ADD0 . . . . . –0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND
  $\overline{ALFL}$, $\overline{BUSY}$ . . . . . –0.3 V to V_{DD} +0.3 V
Data Pins
  DB11–DB0 . . . . . –0.3 V to V_{DD} +0.3 V
Operating Temperature Range
  J, K, L Versions . . . . . 0°C to +70°C
  A, B Versions . . . . . –25°C to +85°C
  S Version . . . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
  Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

CAUTION

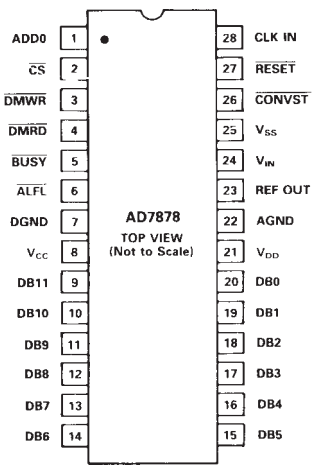
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7878 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

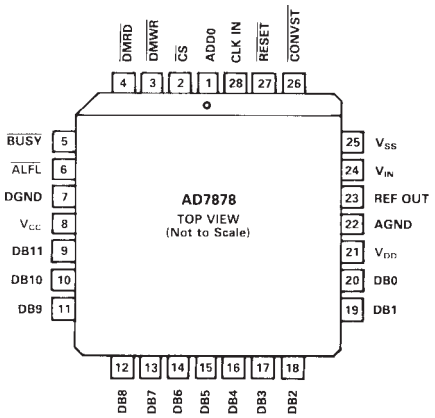
Pin Number	Pin Mnemonic	Function
1	ADD0	Address Input. This control input determines whether the word placed on the output data bus during a read operation is a data word from the FIFO RAM or the contents of the status/control register. A logic low accesses the data word from Location 0 of the FIFO while a logic high selects the contents of the register (see Status/Control Register section).
2	$\overline{CS}$	Chip Select. Active low logic input. The device is selected when this input is active.
3	$\overline{DMWR}$	Dam Memory Write. Active low logic input. $\overline{DMWR}$ is used in conjunction with $\overline{CS}$ low and ADD0 high to write data to the status/control register. Corresponds to $\overline{DMWR}$ (ADSP-2100), R/$\overline{W}$ (MC68000, TMS32020), $\overline{WE}$ (TMS32010).
4	$\overline{DMRD}$	Data Memory READ. Active low logic input. $\overline{DMRD}$ is used in conjunction with $\overline{CS}$ low to enable the three-state output buffers. Corresponds directly to $\overline{DMRD}$ (ADSP-2100), $\overline{DEN}$ (TMS32010).
5	$\overline{BUSY}$	Active Low Logic Output. This output goes low when the ADC receives a $\overline{CONVST}$ pulse and remains low until the track/hold has gone into its hold mode. The three-state drivers of the AD7878 can be disabled while the $\overline{BUSY}$ signal is low (see Extended READ/WRITE section). This is achieved by writing a logic 0 to DB5 ($\overline{DISO}$) of the status/control register. Writing a logic 1 to DB5 of the status/control register allows data to be accessed from the AD7878 while BUSY is low.
6	$\overline{ALFL}$	FIFO Almost Full. A logic low indicates that the word count (i.e., number of conversion results) in the FIFO memory has reached the programmed word count in the status/control register. $\overline{ALFL}$ is updated at the end of each conversion. The $\overline{ALFL}$ output is reset to a logic high when a word is read from the FIFO memory and the word count is less than the preprogrammed word count. It can also be set high by writing a logic 1 to DB7 ($\overline{ENAF}$) of the status/control register.
7	DGND	Digital Ground. Ground reference for digital circuitry.
8	V_{CC}	Digital supply voltage, +5 V ± 5%. Positive supply voltage for digital circuitry.
9	DB11	Data Bit 11 (MSB). Three-state TTL output. Coding for the data words in FIFO RAM is twos complement.
10–15	DB10–DB5	Data Bit 10 to Data Bit 5. Three-state TTL input/outputs.
16–19	DB4–DB1	Data Bit 4 to Data Bit 1. Three-state TTL outputs.
20	DB0	Data Bit 0 (LSB). Three-state TTL output.
21	V_{DD}	Analog positive supply voltage, +5 V ± 5%.
22	AGND	Analog Ground. Ground reference for track/hold, reference and DAC.
23	REF OUT	Voltage Reference Output. The internal 3 V analog reference is provided at this pin. The external load capability of the reference is 500 μA.
24	V_{IN}	Analog Input. Analog input range is ±3 V.
25	V_{SS}	Analog negative supply voltage, –5 V ± 5%.
26	$\overline{CONVST}$	Convert Start. Logic input. A low to high transition on this input puts the track/hold into its hold mode and starts conversion. The $\overline{CONVST}$ input is asynchronous to CLK IN and independent of $\overline{CS}$, $\overline{DMWR}$ and $\overline{DMRD}$.
27	$\overline{RESET}$	Reset. Active low logic input. A logic low sets the words in FIFO memory to 1000 0000 0000 and resets the $\overline{ALFL}$ output and status/control register.
28	CLK IN	Clock Input. TTL-compatible logic input. Used as the clock source for the A/D converter. The mark-space ratio of this clock can vary from 35/65 to 65/35.

PIN CONFIGURATIONS

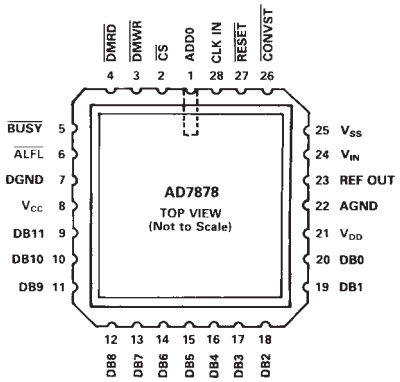
DIP



PLCC



LCCC



ORDERING GUIDE

Model[1, 2]	Temperature Range	Signal-to-Noise Ratio	Data Access Time	Package Options[3]
AD7878JN	0°C to +70°C	70 dB	57 ns	N-28
AD7878AQ	–25°C to +85°C	70 dB	57 ns	Q-28
AD7878SQ	–55°C to +125°C	70 dB	57 ns	Q-28
AD7878KN	0°C to +70°C	72 dB	57 ns	N-28
AD7878BQ	–25°C to +85°C	72 dB	57 ns	Q-28
AD7878LN	0°C to +70°C	72 dB	41 ns	N-28
AD7878SE[4]	–55°C to +125°C	70 dB	57 ns	E-28A
AD7878JP	0°C to +70°C	70 dB	57 ns	P-28A
AD7878KP	0°C to +70°C	72 dB	57 ns	P-28A
AD7878LP	0°C to +70°C	72 dB	41 ns	P-28A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact our local sales office for military data sheet.
[2]Analog Devices reserves the right to ship either ceramic (D-28) packages or cerdip (Q-28) hermetic packages.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier, Q = Cerdip.
[4]Available to /883B processing only.

STATUS/CONTROL REGISTER

The status/control register serves the dual function of providing control and monitoring the status of the FIFO memory. This register is directly accessible through the data bus (DB11–DB0) with a read or write operation while ADD0 is high. A write operation to the status/control register provides control for the $\overline{\text{ALFL}}$ output, bus interface and FIFO counter reset. This is normally done on power-up initialization. The FIFO memory address pointer is incremented after each conversion and compared with a preprogrammed count in the status/control register. When this preprogrammed count is reached, the $\overline{\text{ALFL}}$ output is asserted if the $\overline{\text{ENAF}}$ control bit is set to zero. This $\overline{\text{ALFL}}$ can be used to interrupt the microprocessor after any predetermined number of conversions (between 1 and 8). The status of the address pointer along with sample overrange and $\overline{\text{ALFL}}$ status can be accessed at any time by reading the status/control register. Note: reading the status/control register does not cause any internal data movement in the FIFO memory. Status information for a particular word should be read from the status register before the data word is read from the FIFO memory.

STATUS/CONTROL REGISTER FUNCTION DESCRIPTION

DB11 ($\overline{\text{ALFL}}$)
Almost Full Flag, Read only. This is the same as Pin 6 ($\overline{\text{ALFL}}$ output) status. A logic low indicates that the word count in the FIFO memory has reached the preprogrammed count in bit locations DB10–DB8. $\overline{\text{ALFL}}$ is updated at the end of conversion.

DB10–DB8 (AFC2–AFC0)
Almost Full Word Count, Read/Write. The count value determines the number of words in the FIFO memory, which will cause $\overline{\text{ALFL}}$ to be set. When the FIFO word count equals the programmed count in these three bits, both the $\overline{\text{ALFL}}$ output and DB11 of the status register are set to a logic low. For example, when a code of 011 is written to these bits, $\overline{\text{ALFL}}$ is set when Location 0 through Location 3 of the FIFO memory contains valid data. AFC2 is the most significant bit of the word count. The count value can be read back if required.

DB7 ($\overline{\text{ENAF}}$)
Enable Almost Full, Read/Write. Writing a 1 to this bit disables the $\overline{\text{ALFL}}$ output and status register bit DB11.

DB6 (FOVR/RESET)
FIFO Overrun/RESET, Read/Write. Reading a 1 from this bit indicates that at least one sample has been discarded because the FIFO memory is full. When the FIFO is full (i.e., contains eight words) any further conversion results will be lost. Writing a 1 to this bit causes a system RESET as per the $\overline{\text{RESET}}$ input (Pin 27).

DB5 (FOOR/DISO)
FIFO Out of RANGE/Disable Outputs, Read/Write. Reading a 1 from this bit indicates that at least one sample in the FIFO memory is out of range. Writing a 0 to this bit prevents the data bus from becoming active while $\overline{\text{BUSY}}$ is low, regardless of the state of $\overline{\text{CS}}$ and $\overline{\text{DMRD}}$.

DB4 (FEMP)
FIFO Empty, Read Only. Reading a 1 indicates there are no samples in the FIFO memory. When the FIFO is empty the internal ripple-down effects of the FIFO are disabled and further reads will continue to access the last valid data word in Location 0.

DB3 (SOOR)
Sample out of Range, Read Only. Reading a 1 indicates the next sample to be read is out of range, i.e., the sample in Location 0 of the FIFO.

DB–DB0 (FCN2–FCN0)
FIFO Word Count, Read Only. The value read from these bits indicates the number of samples in the FIFO memory. For example, reading 011 from these bits indicates that Location 0 through Location 3 contains valid data. Note: reading all 0s indicates there is either one word or no word in the FIFO memory; in this case the FIFO Empty determines if there is no word in memory. FCN2 is the most significant bit.

Table I. Status/Control Bit Function Description

BIT LOCATION	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
STATUS INFORMATION (READ)	$\overline{\text{ALFL}}$	AFC2	AFC1	AFC0	$\overline{\text{ENAF}}$	FOVR	FOOR	FEMP	SOOR	FCN2	FCN1	FCN0
CONTROL FUNCTION (WRITE)	X	AFC2	AFC1	AFC0	$\overline{\text{ENAF}}$	RESET	$\overline{\text{DISO}}$	X	X	X	X	X
RESET STATUS	1	0	0	0	0	0	0	1	0	0	0	0

X =DON'T CARE

INTERNAL FIFO MEMORY

The internal FIFO memory of the AD7878 consists of eight memory locations. Each word in memory contains 13 bits of information—12 bits of data from the conversion result and one additional bit which contains information as to whether the 12-bit result is out of range or not. A block diagram of the AD7878 FIFO architecture is shown in Figure 3.

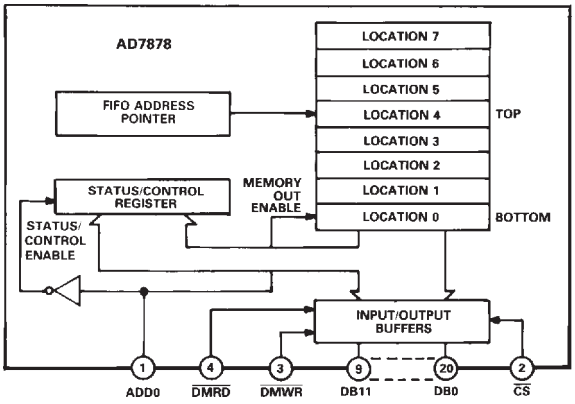


Figure 3. Internal FIFO Architecture

The conversion result is gathered in the successive approximation register (SAR) during conversion. At the end of conversion this result is transferred to the FIFO memory. The FIFO address pointer always points to the top of memory, which is the uppermost location containing valid data. The pointer is incremented after each conversion. A read operation from the FIFO memory accesses data from the bottom of the FIFO, Location 0. On completion of the read operation, each data word moves down one location and the address pointer is decremented by one. Therefore, each conversion result from the SAR enters at the top of memory, propagates down with successive reads until it reaches Location 0 from where it can be accessed by a microprocessor read operation.

The transfer of information from the SAR to the FIFO occurs in synchronization with the AD7878 input clock (CLK IN). The propagation of data words down the FIFO is also synchronous with this clock. As a result, a read operation to obtain data from the FIFO must also be synchronous with CLK IN to avoid Read/Write conflicts in the FIFO (i.e., reading from FIFO Location 0 while it is being updated). This requires that the microprocessor clock and the AD7878 CLK IN are derived from the same source.

INTERNAL COMPARATOR TIMING

The ADC clock, which is applied to CLK IN, controls the successive approximation A/D conversion process. This clock is internally divided by four to yield a bit trial cycle time of 500 ns min (CLK IN = 8 MHz clock). Each bit decision occurs 25 ns after the rising edge of this divided clock. The bit decision is latched by the rising edge of an internal comparator strobe signal. There are 12-bit decisions, as in a normal successive approximation routine, and one extra decision that checks if the input sample is out of range. In a normal successive approximation A/D converter, reading data from the device during conversion can upset the conversion in progress. This is due to on-chip transients, generated by charging or discharging the databus, concurrent with a bit decision. The scheme outlined below and shown in Figure 4 describes how the AD7878 overcomes this problem.

The internal comparator strobe on the AD7878 is gated with both $\overline{\text{DMRD}}$ and $\overline{\text{DMWR}}$ so that if a read or write operation occurs when a bit decision is about to be made, the bit decision point is deferred by one CLK IN cycle. In other words, if $\overline{\text{DMRD}}$ or $\overline{\text{DMWR}}$ goes low (with $\overline{\text{CS}}$ low) at any time during the CLK IN low time immediately prior to the comparator strobing edge (t_{LOW} of Figure 4), the bit trial is suspended for a clock cycle. This makes sure that the bit decision is latched at a time when the AD7878 is not attempting to charge or discharge the data bus, thereby ensuring that no spurious transients occur internally near a bit decision point.

The decision point slippage mechanism is shown in Figure 4 for the MSB decision. Normally, the MSB decision occurs 25 ns after the fourth rising CLK IN edge after $\overline{\text{CONVST}}$ goes high. However, in the timing diagram of Figure 4, $\overline{\text{CS}}$ and $\overline{\text{DMRD}}$ or $\overline{\text{DMWR}}$ are low in the time period t_{LOW} prior to the MSB decision point on the fourth rising edge. This causes the internal comparator strobe to be slipped to the fifth rising clock edge. The AD7878 will again check during a period t_{LOW} prior to this fifth rising clock edge; and if the $\overline{\text{CS}}$ and $\overline{\text{DMRD}}$ or $\overline{\text{DMWR}}$ are still low, the bit decision point will be slipped a further clock cycle.

The conversion time for the ADC normally consists of the 13-bit trials described above and one extra internal clock cycle during which data is written from the SAR to the FIFO. For an 8 MHz input clock this results in a conversion time of 7 μs. However, the software routine servicing the AD7878 has the potential to read 16 times from the device during conversion—8 reads from the FIFO and 8 reads from the status/control register. It also has the potential to write once to the status/control register. If these

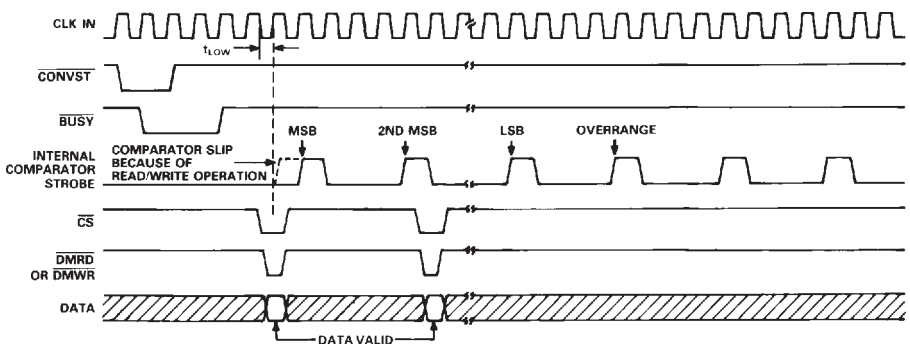


Figure 4. Operational Timing Diagram

17 (16 read plus 1 write) operations all occur during t_{LOW} time periods, the conversion time will slip by 17 CLK IN cycles. Therefore, if read or write operations can occur during t_{LOW} periods, it means that the conversion time for the ADC can vary from 7 μs to 9.12 μs (assuming 8 MHz CLK IN). This calculation assumes there is a slippage of one CLK IN cycle for each read or write operation.

INITIATING A CONVERSION

Conversion is initiated on the AD7878 by asserting the $\overline{\text{CONVST}}$ input. This $\overline{\text{CONVST}}$ input is an asynchronous input independent of either the ADC or DSP clocks. This is essential for applications where precise sampling in time is important. In these applications the signal sampling must occur at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. In these cases the $\overline{\text{CONVST}}$ input is driven from a tamer or some precise clock source. On receipt of a $\overline{\text{CONVST}}$ pulse, the AD7878 acknowledges by taking the $\overline{\text{BUSY}}$ output low. This $\overline{\text{BUSY}}$ output can be used to ensure no bus activity while the track/hold goes from track to hold mode (see Extended Read/Write section). The $\overline{\text{CONVST}}$ input must stay low for at least two CLK IN periods. The track/hold amplifier switches from the track to hold mode on the rising edge of $\overline{\text{CONVST}}$ and conversion is also initiated at this point. The $\overline{\text{BUSY}}$ output returns high after the $\overline{\text{CONVST}}$ input goes high and the ADC begins its successive approximation routine. Once conversion has been initiated another conversion start should not be attempted until the full conversion cycle has been completed. Figure 5 shows the taming diagram for the conversion start.

In applications where precise sampling is not critical, the $\overline{\text{CONVST}}$ pulse can be generated from a microprocessor $\overline{\text{WR}}$ or $\overline{\text{RD}}$ line gated with a decoded address (different from the AD7878 $\overline{\text{CS}}$ address). Note that the $\overline{\text{CONVST}}$ pulse width must be a minimum of two AD7878 CLK IN cycles.

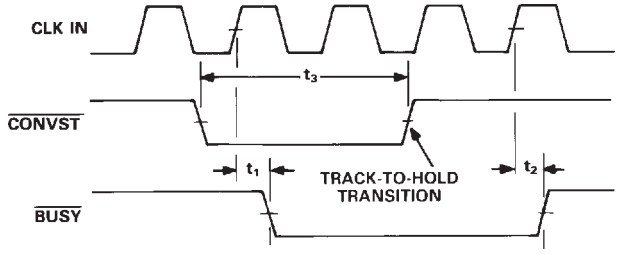


Figure 5. Conversion Start Timing Diagram

READ/WRITE OPERATIONS

The AD7878 read/write operations consist of reading from the FIFO memory and reading and writing from the status/control register. These operations are controlled by the $\overline{\text{CS}}$, $\overline{\text{DMRD}}$, $\overline{\text{DMWR}}$ and ADD0 logic inputs. A description of these operations is given in the following sections. In addition to the basic read/write operations there is an extended read/write operation. This can occur if a read/write operation occurs during a $\overline{\text{CONVST}}$ pulse. This extended read/write is intended for use with microprocessors that can be driven into a WAIT state, and the scheme is recommended for applications where an external timer controls the $\overline{\text{CONVST}}$ input asynchronously to the microprocessor read/write operations.

Basic Read Operation

Figure 6 shows the timing diagram for a basic read operation on the AD7878. $\overline{\text{CS}}$ and $\overline{\text{DMRD}}$ going low accesses data from either the status/control register or the FIFO memory. A read operation with ADD0 low accesses data from the FIFO while a read with ADD0 high accesses data from the status/ control register.

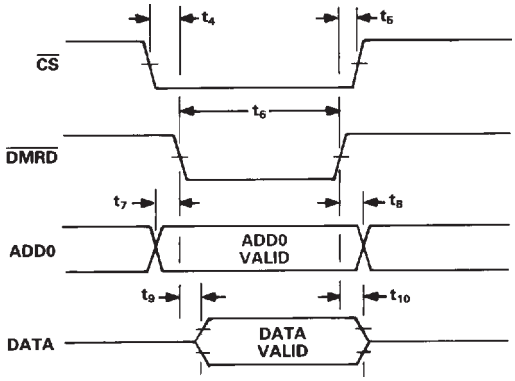


Figure 6. Basic Read Operation

Basic Write Operation

A basic write operation to the AD7878 status/control register consists of bringing $\overline{\text{CS}}$ and $\overline{\text{DMWR}}$ low with ADD0 high. Internally these signals are gated with CLK IN to provide an internal REGISTER ENABLE signal (see Figure 7). The pulse width of this REGISTER ENABLE signal is effectively the overlap between the CLK IN low time and the $\overline{\text{DMWR}}$ pulse. This may result in shorter write pulse widths, data setup times and data hold times than those given by the microprocessor. The timing on the AD7878 timing diagram of Figure 8 is therefore given with respect to the internal REGISTER ENABLE signal rather than the $\overline{\text{DMWR}}$ signal.

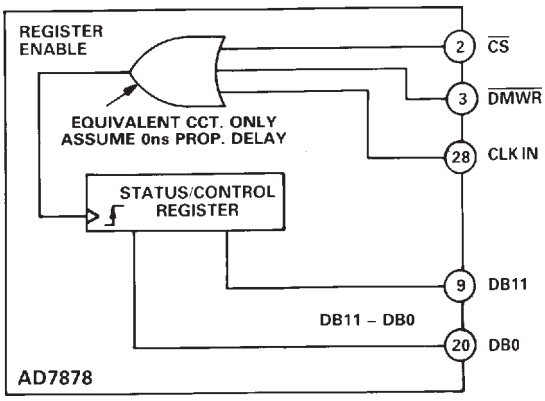


Figure 7. $\overline{\text{DMWR}}$ Internal Logic

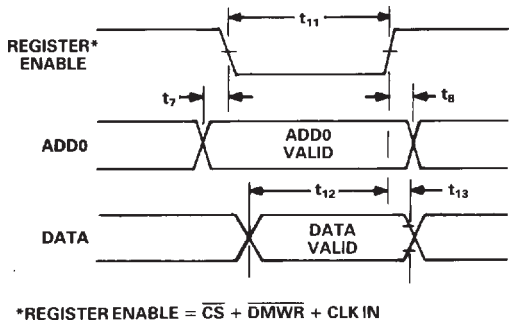


Figure 8. Basic Write Operation

Extended Read/Write Operation

As described earlier, a read/write operation to the AD7878 can cause spurious on-chip transients. Should these transients occur while the track/hold is going from track to hold mode, it may result in an incorrect value of V_{IN} being held by the track/hold amplifier. Because the $\overline{CONVST}$ input has asynchronous capability, a read/write operation could occur while $\overline{CONVST}$ is low. The AD7878 allows the read/write operation to occur but has the facility to disable its three-state drivers so that there is no data bus activity and, hence, no transients while the track/hold goes from track to hold.

Writing a logic 0 to DB5 ($\overline{DISO}$) of the status/control register prevents the output latches from being enabled while the AD7878 $\overline{BUSY}$ signal is low. If a microprocessor read/write operation can occur during the $\overline{BUSY}$ low time, the $\overline{BUSY}$ should be gated with $\overline{CS}$ of the AD7878 and this gated signal used to stretch the instruction cycle using DMACK (ADSP-2100), READY (TMS32020) or $\overline{DTACK}$ (68000).

When $\overline{CONVST}$ goes low, the AD7878 acknowledges it by bringing $\overline{BUSY}$ low on the next rising edge of CLK IN. With a logic 0 in DB5, the AD7878 data bus cannot now be enabled. If a read/write operation now occurs, the $\overline{BUSY}$ and $\overline{CS}$ gated signal drives the microprocessor into a WAIT state, thereby extending the read/write operation. $\overline{BUSY}$ goes high on the second rising edge of CLK IN after $\overline{CONVST}$ goes high. The AD7878 data outputs are now enabled and the microprocessor is released from its WAIT state, allowing it to complete its read/write operation to the AD7878.

The microprocessor cycle time for the read/write operation is extended by the $\overline{CONVST}$ pulse width plus two CLK IN periods worst case. This is the maximum length of time for which $\overline{BUSY}$ can be low. Assuming a $\overline{CONVST}$ pulse width of two CLK IN periods and an 8 MHz CLK IN, the instruction cycle is extended by 500 ns maximum. Figure 9 shows the timing diagram for an extended read operation. In a similar manner, a write operation will be extended if it occurs during a $\overline{CONVST}$ pulse.

For processors that cannot be forced into a WAIT state, writing a logic 1 into DB5 of the status/control register allows the output latches to be enabled while $\overline{BUSY}$ is low. In this case $\overline{BUSY}$ still goes low as before, but it would not be used to stretch the read/write cycle and the instruction cycle continues as normal (see Figures 6 and 8).

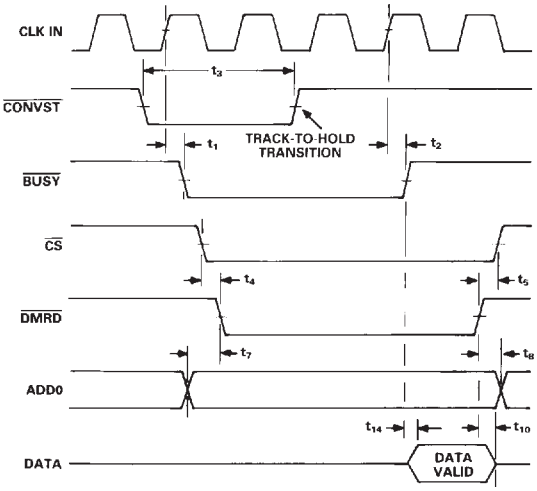


Figure 9. Extended Read Operation

AD7878 DYNAMIC SPECIFICATIONS

The AD7878 is specified and 100% tested for dynamic performance specifications rather than for traditional dc specifications such as Integral and Differential Nonlinearity. These ac specifications provide information on the AD7878's effect on the spectral content of the input signal. Hence, the parameters for which the AD7878 is specified include SNR, Harmonic Distortion, intermodulation Distortion and Peak Harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal-to-noise ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals (excluding dc) up to half the sampling frequency ($f_S/2$). SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-noise ratio for a sine wave input is given by

$$SNR = (6.02\ N + 1.76)\ dB \quad (1)$$

where N is the number of bits. Thus for an ideal 12-bit converter, SNR = 74 dB.

The output spectrum from the ADC is evaluated by applying a sine-wave signal of very low distortion to the V_{IN} input, which is sampled at a 100 kHz sampling rate. A Fast Fourier Transform (FFT) plot is generated from which the SNR data can be obtained. Figure 10 shows a typical 2048 point FFT plot of the AD7878KN with an input signal of 25 kHz and a sampling frequency of 100 kHz. The SNR obtained from this graph is 72.6 dB. It should be noted that the harmonics are included in the SNR calculation.

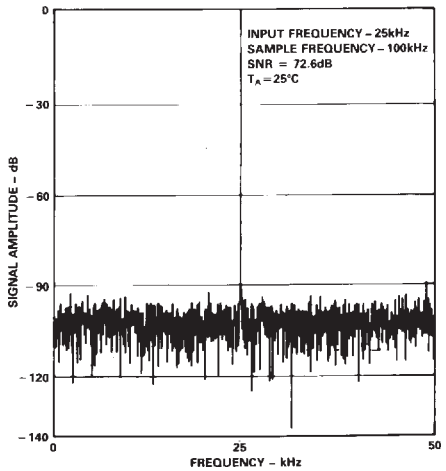


Figure 10. AD7878 FFT Plot

Effective Number of Bits

The formula given in (1) relates the SNR to the number of bits. Rewriting the formula, as in (2), it is possible to get a measure of performance expressed in effective number of bits (N). The effective number of bits for a device can be calculated directly from its measured SNR.

$$N = \frac{SNR - 1.76}{6.02} \quad (2)$$

Figure 11 shows a typical plot of effective number of bits versus frequency for an AD7878KN with a sampling frequency of 100 kHz. The effective number of bits typically falls between 11.7 and 11.85 corresponding to SNR figures of 72.2 and 73.1 dB.

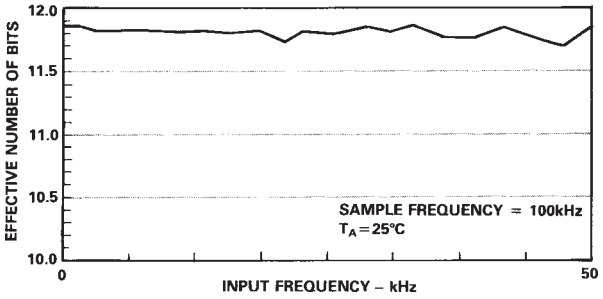


Figure 11. Effective Number of Bits vs. Frequency

Harmonic Distortion

Harmonic Distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7878, Total Harmonic Distortion (THD) is defined as:

$$THD = 20 \log \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second to the sixth harmonic. The *THD* is also derived from the FFT plot of the ADC output spectrum.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa + nfb where m, n = 0, 1, 2, 3 . . . . , etc. Intermodulation terms are those for which neither m nor n is equal to zero. For example, the second order terms include (fa + fb) and (fa – fb) while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

Using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Intermodulation distortion is calculated using an FFT algorithm but, in this case, the input consists of two equal amplitude, low distortion sine waves. Figure 12 shows a typical IMD plot for the AD7878.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to FS/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification will be determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor the largest peak will be a noise peak.

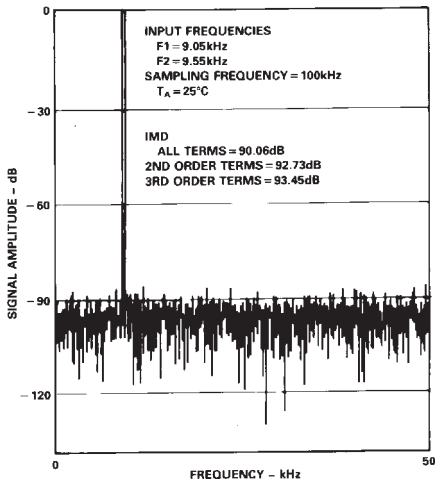


Figure 12. AD7878 IMD Plot

Histogram Plot

When a sine wave of a specified frequency is applied to the V_{IN} input of the AD7878 and several million samples are taken, it is possible to plot a histogram showing the frequency of occurrence of each of the 4096 ADC codes. If a particular step is wider than the ideal 1 LSB width, then the code associated with that step will accumulate more counts than for the code for an ideal step. Likewise, a step narrower than ideal will have fewer counts. Missing codes are easily seen in the histogram plot because a missing code means zero counts for a particular code. Large spikes in the plot indicate large differential nonlinearity.

Figure 13 shows a histogram plot for the AD7878KN with a sampling frequency of 100 kHz and an input frequency of 25 kHz. For a sine-wave input, a perfect ADC would produce a cusp probability density function described by the equation:

$$p(V) = \frac{1}{\pi\sqrt{(A^2 - V^2)}}$$

where A is the peak amplitude of the sine wave and $p(V)$ is the probability of occurrence at a voltage V. The histogram plot of Figure 13 corresponds very well with this cusp shape. The absence of large spikes in this plot indicates small dynamic differential nonlinearity (the largest spike in the plot represents less than 1/4 LSB of DNL error). The AD7878 has no missing codes under these conditions since no code records zero counts.

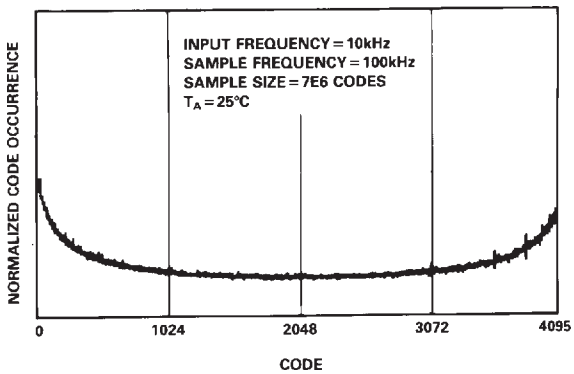


Figure 13. AD7878 Histogram Plot

CONVERSION TIMING

The track-and-hold on the AD7878 goes from track-to-hold mode on the rising edge of $\overline{\text{CONVST}}$, and the value of V_{IN} at this point is the value which will be converted. However, the conversion actually sorts on the next rising edge of CLK IN after $\overline{\text{CONVST}}$ goes high. If $\overline{\text{CONVST}}$ goes high within approximately 30 ns prior to a rising edge of CLK IN, that CLK IN edge will not be seen as the first CLK IN edge of the conversion process, and conversion will not actually start until one CLK IN cycle later. As a result, the conversion time (from $\overline{\text{CONVST}}$ to FIFO update) will vary by one clock cycle depending on the relationship between $\overline{\text{CONVST}}$ and CLK IN. A conversion cycle normally consists of 56 CLK IN cycles (assuming no read/write operations) which corresponds to a 7 As conversion time. If $\overline{\text{CONVST}}$ goes high within 30 ns prior to a rising edge of CLK IN, the conversion time will consist of 57 CLK IN cycles, i.e., 7.125 µs. This effect does not cause track/hold jitter.

INTERNAL REFERENCE

The AD7878 has an on-chip temperature compensated buried Zener reference (see Figure 14) that is factory trimmed to 3 V ± 1%. Internally, it provides both the DAC reference and the dc bias required for bipolar operation. The reference output is available (REF OUT) and is capable of providing up to 500 µA to an external load.

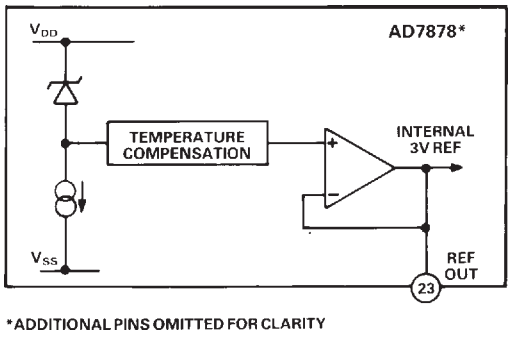


Figure 14. AD7878 Reference Circuit

The maximum recommended capacitance on REF OUT for normal operation is 50 pF. If the reference is required for use external to the AD7878, it should be decoupled with a 200 Ω resistor in series with a parallel combination of a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor. These decoupling components are required to remove voltage spikes caused by the internal operation of the AD7878.

TRACK-AND-HOLD AMPLIFIER

The track-and-hold amplifier on the analog input of the AD7878 allows the ADC to accurately convert an input sine wave of 6 V peak-peak amplitude to 12-bit accuracy. The input bandwidth of the track/hold amplifier is much greater than the Nyquist rate of the ADC even when operated at its minimum conversion time. The 0.1 dB cutoff frequency occurs typically at 500 kHz. The track/hold amplifier acquires an input signal to 12-bit accuracy in less than 2 µs.

The operation of the track/hold amplifier is transparent to the user. The track/hold amplifier goes from its tracking mode to its hold mode at the start of conversion on the rising edge of $\overline{\text{CONVST}}$ and returns to track mode at the end of conversion.

ANALOG INPUT

Figure 15 shows the AD7878 analog input. The analog input range is ±3 V into an input resistance of typically 15 kΩ. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . . FS–3/2 LSBs). The output code is 2s complement binary with 1 LSB = FS/4096 = 6 V/4096 = 1.46 mV. The ideal input/output transfer function is shown in Figure 16.

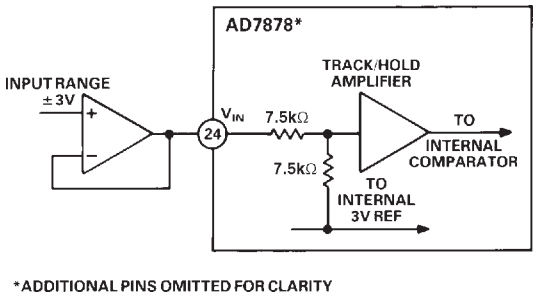


Figure 15. AD7878 Analog Input

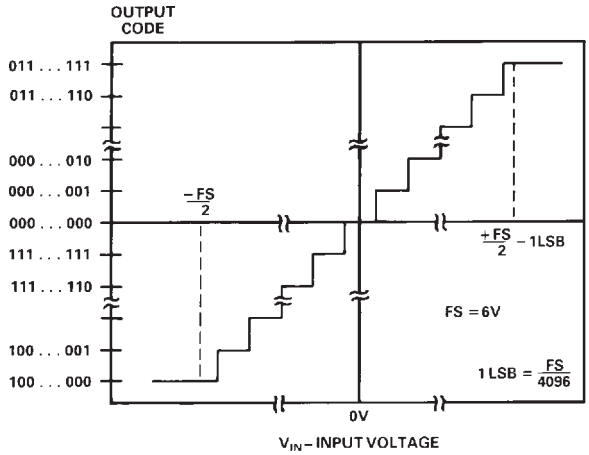


Figure 16. Input/Output Transfer Function

OFFSET AND FULL-SCALE ADJUSTMENT

In most Digital Signal Processing (DSP) applications offset and full-scale error have little or no effect on system performance. Offset error can always be eliminated in the analog domain by ac coupling. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. Some applications may require that the input signal span the full analog input dynamic range and, accordingly, offset and full-scale error will have to be adjusted to zero.

Where adjustment is required, offset must be adjusted before full-scale error. This is achieved by trimming the offset of the op amp driving the analog input of the AD7878 while the input voltage is 1/2 LSB below ground. The trim procedure is as follows: apply a voltage of –0.73 mV (–1/2 LSB) at V_1 and adjust the op amp offset voltage until the ADC output code flickers between 1111 1111 1111 and 0000 0000 0000.

Gain error can be adjusted at either the first code transition (ADC negative full scale) or the last code transition (ADC positive full scale). The trim procedures for both cases are as follows:

Positive Full-Scale Adjust
Apply a voltage of 2.9978 V (FS/2 – 3/2 LSBs) at V_1. Adjust R2 until the ADC output code flickers between 0111 1111 1110 and 0111 1111 1111.

Negative Full-Scale Adjust
Apply a voltage of –2.9993 V (–FS/2 + 1/2 LSB) at V_1 and adjust R2 until the ADC output code flickers between 1000 0000 0000 and 1000 0000 0001.

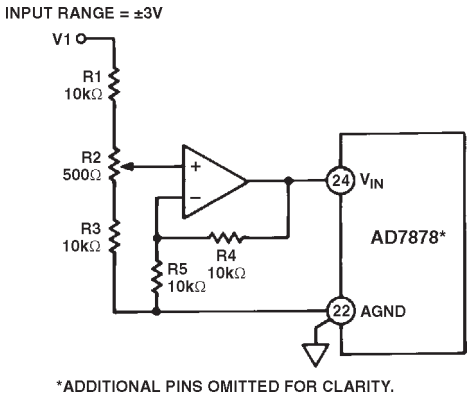


Figure 17. AD7878 Full-Scale Adjust Circuit

MICROPROCESSOR INTERFACING

The AD7878 high speed bus timing allows direct interfacing to DSP processors. Due to the complexity of the AD7878 internal logic, only synchronous interfacing is allowed. This means that the ADC clock must be the same as, or a derivative of, the processor clock. Suitable processor interfaces are shown in Figures 18 to 21.

AD7878–ADSP-2100/TMS32010/TMS32020

All three interfaces use an external timer for conversion control, allowing the ADC to sample the analog input asynchronously to the microprocessor. The AD7878 $\overline{ALFL}$ output interrupts the processor when the FIFO preprogrammed word count is reached. The processor then reads the conversion results from the AD7878 internal FIFO memory.

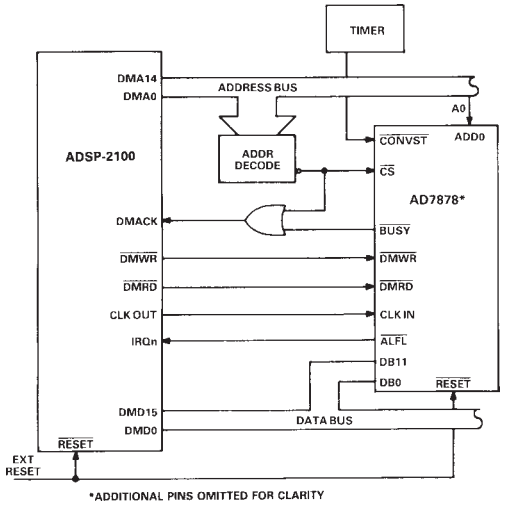


Figure 18. AD7878–ADSP-2700 Interface

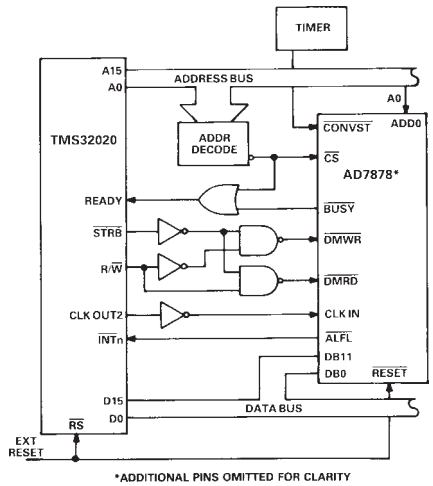


Figure 19. AD7878–TMS32020 Interface

The interfaces to the ADSP-2100 and the TMS32020 gate the AD7878 $\overline{CS}$ and the $\overline{BUSY}$ to provide a signal which drives the processor into a wait state if a read/write operation to the ADC is attempted while the ADC track/hold amplifier is going from the track to the hold mode. This avoids digital feedthrough to the analog circuitry. The TMS32020 does not have separate $\overline{RD}$ and $\overline{WR}$ outputs to drive the AD7878 $\overline{DMWR}$ and $\overline{DMRD}$ inputs. These are generated from the processor $\overline{STRB}$ and R/$\overline{W}$ outputs with the addition of some logic gates.

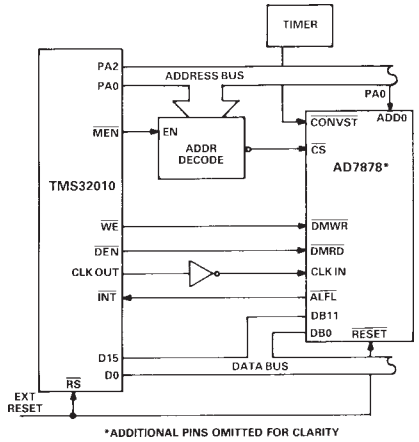


Figure 20. AD7878–TMS32020 Interface

AD7878–M CC8000

This interface also uses an external timer for conversion control as described for the previous three interfaces. It is discussed separately because it needs extra logic due to the nature of its interrupts. The MC68000 has eight levels of external interrupt. When interrupting this processor one of these levels (0 to 7) has to be encoded onto the $\overline{IPL2}$–$\overline{IPL0}$ inputs. This is achieved with a 74148 encoder in Figure 21, (interrupt Level 1 is taken for example purposes only). The MC68000 places this interrupt level on address bits A3 to A1 at the start of the interrupt service routine. Additional logic is used to decode this interrupt level on the address bus and the FC2–FC0 outputs to generate a $\overline{VPA}$ signal for the MC68000. This results in an autovectored interrupt, the start address for the service routine must be loaded into the appropriate auto vector location during initialization. For further information on the 68000 interrupts consult the 68000 *User's Manual.*

The MC68000 $\overline{AS}$ and R/$\overline{W}$ outputs are used to generate separate $\overline{DMWR}$ and $\overline{DMRD}$ inputs for the AD7878. As with the three interfaces previously described, WAIT states are inserted if a read/write operation is attempted while the track/hold amplifier is going from the track to the hold mode.

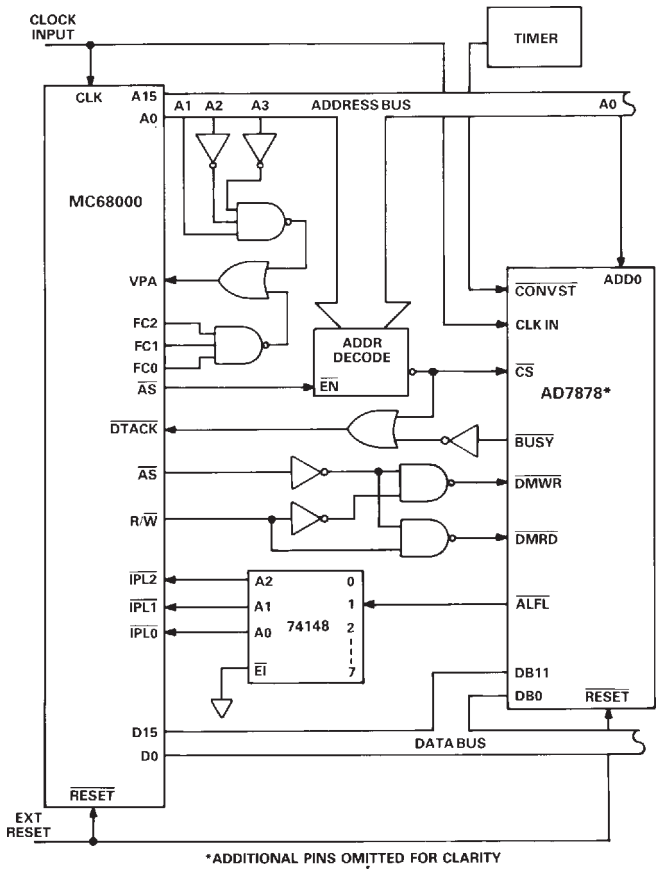


Figure 21. AD7878–MC68000 Interface

Typical AD7878 Microprocessor Operating Sequence

After power-up or reset, the status/control register is initialized by writing to the AD7878. This enables the $\overline{ALFL}$ output if required for a microprocessor interrupt and sets the effective word length of the FIFO memory. The processor now executes the main body of the program while waiting for an ADC interrupt. This interrupt will occur when the preprogrammed number of samples are collected in the FIFO memory. The interrupt service routine first interrogates DB5(FOOR) of the status/control register to determine if any sample in the FIFO memory is out of range. If all data samples are valid, then the program proceeds to read the FIFO memory. If, on the other hand, at least one sample is out of range, then an overrange routine is called.

There are many actions that can be taken by the out of range routine, the selection of which is application dependent. One option is to ignore all the current samples residing in the FIFO memory, reinitialize the status/control register and return to the main body of the program. Another option is to check the individual out of range status of each word in the FIFO memory and to discard the invalid ones. The underrange or overrange status of each word can also be determined and the analog input adjusted accordingly before returning to the main program.

Note: there is no need to check the out-of-range status if the analog input is always assured to be within range.

THROUGHPUT RATE

The AD7878 has a maximum specified throughput rate (sample rate) of 100 kHz. This is a worst-case test condition and specifications apply for reduced sampling rates, provided that Nyquist criterion is obeyed. The throughput rate must take into account ADC $\overline{CONVST}$ pulse width, ADC conversion time and the track/hold amplifier acquisition time. The time required for each of these tasks is shown in Table II for a selection of DSP processors. Since the ADC clock has to be synchronized to the microprocessor dock, the conversion time depends on the microprocessor used. In addition, time must be allowed for reading data from the AD7878. If this task is performed during the track/hold amplifier acquisition period, then it does not impact the overall throughput rate. However, if the read operations occur during a conversion, they may stretch the conversion time and reduce the track/hold amplifier acquisition time. The track/hold amplifier requires a minimum of 2 µs to operate to specification. The time required to read from the AD7878 depends on the number of FIFO memory locations to be read and the software organization.

As an example, consider an application using the ADSP-2100 and the AD7878 with a throughput rate of 100 kHz. The time required for the $\overline{CONVST}$ pulse and the ADC conversion is 7.375 µs. This leaves 2.625 µs for the track/hold acquisition time and for reading the ADC (both operations occurring in parallel). The ADSP-2100, when operating from a 32 MHz clock, has an instruction cycle of 125 ns and an interrupt response time of 500 ns. This allows adequate time to perform 16 read operations within the time budget allowed.

Table II. AD7878 Throughput Rate

	$\overline{CONVST}$ Pulse Width	Conversion Time	T/H Acquisition Time
Number of Clock Cycles	2 min	57 max	Non-Applicable
ADSP-2100[1]	250 ns min	7.125 µs max	2 µs min
TMS32010[2]	400 ns min	11.14 µs max	2 µs min
TMS32020[2]	400 ns min	11.14 µs max	2 µs min

NOTES
[1]ADSP-2100 Clock Frequency = 32 MHz.
[2]TMS320XX Clock Frequency = 20 MHz.

APPLICATION HINTS

Good printed circuit board (PCB) layout is as important as the overall circuit design itself in achieving high speed A/D performance. The AD7878 is required to make bit decisions on an LSB size of 1.465 mV. To achieve this, the designer has to be conscious of noise both in the ADC itself and in the preceding analog circuitry. Switching mode power supplies are not recommended as the switching spikes will feed through to the comparator, causing noisy code transitions. Other concerns are ground loops and digital feedthrough from microprocessors. These factors influence any ADC, and a proper PCB layout that minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Guard (screen) the analog input with AGND.

Establish a single point analog ground (star ground) separate from the logic system ground at Pin 22 (AGND) or as dose as possible to the AD7878, as shown in Figure 22. Connect all other grounds and Pin 7 (AD7878 DGND) to this single analog ground point. Do not connect any other digital grounds to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC, so make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise. The circuit layouts of Figures 25 and 26 have both analog and digital ground planes, which are kept separated and only joined together at the AD7878 AGND pin.

NOISE

Keep the input signal leads to V_{IN} and signal return leads from AGND (Pin 22) as short as possible to minimize input noise coupling. In applications where this is not possible, use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

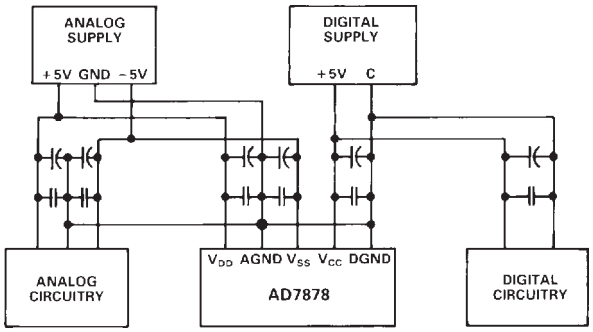


Figure 22. Power Supply Grounding Practice

DATA ACQUISITION BOARD

Figure 23 shows the AD7878 in a data acquisition circuit that will interface directly to either the ADSP-2100, TMS32010 or the TMS32020. The corresponding printed circuit board (PCB) layout and silkscreen are shown in Figures 24 to 26.

The only additional component required for a full data acquisition system is an antialiasing filter. There is a component grid provided near the analog input on the PCB which may be used for such a filter or any other conditioning circuitry. To facilitate this option, a wire link (labelled LK1 on the PCB) is required on the analog input track. This link connects the input signal to either the component grid or directly to the buffer amplifier driving the AD7878 analog input.

Microprocessor connections to the PCB can be made by either of two ways:

1. 96-contact (3 ROW) Eurocard connector.
2. 26-contact (2 ROW) IDC connector.

The 96-contact Eurocard connector is directly compatible with the ADSP-2100 Evaluation Board Prototype Expansion Connector. The expansion connector on the ADSP-2100 has eight decoded drip enable outputs labelled $\overline{ECE8}$ to $\overline{ECE1}$. $\overline{ECE6}$ is used to drive the AD7878 $\overline{CS}$ input on the data acquisition board. To avoid selecting onboard RAM sockets at the same time, LK6 on the ADSP-2100 board must be removed. In addition, the expansion connector on the ADSP-2100 has four interrupts labelled $\overline{EIRQ3}$ to $\overline{EIRQ0}$. The AD7878 $\overline{ALFL}$ output connects to $\overline{EIRQ0}$. The AD7878 and ADSP-2100 data lines are aligned for left justified data transfer.

The 26-way IDC connector contains all the necessary contacts for both the TMS32010 and TMS32020. There are two switches on the data acquisition board that must be set to enable the appropriate interface configuration (see Table III). The interface connections for the TMS32010/32020 and IDC signal contact numbers are shown in Table IV and Figure 23. Note the AD7878 CS input must be decoded from the address bus prior to the AD7878 evaluation board for the TMS320XX interfaces.

Connections to the analog input (V_{IN}) and the $\overline{CONVST}$ input are made via two BNC sockets labelled SKT1 and SKT2 on the silkscreen. If the $\overline{CONVST}$ input is derived from either the microprocessor or ADC clock, the effects of clock noise coupling will be reduced.

Table III. AD7878 PCB Switch Settings

SWITCH SETTING

Microprocessor	SW1	SW2
ADSP-2100	A	A
TMS32010	B	A
TMS32020	B	B

POWER SUPPLY CONNECTIONS

The PCB requires two analog supplies and one 5 V digital supply. Connections to the analog supplies are made directly to the PCB as shown on the silk screen in Figure 24. The connections are labelled V+ and V– and the range for both of these supplies is 12 V to 15 V. Connection to the 5 V digital supply is made through either of the two microprocessor connectors. The +5 V and –5 V analog power supplies required by the AD7878 are generated from two voltage regulators on the V+ and V– power supply inputs (IC3 and IC4 in Figure 23).

COMPONENT LIST

IC1	AD711 Op Amp
IC2	AD7878 Analog-to-Digital Converter
IC3	MC78L05 5 V Regulator
IC4	MC79L05 –5 V Regulator
IC5*	74HC00 Quad NAND Gate
IC6*	74HC04 Hex Inverter
IC7	74HC02 Quad NOR Gate
SW1	Single Pole Double Throw
SW2	Double Pole Double Throw
LK1	Wire Link for Analog Input
C1, C3, C5, C7, C9 C11, C13, C15	10 µF Capacitors
C2, C4, C6, C8, C10 C12, C14, C16	0.1 µF Capacitors
R1*, R2*	10 kΩ Resistors
SKT1, SKT2	BNC Sockets
SKT3	26-Contact (2 Row) IDC Connector
SKT4	96-Contact (3 Row) Eurocard Connector

*Not required for ADSP-2100 Interface.

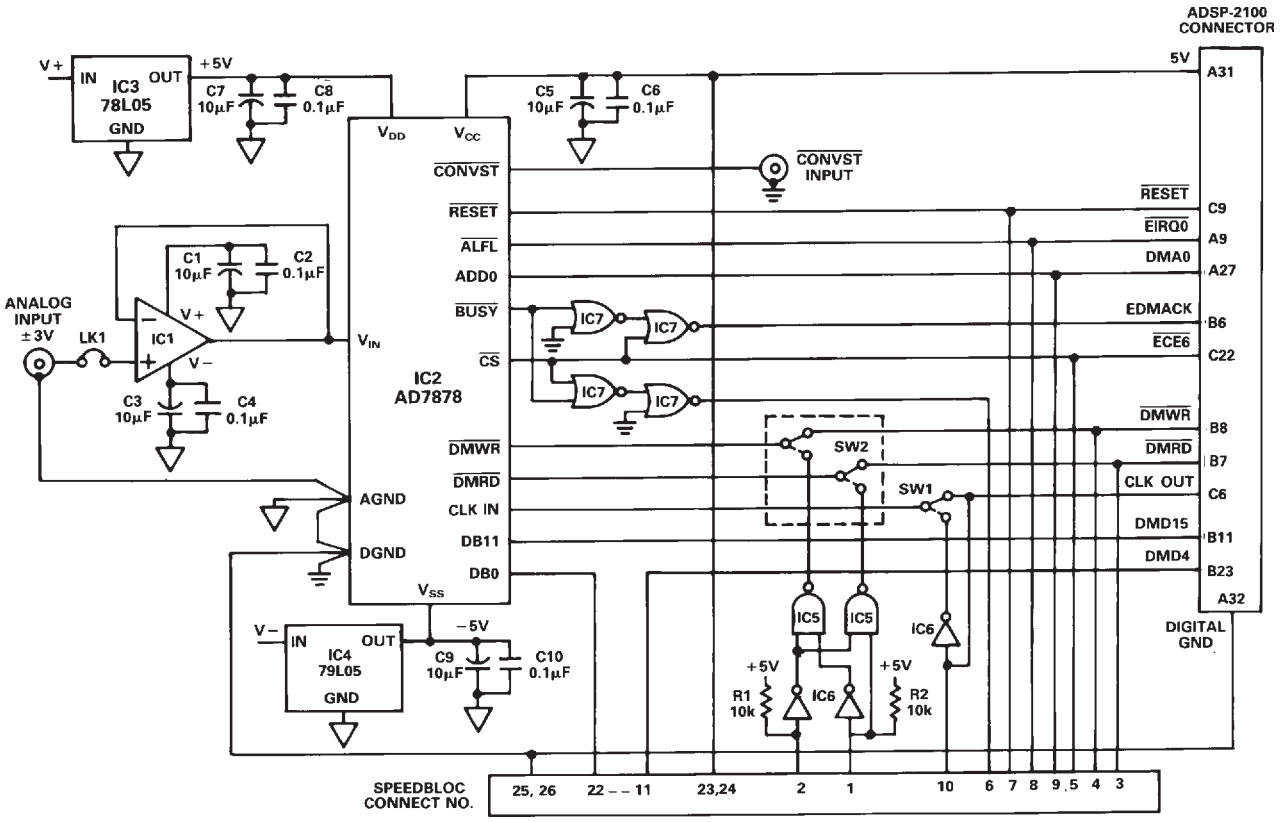


Figure 23. Data Acquisition Circuit Using the AD7878

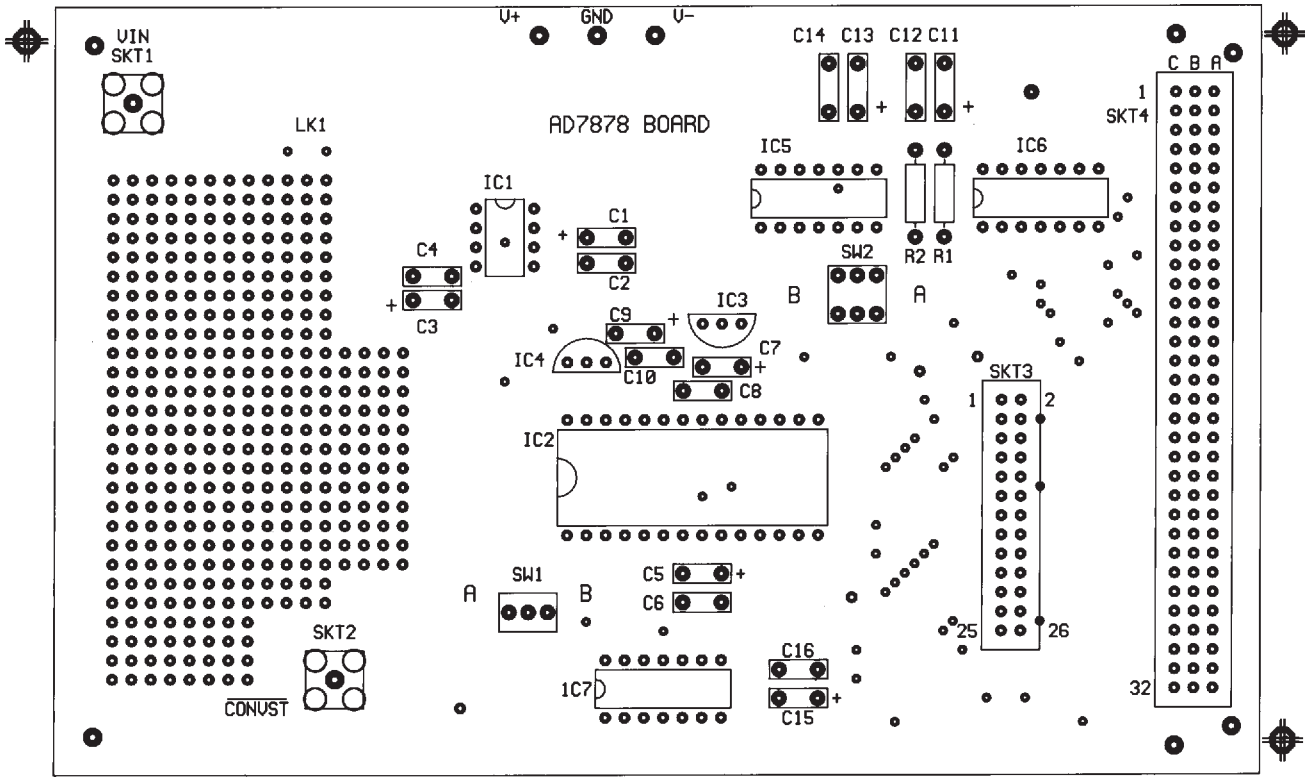


Figure 24. PCB Silkscreen for Figure 23

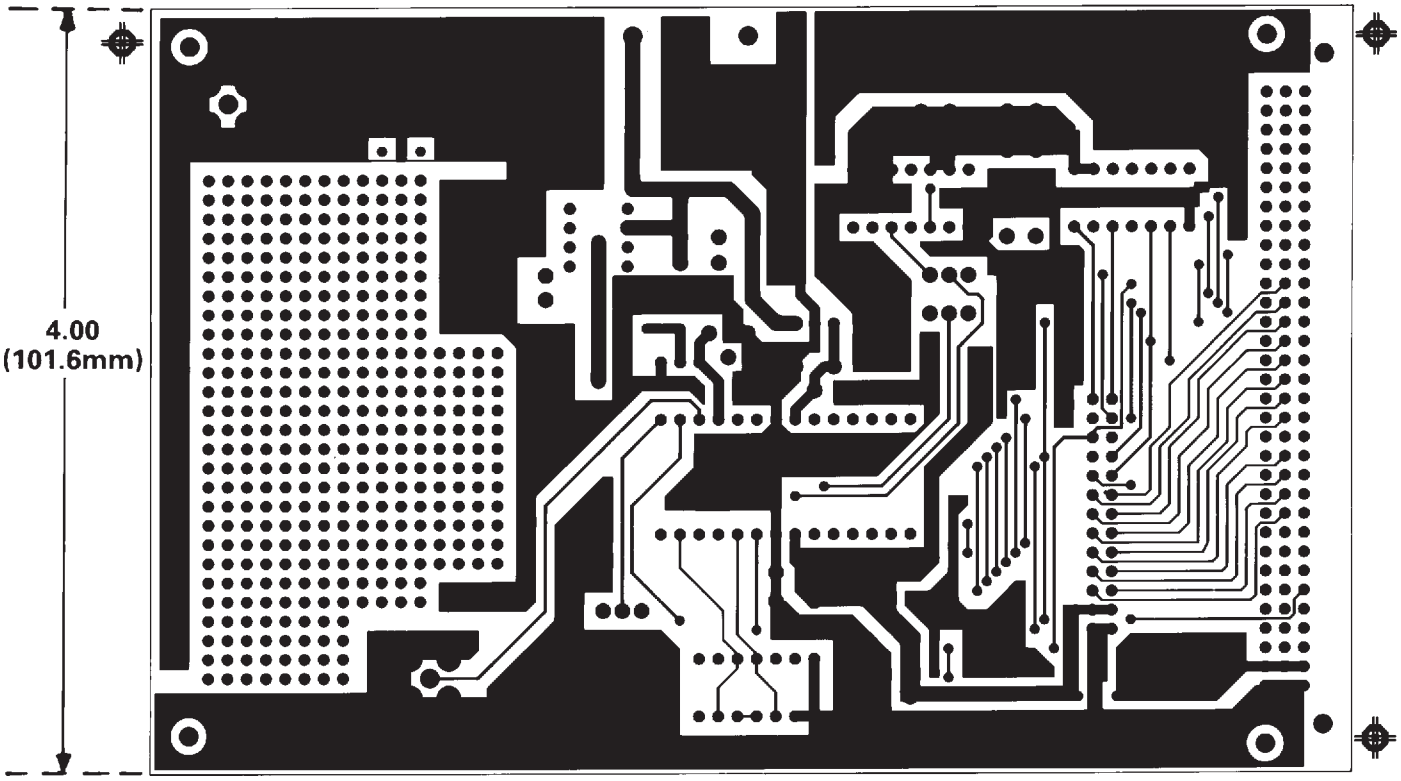


Figure 25. PCB Component Side Layout for Figure 23

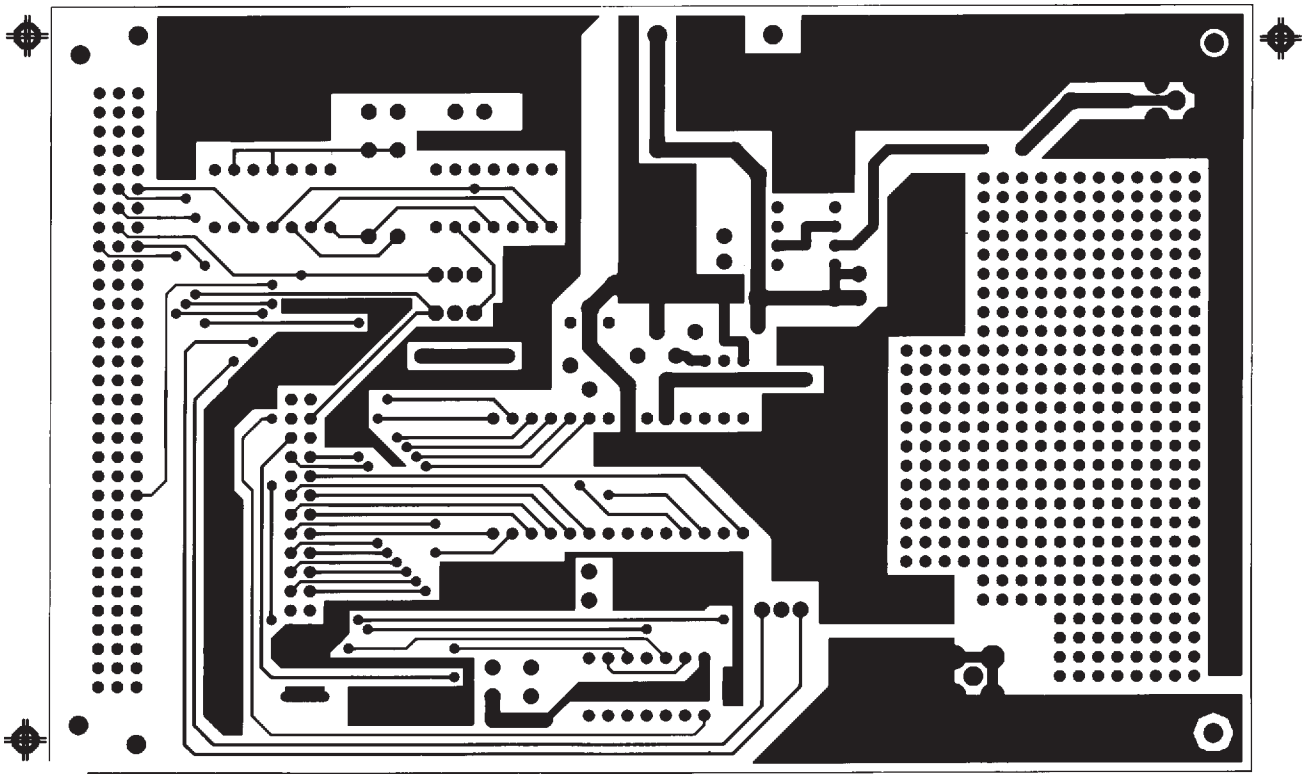


Figure 26. PCB Solder Side Layout for Figure 23

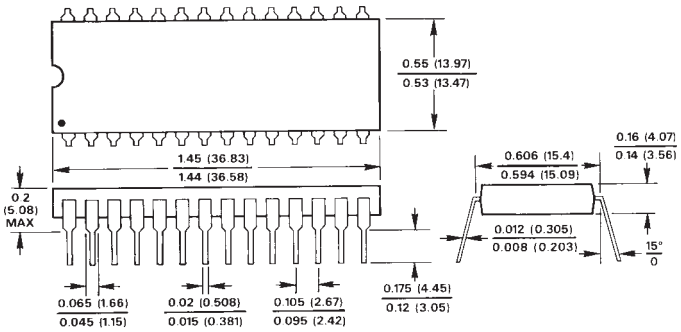
Table IV. TMS32010/TMS32020 Interface Connections

IDC Contact No.	Signal Connect Mnemonic	TMS32010 Signal	TMS32020 Signal
1	R/$\overline{W}$	—	R/$\overline{W}$
2	$\overline{STRB}$	—	$\overline{STRB}$
3	$\overline{DMRD}$	$\overline{DEN}$	—
4	$\overline{DMWR}$	$\overline{WE}$	—
5	$\overline{CS}$	$\overline{CS}$	$\overline{CS}$
6	READY	—	READY
7	$\overline{RESET}$	$\overline{RESET}$	$\overline{RESET}$
8	$\overline{ALFL}$	$\overline{INT}$	$\overline{INT}$
9	ADD0	PA0	A0
10	CLK	CLKOUT	CLKOUT2
11	DB10	D10	D10
12	DB11	D11	D11
13	DB8	D8	D8
14	DB9	D9	D9
15	DB6	D6	D6
16	DB7	D7	D7
17	DB4	D4	D4
18	DB5	D5	D5
19	DB2	D2	D2
20	DB3	D3	D3
21	DB0	D0	D0
22	DB1	D1	D1
23	5 V	5 V	5 V
24	5 V	5 V	5 V
25	GND	GND	GND
26	GND	GND	GND

OUTLINE DIMENSIONS

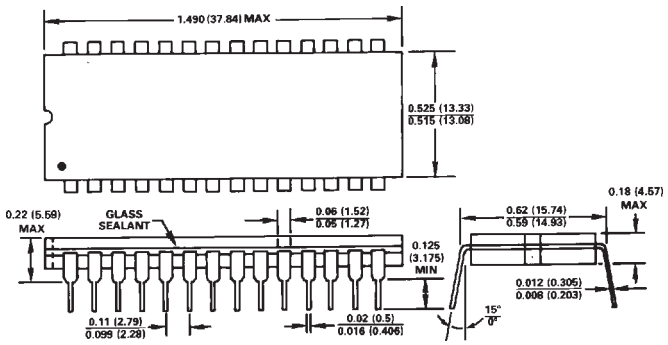
Dimensions shown in inches and (mm).

28-Pin Plastic DIP (N-28)



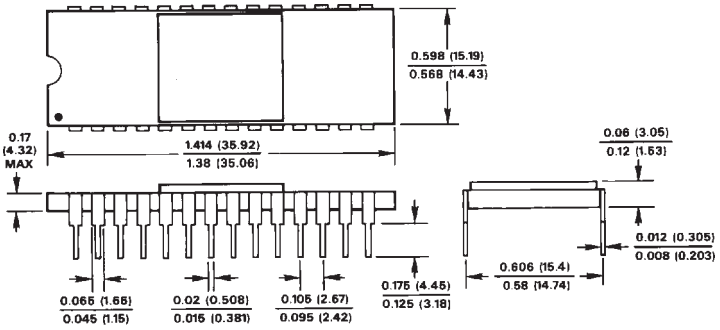
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42

28-Pin Cerdip (Q-28)



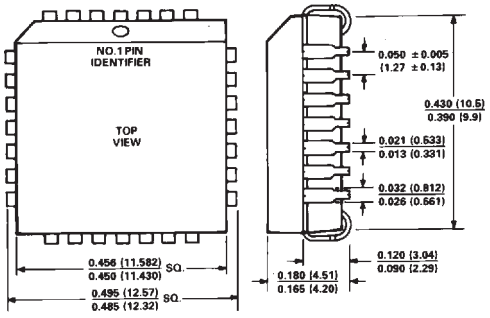
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42

28-Pin Ceramic DIP (D-28)

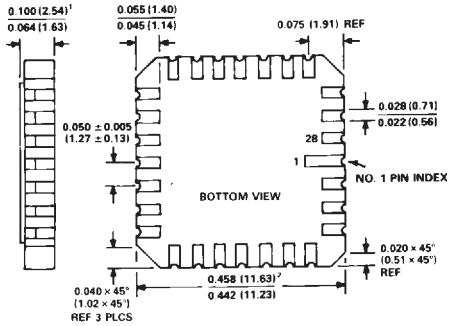


LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

28-Terminal PLCC (P-28A)



28-Terminal LCCC (E-28A)



NOTES
[1] THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS.
[2] APPLIES TO ALL FOUR SIDES.
ALL TERMINALS ARE GOLD PLATED.

NOTE

[1]Analog Devices reserves the right to ship either cerdip or ceramic hermetic

C1204a–1–5/97

PRINTED IN U.S.A.