CMOS LSI

No. 4366B

LC79401D

Dot-Matrix LCD Driver

Overview

The LC79401D is a segment driver LSI for use with large scale dot-matrix LCD displays. The LC79401D latches 80 bits of display data sent from a controller using a 4-bit parallel transfer technique and generates LCD drive signals. When combined as a kit with a common driver, either the LC7943D (QIP80D), the LC79430D (QIP100D), or the LC79431D (QIP100D), the LC79401D can drive large screen LCD panels.

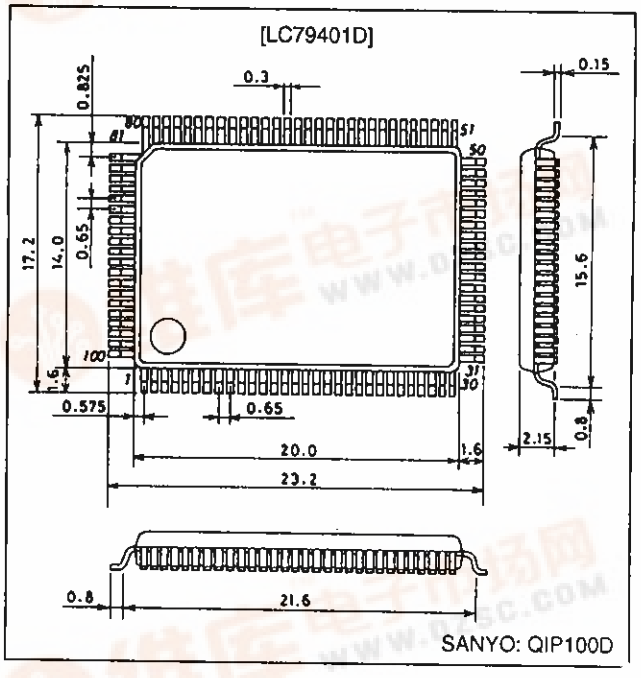
Features

- Incorporates LCD drive circuits for 80 bits of display
- Supports display duties from 1/64 to 1/256
- The provision of a chip disable pin supports power reduction in large-scale panels.
- Allows external provision of the bias power supply
- Operating supply voltage/operating temperature
  V_{DD} (logic block): 5 V ±10%/–20 to +75°C
  V_{DD}-V_{EE} (LCD block): 12 to 32 V/–20 to +75°C
- Data transfer clock: 6.0 MHz (max), bidirectional shifting supported
- Data input: 4-bit parallel input
- CMOS process
- 100-pin flat plastic package

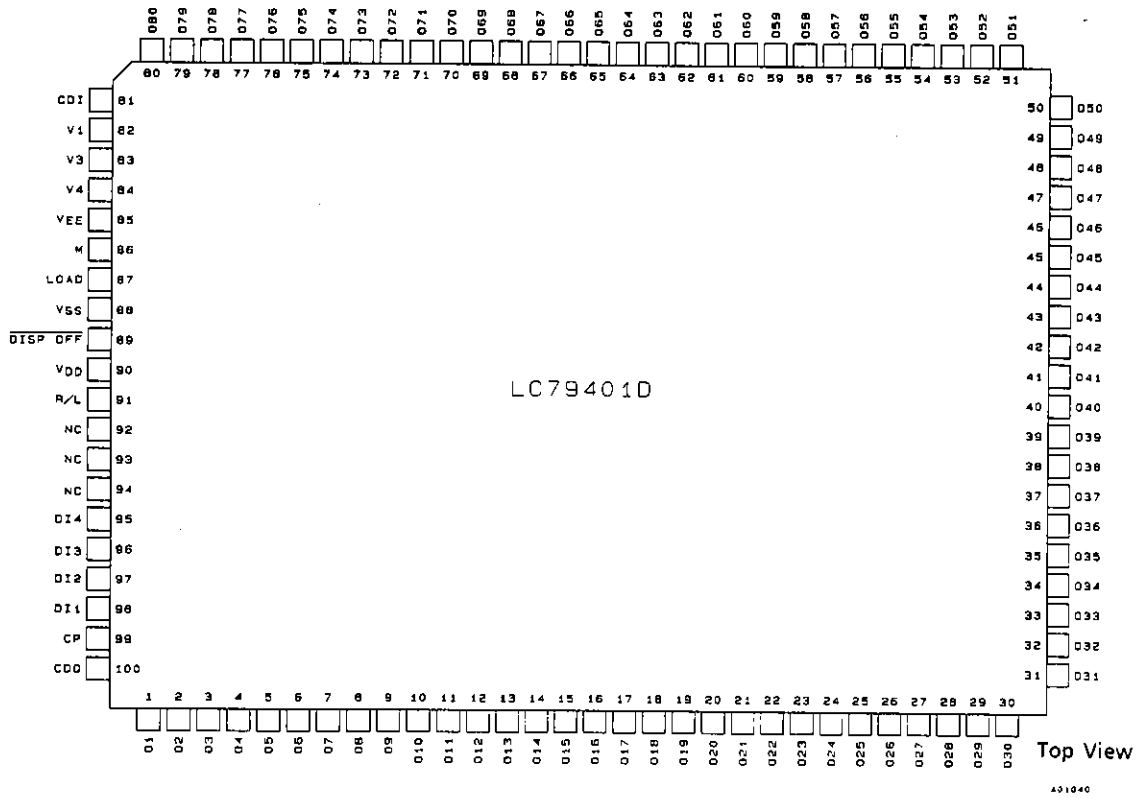
Package Dimensions

unit: mm

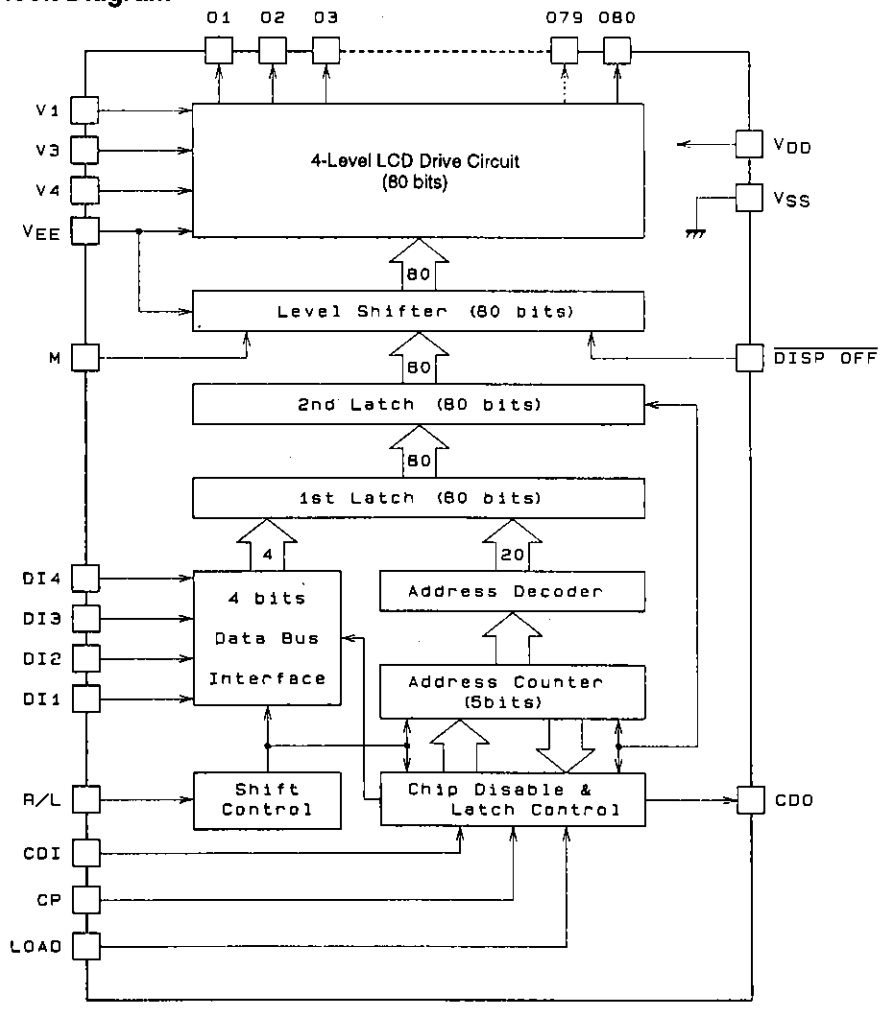
3180-QIP100D



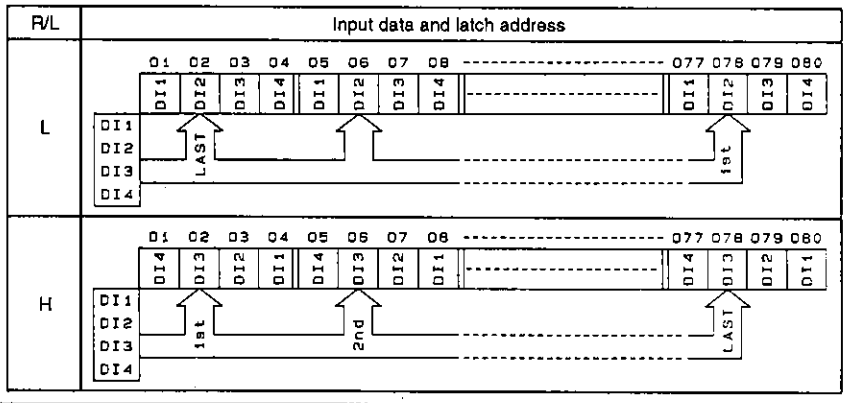
Pin Assignment



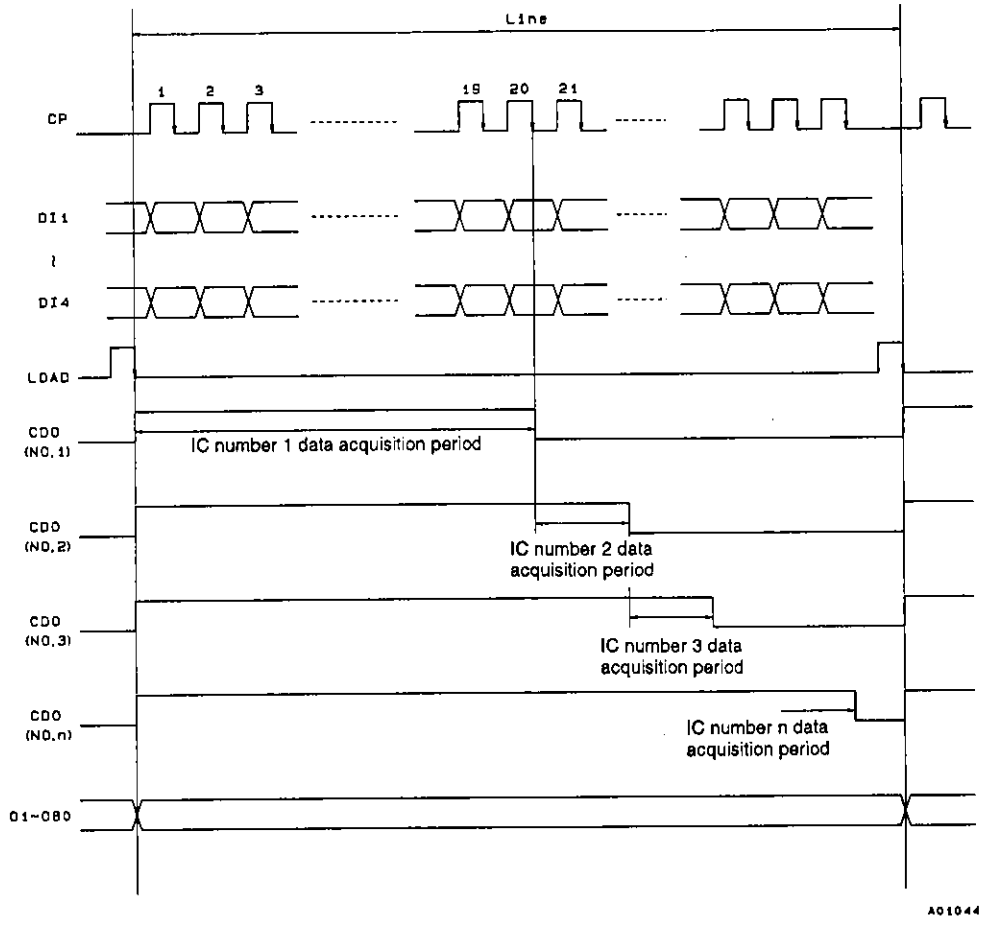
Equivalent Circuit Block Diagram



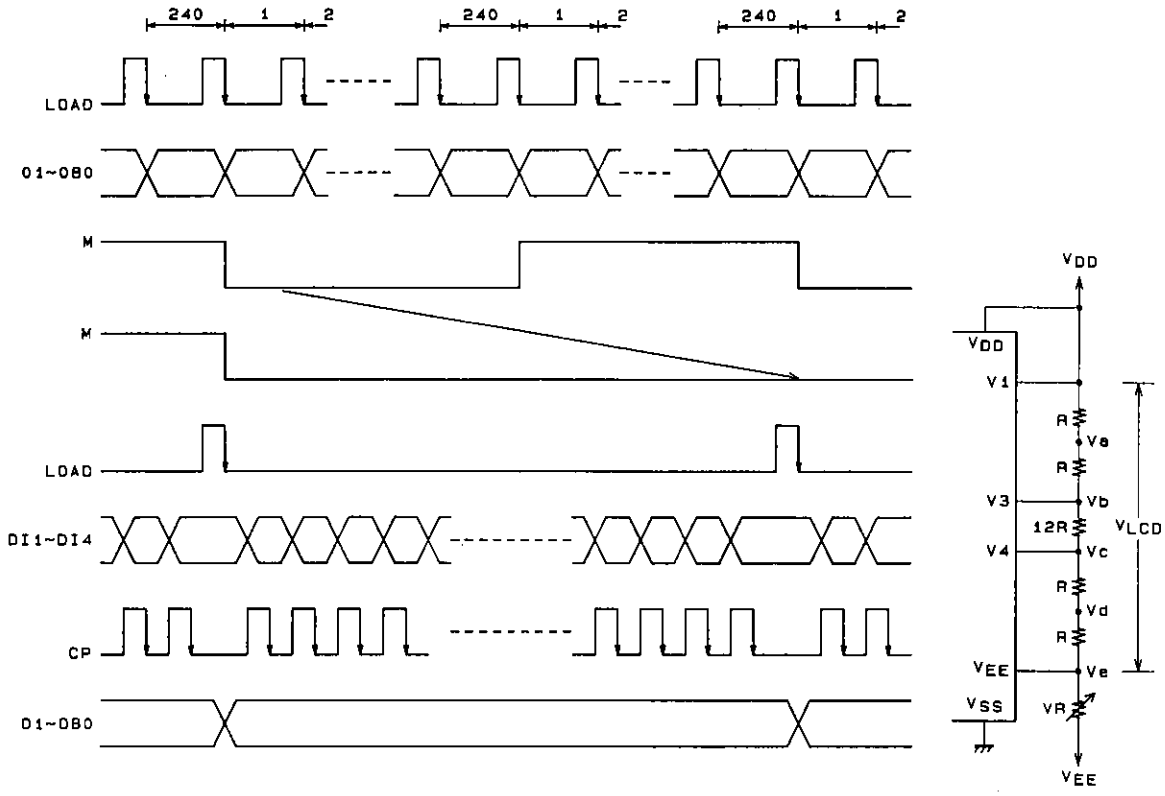
Pin Functions

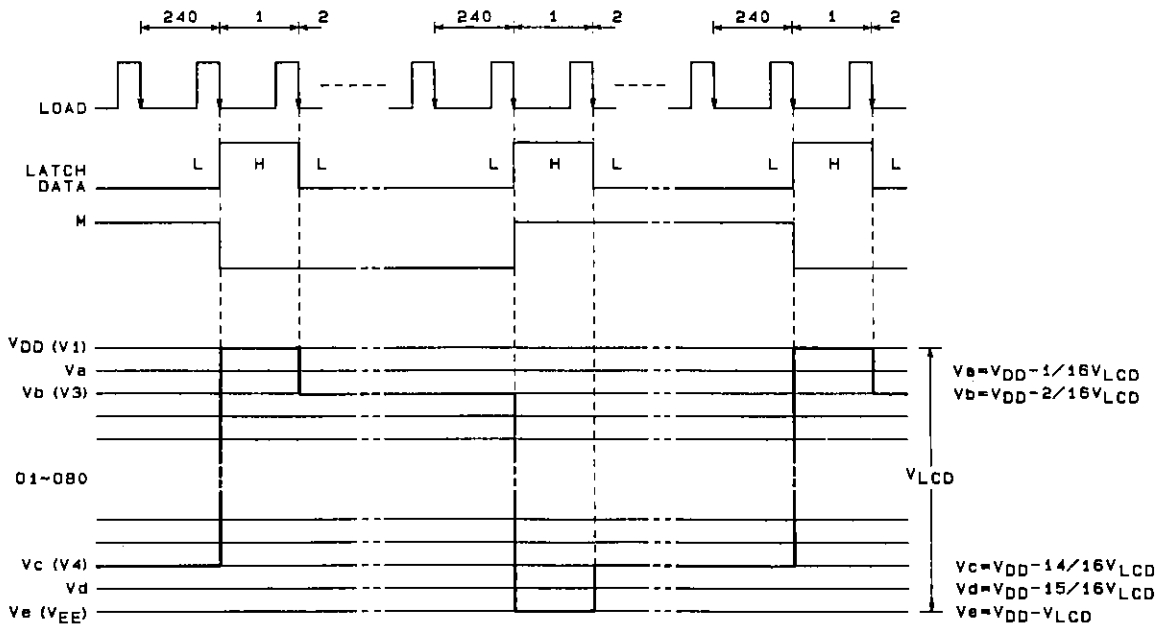
<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>90
88
85</td><td>V_{DD}
V_{SS}
V_{EE}</td><td>Power supply</td><td>V_{DD}-V_{SS}: Logic power supply
V_{DD}-V_{EE}: LCD drive circuit power supply</td></tr>
<tr><td>82
83
84</td><td>V1
V3
V4</td><td>Power supply</td><td>LCD drive level power supply
V1, V_{EE}: Selected level
V3, V4: Unselected level</td></tr>
<tr><td>99</td><td>CP</td><td>Input</td><td>Display data acquisition clock (falling edge trigger)</td></tr>
<tr><td>87</td><td>LOAD</td><td>Input</td><td>Display data latch clock (falling edge trigger)
The display data LCD drive signal is output on the falling edge.</td></tr>
<tr><td>95
96
97
98</td><td>DI4
DI3
DI2
DI1</td><td>Input</td><td><table><tr><th>Display data</th><th>LCD drive output</th><th>LCD display</th></tr><tr><td>H</td><td>Selected level</td><td>On</td></tr><tr><td>L</td><td>Unselected level</td><td>Off</td></tr></table></td></tr>
<tr><td>91</td><td>R/L</td><td>Input</td><td>Control pin that inverts the data output destination
 
</td></tr>
<tr><td>86</td><td>M</td><td>Input</td><td>LCD drive output alternation signal</td></tr>
<tr><td>81</td><td>CDI</td><td>Input</td><td>Chip disable pin
High level: Data is not acquired
Low level: Data is acquired.</td></tr>
<tr><td>100</td><td>CDO</td><td>Output</td><td>Connect to the CDI pin on the next chip when cascade connection is used.</td></tr>
<tr><td>89</td><td>$\overline{\text{DISP OFF}}$</td><td>Input</td><td>Input that controls the O1 to O80 output pins. During periods when this pin is low, the O1 to O80 output pins output the V1 level. See the truth table.</td></tr>
<tr><td>1 to 80</td><td>O1 to O80</td><td>Output</td><td>LCD drive outputs
The output levels are determined by the combination of the output data, the M signal, and the $\overline{\text{DISP OFF}}$ pin as shown in the table.
<table><tr><th>M</th><th>Q</th><th>$\overline{\text{DISP OFF}}$</th><th>Output</th></tr><tr><td>L</td><td>L</td><td>H</td><td>V3</td></tr><tr><td>L</td><td>H</td><td>H</td><td>V1</td></tr><tr><td>H</td><td>L</td><td>H</td><td>V4</td></tr><tr><td>H</td><td>H</td><td>H</td><td>V_{EE}</td></tr><tr><td>*</td><td>*</td><td>L</td><td>V1</td></tr></table>Note: Don't care (fixed at high or low)</td></tr>
<tr><td>92
93
94</td><td>NC</td><td>—</td><td>Must be left open.</td></tr>
</table>

Output Timing



Timing Chart (1/240 duty, 1/16 bias)





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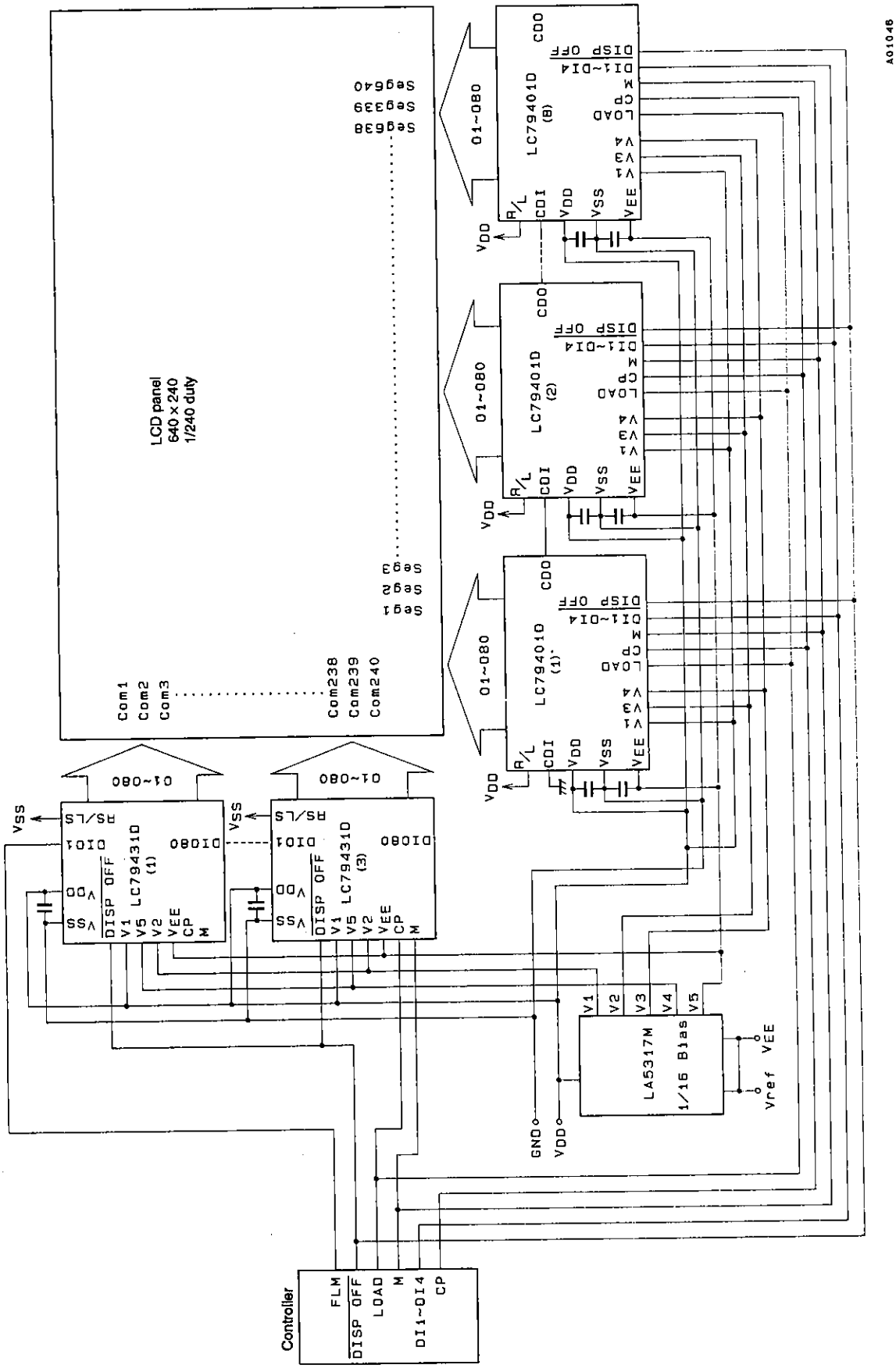
Sample Application Circuit



Specifications

Absolute Maximum Ratings at Ta = 25 ±2°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage (logic)	V_{DD} max		–0.3 to +7.0	V
Maximum supply voltage (LCD)	V_{DD}-V_{EE} max	*1	0 to 35	V
Maximum input voltage	V_I max		–0.3 to V_{DD} + 0.3	V
Storage temperature	Tstg		–40 to +125	°C

Note: 1. $V_{DD} \geq V1 > V3 > V4 > V_{EE}$

Allowable Operating Ranges at Ta = –20 to +75°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage (logic)	V_{DD}		4.5		5.5	V
Supply voltage (LCD)	V_{DD}-V_{EE}	*2, 3	12		32	V
Input high level voltage	V_{IH}	DI1 to DI4, CP, LOAD, CDI, R/L, M, $\overline{\text{DISP OFF}}$	0.8 V_{DD}			V
Input low level voltage	V_{IL}	DI1 to DI4, CP, LOAD, CDI, R/L, M, $\overline{\text{DISP OFF}}$			0.2 V_{DD}	V
CP (shift clock)	f_{CP}	CP			6.0	MHz
CP pulse width	t_{WC}	CP	50			ns
LOAD pulse width	t_{WL}	LOAD	50			ns
Setup time	t_{SETUP}	DI1 to DI4 → CP	30			ns
Hold time	t_{HOLD}	DI1 to DI4 → CP	30			ns
CP → LOAD	t_{CL}	CP → LOAD	80			ns
LOAD → CP	t_{LC}	LOAD → CP	110			ns
CP and LOAD rise time	t_R	CP, LOAD			*4	ns
CP and LOAD fall time	t_F	CP, LOAD			*4	ns

Note: 2. $V_{DD} \geq V1 > V3 > V4 > V_{EE}$
3. When the power is turned on, either the logic system power must be turned on before the LCD drive system power or else they must both be turned on at the same time. When the power is turned off, either the LCD drive system power must be turned off before the logic system power, or else both must be turned off at the same time.
4. The CP and LOAD rise time (t_R) and the CP and LOAD fall time (t_F) must satisfy equations ① and ② below at the same time.
① $t_R, t_F < \frac{1}{2\,fCP} - t_{WC}$
② $t_R, t_F < 50$ ns

Electrical Characteristics at Ta = 25°C ± 2°C, V_{DD} = 5 V ± 10%

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high level current	I_{IH}	$V_{IN} = V_{DD}$: LOAD, CP, CDI, R/L, DI1 to DI4, M, $\overline{\text{DISP OFF}}$			1	μA
Input low level current	I_{IL}	$V_{IN} = V_{SS}$: LOAD, CP, CDI, R/L, DI1 to DI4, M, $\overline{\text{DISP OFF}}$	–1			μA
Output high level voltage	V_{OH}	I_{OH} = –400 μA: CDO	V_{DD} – 0.4			V
Output low level voltage	V_{OL}	I_{OL} = 400 μA: CDO			0.4	V
Driver on resistance	R_{ON} (1)	V_{DD}-V_{EE} = 30 V, | V_{DE}-V_O | = 0.5 V: O1 to O80*5		1.5	3.0	kΩ
	R_{ON} (2)	V_{DD}-V_{EE} = 20 V, | V_{DE}-V_O | = 0.5 V: O1 to O80*5		2.0	3.5	kΩ
Standby current drain	I_{ST}	CDI = V_{DD}, V_{DD}-V_{EE} = 30 V, CP = 6.0 MHz, output unloaded: V_{SS}			200	μA
operating current drain	I_{SS}*6	V_{DD}-V_{EE} = 30 V, CP = 6 MHz, LOAD = 14 kHz, M = 35 Hz: V_{SS}			4.0	mA
	I_{EE}*7	V_{DD}-V_{EE} = 30 V, CP = 6 MHz, LOAD = 14 kHz, M = 35 Hz: V_{EE}			0.5	mA
Input capacitance	CI	f = 6.0 MHz: CP		5		pF

Note: 5. V_{DE} = one of V1, V3, V4 or V_{EE}. V1 = V_{DD}, V3 = 15/17 (V_{DD}-V_{EE}), V4 = 2/17 (V_{DD} - V_{EE})
6. I_{SS} is the current flowing from V_{DD} to V_{SS}.
7. I_{EE} is the current flowing from V_{DD} to V_{EE}.

Switching Characteristics at Ta = 25°C ± 2°C, V_{SS} = 0 V, V_{DD} = 5 V ± 10%

Parameter	Symbol	Conditions	min	typ	max	Unit
Output delay time	t_D	Load = 15 pF: CDO			80	ns

Switching Characteristics Diagram