

Ordering number : EN5682

CMOS LSI



LC7972VA, 7972VB

CMOS Operational Amplifier with Programmable Offset Correction Function

Overview

The LC7972VA and LC7972VB are dual inverting/noninverting operational amplifier ICs that are fabricated in a CMOS process. These ICs provide a programmable offset correction function and a power saving function for use when the operational amplifier is unused, both of which can be controlled from a microprocessor interface.

Features

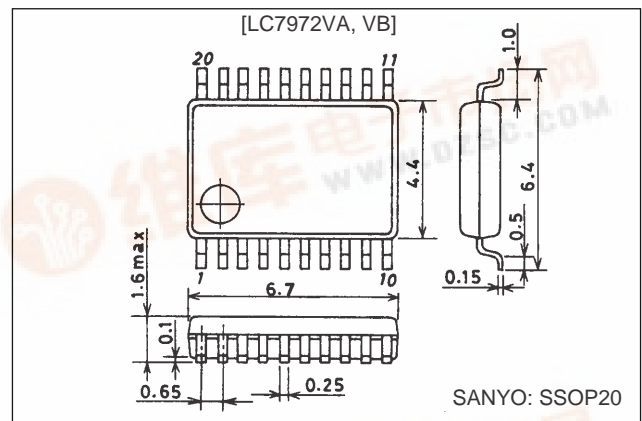
- High input impedance provided by fabrication in a CMOS process.
- Low power provided by fabrication in a CMOS process.
- One of two types of operational amplifier can be selected: inverting (operational amplifier 1) or noninverting (operational amplifier 2)
- Operating supply voltage: 4.9 to 5.2 V
- Package: SSOP20
- Operating temperature: Ta = -30 to +70°C

- The following modes are supported. These are selected via port level settings.

Package Dimensions

unit: mm

3179A-SSOP20



| Port | Level | Function |
|-------|-------|--|
| OP1ON | L | Operational amplifier 1: Operation stopped (low-power mode) |
| | H | Operational amplifier 1: Normal operation (OP2ON must be low in this mode.) |
| OP2ON | L | Operational amplifier 2: Operation stopped (low-power mode) |
| | H | Operational amplifier 2: Normal operation (OP1ON must be low in this mode.) |
| OFST1 | L | Operational amplifier 1: Offset mode (inverting input = V _{SS}) |
| | H | Operational amplifier 1: Operating mode (inverting input = normal input) |
| OFST2 | L | Operational amplifier 2: Offset mode (noninverting input = V _{SS}) |
| | H | Operational amplifier 2: Operating mode (noninverting input = normal input) |
| CLKC | L | Operational amplifier power supply clock: Internal clock |

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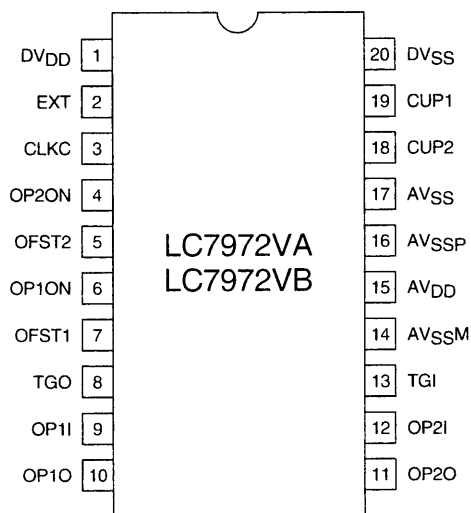
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Pin Assignment



Top view

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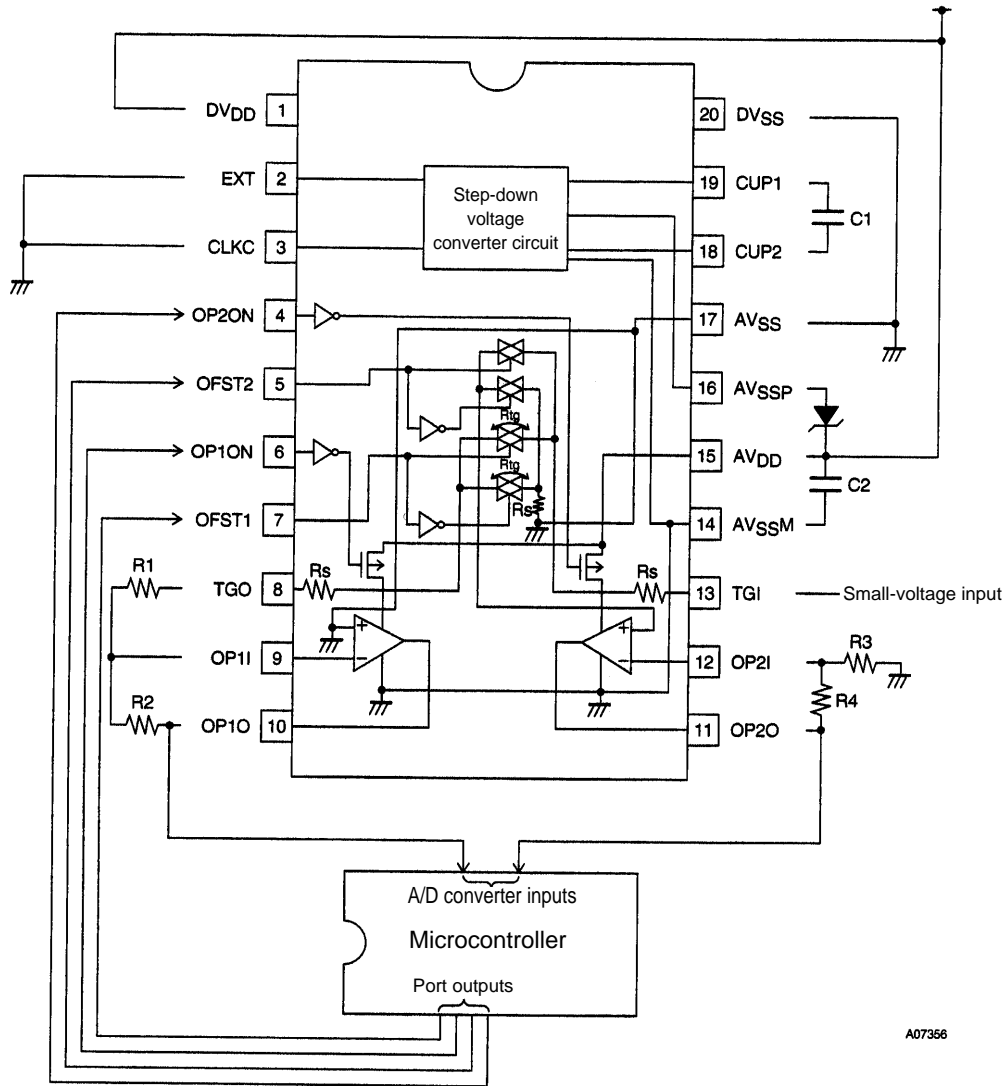
Pin Functions

| Pin | | Function |
|-----|-------------------|--|
| No. | Symbol | |
| 1 | DV _{DD} | Digital system power supply. Normally connected to +5 V. |
| 2 | EXT | Must be tied low. |
| 3 | CLKC | Must be tied low. |
| 4 | OP2ON | Operational amplifier 2 operation control |
| 5 | OFST2 | Operational amplifier 2 mode control |
| 6 | OP1ON | Operational amplifier 1 operation control |
| 7 | OFST1 | Operational amplifier 1 mode control |
| 8 | TGO | Operational amplifier 1 VSS/small voltage output |
| 9 | OP1I | Operational amplifier 1 input |
| 10 | OP1O | Operational amplifier 1 output |
| 11 | OP2O | Operational amplifier 2 output |
| 12 | OP2I | Operational amplifier 2 input |
| 13 | TGI | Small voltage input common to operational amplifiers 1 and 2 |
| 14 | AV _{SSM} | Operational amplifier power supply minus voltage generation |
| 15 | AV _{DD} | Analog system power supply. Normally connected to +5 V. |
| 16 | AV _{SSP} | Operational amplifier power supply external Zener diode connection |
| 17 | AV _{SS} | Analog system ground. Must be connected to 0 V. |
| 18 | CUP2 | Operational amplifier power supply external capacitor connection 2 |
| 19 | CUP1 | Operational amplifier power supply external capacitor connection 1 |
| 20 | DV _{SS} | Digital system ground. Must be connected to 0 V. |

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System Block Diagram and Sample Application

A circuit that amplifies very small voltages around the V_{SS} level can be constructed by adding the peripheral circuits shown in the figure below.



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Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|---------------------|--|------------------------------|------|
| Maximum supply voltage | V _{DD max} | V _{DD} | -0.3 to +7.0 | V |
| Output voltage | V _O | OP1O, OP2O, TGO | -0.3 to V _{DD} +0.3 | V |
| Input voltage | V _{I1} | OP1ON, OFST1, OP2ON, OFST2, EXT, CLKC, CUP2, CUP1, AV _{SSP} , OP1I, OP2I, TGI | -0.3 to V _{DD} +0.3 | V |
| | V _{I2} | AV _{SSM} | -3 to +0.3 | V |
| Peak output current | I _{OP} | OP1O, OP2O, TGO | -1 to +1 | mA |
| Average output current | I _{OA} | OP1O, OP2O, TGO : The current per pin | -1 to +1 | mA |
| Allowable power dissipation | Pd max | SSOP20 : Ta = -30 to +70°C | 100 | mW |
| Operating temperature | T _{opr} | | -30 to +70 | °C |
| Storage temperature | T _{stg} | | -55 to +125 | °C |

Allowable Operating Ranges at Ta = -30 to +70°C, V_{SS} = 0 V, V_{DD} = 4.9 to 5.2 V, unless otherwise specified

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---------------------------|------------------|--|---------------------|------|---------------------|------|
| | | | min | typ | max | |
| Supply voltage | V _{DD} | V _{DD} | 4.9 | | 5.2 | V |
| Input high-level voltage | V _{IH} | OP1ON, OFST1, OP2ON, OFST2 | 0.7 V _{DD} | | V _{DD} | V |
| Input low-level voltage | V _{IL1} | OP1ON, OFST1, OP2ON, OFST2, CLKC | V _{SS} | | 0.3 V _{DD} | V |
| | V _{IL2} | EXT | V _{SS} | | 0.3 V _{DD} | V |
| Common-mode input voltage | V _{IC} | | 0 | | 4.2 | V |
| Voltage drop | D _V | AV _{SSM} : Zener diode = 5.1 V (X rank specified) | | -0.2 | | V |

Electrical Characteristics at Ta = -30 to +70°C, V_{SS} = 0 V, V_{DD} = 4.9 to 5.2 V, unless otherwise specified

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|-------------------|---|-----------------------|------|-----|------|
| | | | min | typ | max | |
| Input high-level current | I _{IH1} | OP1ON, OFST1, OP2ON, OFST2 : V _{IN} = V _{DD} | | | 1.0 | μA |
| | I _{IH2} | TGI: V _{IN} = V _{DD} , with the built-in TG off. | | | 1.0 | μA |
| Input low-level current | I _{IL1} | OP1ON, OFST1, OP2ON, OFST2, EXT, CLKC : V _{IN} = V _{SS} | -1.0 | | | μA |
| | I _{IL2} | TGI: V _{IN} = V _{SS} , with the built-in TG off. | -1.0 | | | μA |
| Output high-level voltage | V _{OH} | OP1O, OP2O : I _{OH} = -3 μA | V _{DD} - 0.5 | | | V |
| Output low-level voltage | V _{OL} | OP1O, OP2O : I _{OL} = 3 μA | | | 0.5 | V |
| Operational amplifier 1 gain-related resistance | Rtg + 2Rs | TGO, TGI | 500 | 700 | 900 | Ω |
| Operational amplifier 1 gain-related resistance difference | Rx - Ry | TGO, TGI: Offset mode: Rx = Rtg + 2Rs Operating mode: Ry = Rtg + 2Rs | | | 80 | Ω |
| Current drain | | | | | | |
| Operating | I _{DDOP} | V _{DD} : Using the internal clock, with the operational amplifier 1 circuit operating. | | 700 | 900 | μA |
| Standby | I _{DDST} | V _{DD} : Both operational amplifiers 1 and 2 stopped. | | 0.05 | 10 | μA |

Operational Amplifier Characteristics at Ta = 25°C ±2°C, V_{SS} = 0 V, V_{DD} = 4.9 to 5.2 V, unless otherwise specified

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--------------------------------|------------------|---|---------|-----------------------|------|------|
| | | | min | typ | max | |
| Input offset voltage | V _{IO} | OP1I, OP2I : LC7972VA LC7972VB | | 5 | 10.5 | mV |
| | | | | 5 | 15 | mV |
| Supply voltage rejection ratio | P _{SRR} | 1 kHz | | 60 | | dB |
| Common-mode rejection ratio | C _{MRR} | | | 60 | | dB |
| Open-loop voltage gain | A _O | | | 80 | | dB |
| 0-dB bandwidth | f _T | | | 90 | | kHz |
| Maximum output voltage | V _O | OP1O, OP2O : R _L ≥ 100 kΩ | | V _{DD} - 0.5 | | V |
| Current drain | I _{CC} | For the operational amplifier 1 circuit | | 100 | | μA |
| Settling time | T _{SET} | OP1O, OP2O | | 900 | | μs |