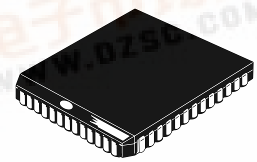
MCM67A618

64K x 18 Bit Asynchronous/ Latched Address Fast Static RAM



FN PACKAGE
PLASTIC
CASE 778–02

The MCM67A618 is a 1,179,648 bit latched address static random access memory organized as 65,536 words of 18 bits, fabricated with Motorola's high–performance silicon–gate BiCMOS technology. The device integrates a 64K x 18 SRAM core with advanced peripheral circuitry consisting of address and data input latches, active low chip enable, separate upper and lower byte write strobes, and a fast output enable. This device has increased output drive capability supported by multiple power pins.

Address, data in, and chip enable latches are provided. When latch enables (AL for address and chip enables and DL for data in) are high, the address, data in, and chip enable latches are in the transparent state. If latch enables are tied high the device can be used as an asynchronous SRAM. When latch enables are low the address, data in, and chip enable latches are in the latched state. This input latch simplifies read and write cycles by guaranteeing address and data–in hold time in a simple fashion.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits) while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

Six pair of power and ground pins have been utilized and placed on the package for maximum performance.

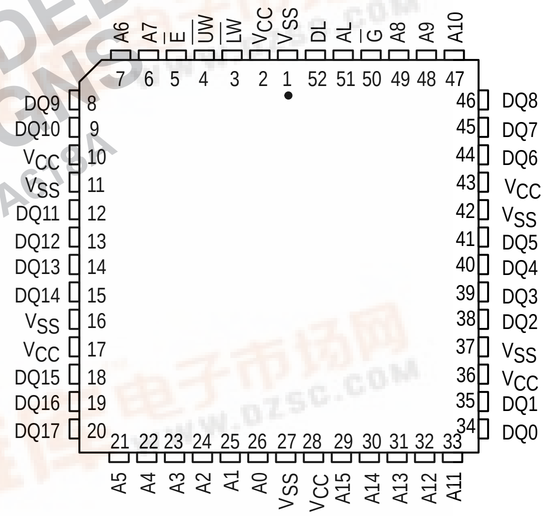
The MCM67A618 will be available in a 52–pin plastic leaded chip carrier (PLCC).

This device is ideally suited for systems that require wide data bus widths, cache memory, and tag RAMs.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 10/12/15 ns Max
- Byte Writeable via Dual Write Enables
- Separate Data Input Latch for Simplified Write Cycles
- Address and Chip Enable Input Latches
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three–State Outputs
- 3.3 V I/O Compatible
- High Board Density 52–Lead PLCC Package

NOT RECOMMENDED FOR NEW DESIGNS
SUBSTITUTE MCM67A618A

PIN ASSIGNMENT

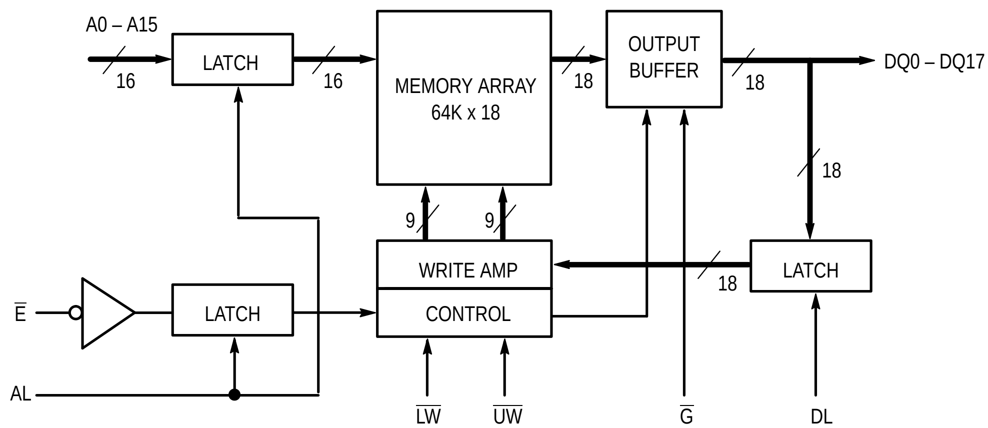


PIN NAMES

A0 – A15	Address Inputs
AL	Address Latch
DL	Data Latch
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Higher Byte Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device.

BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}$	$\overline{LW}$	$\overline{UW}$	AL*	DL*	$\overline{G}$	Mode	Supply Current	I/O Status
H	X	X	X	X	X	Deselected Cycle	I_{SB}	High–Z
L	X	X	L	X	X	Read or Write Using Latched Addresses	I_{CC}	—
L	X	X	H	X	X	Read or Write Using Unlatched Addresses	I_{CC}	—
L	H	H	X	X	L	Read Cycle	I_{CC}	Data Out
L	H	H	X	X	H	Read Cycle	I_{CC}	High–Z
L	L	L	X	L	X	Write Both Bytes Using Latched Data In	I_{CC}	High–Z
L	L	L	X	H	X	Write Both Bytes Using Unlatched Data In	I_{CC}	High–Z
L	L	H	X	X	X	Write Cycle, Lower Byte	I_{CC}	High–Z
L	H	L	X	X	X	Write Cycle, Lower Byte	I_{CC}	High–Z

*$\overline{E}$ and Addresses satisfy the specified setup and hold times for the falling edge of AL. Data–in satisfies the specified setup and hold times for falling edge of DL.

NOTE: This truth table shows the application of each function. Combinations of these functions are valid.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Standby Current ($\overline{G}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{AVAV} min)	I_{CCA10} I_{CCA12} I_{CCA15}	—	290 280 265	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{AVAV} min)	I_{SB1}	—	95	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V, f = f_{max})	I_{SB2}	—	20	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . 1.5 V
Input Pulse Levels . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . 3 ns
Output Timing Reference Level . . . . 1.5 V
Output Load . . . . Figure 1 Unless Otherwise Noted

ASYNCHRONOUS READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM67A618–10		MCM67A618–12		MCM67A618–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	10	—	12	—	15	—	ns	3
Access Times:								ns	4
Address Valid to Output Valid	t_{AVQV}	—	10	—	12	—	15		
$\overline{E}$ Low to Output Valid	t_{ELQV}	—	10	—	12	—	15		
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	7		
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	ns	
Output Buffer Control:								ns	5
$\overline{E}$ Low to Output Active	t_{ELQX}	3	—	3	—	3	—		
$\overline{G}$ Low to Output Active	t_{GLQX}	1	—	1	—	1	—		
$\overline{E}$ High to Output High–Z	t_{EHQZ}	2	5	2	6	2	7		
$\overline{G}$ High to Output High–Z	t_{GHQZ}	2	5	2	6	2	7		
Power Up Time	t_{ELICCA}	0	—	0	—	0	—	ns	

NOTES:
1. AL and DL are equal to V_{IH} for all asynchronous cycles.
2. Both Write Enable signals ($\overline{LW}$, $\overline{UW}$) are equal to V_{IH} for all read cycles.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EHQZ} is less than t_{ELQX} and t_{GHQZ} is less than t_{GLQX} for a given device.

AC TEST LOADS

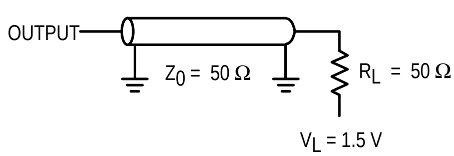


Figure 1A

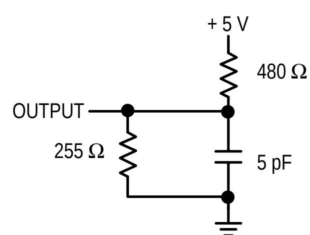
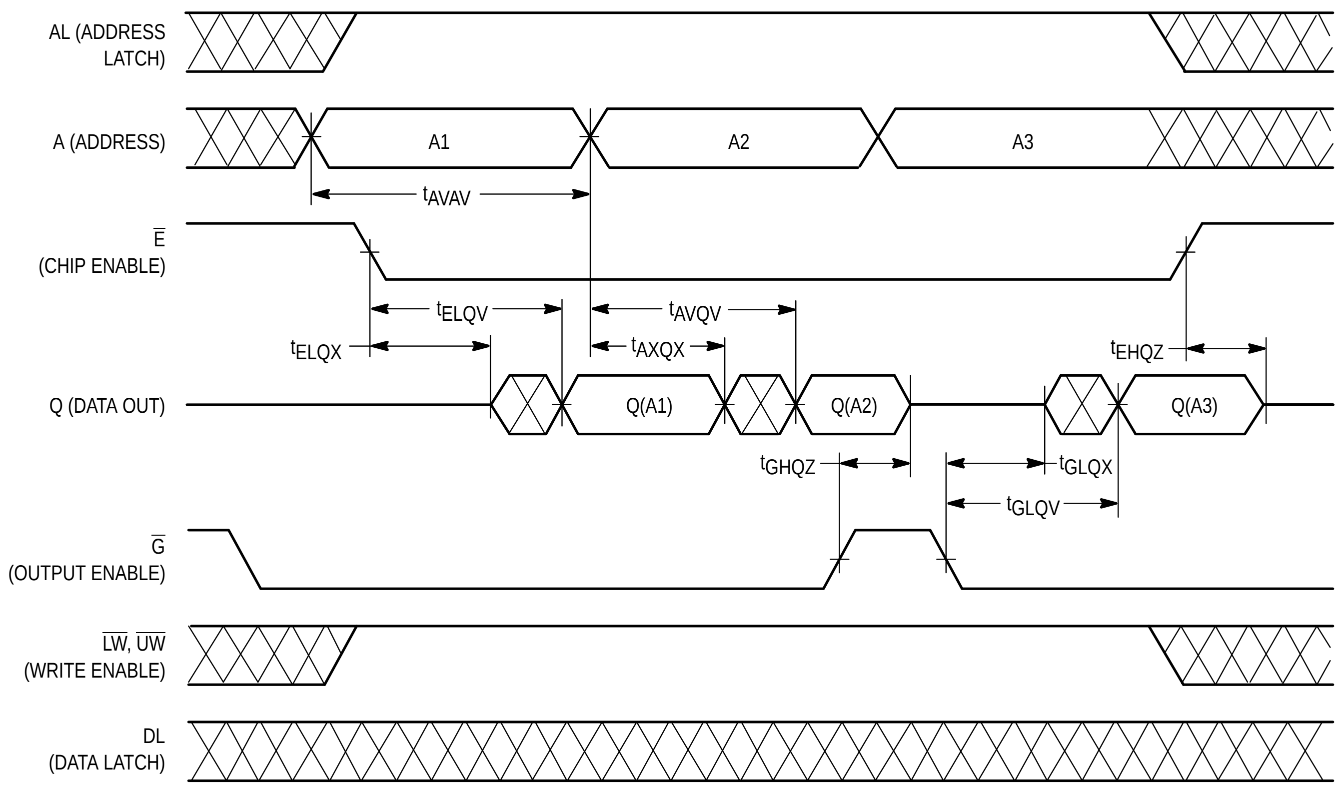


Figure 1B

ASYNCHRONOUS READ CYCLES

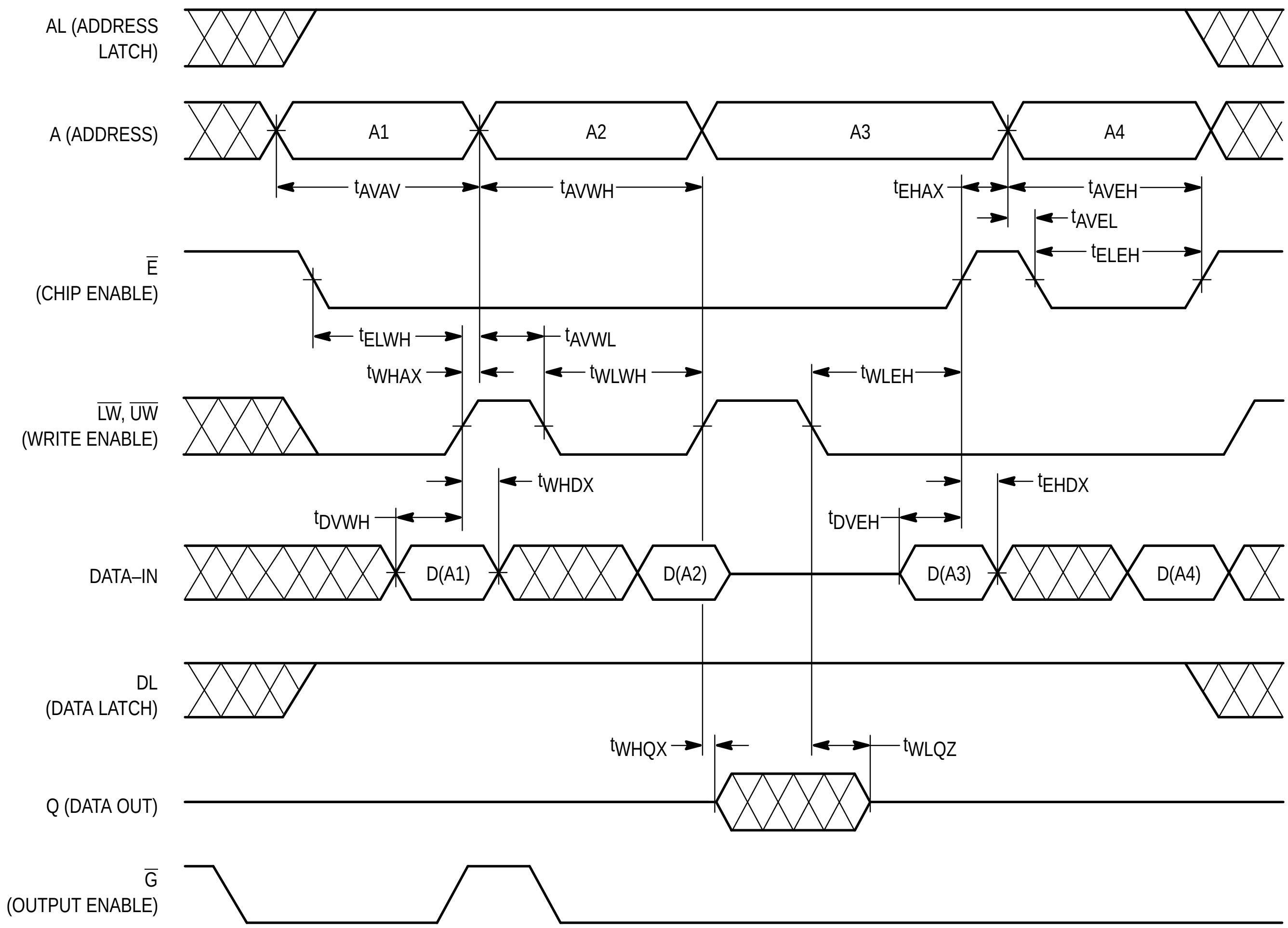


ASYNCHRONOUS WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67A618–10		MCM67A618–12		MCM67A618–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Times	t_{AVAV}	10	—	12	—	15	—	ns	4
Setup Times: Address Valid to End of Write	t_{AVWH}	9	—	10	—	13	—	ns	
Address Valid to $\overline{E}$ High	t_{AVEH}	9	—	10	—	13	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—		
Address Valid to $\overline{E}$ Low	t_{AVEL}	0	—	0	—	0	—		
DataValid to $\overline{W}$ High	t_{DVWH}	5	—	6	—	7	—		
Data Valid $\overline{E}$ High	t_{DVEH}	5	—	6	—	7	—		
Hold Times: $\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—	ns	
$\overline{E}$ High to Address Invalid	t_{EHAX}	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—		
$\overline{E}$ High to Data Invalid	t_{EHDX}	0	—	0	—	0	—		
Write Pulse Width: Write Pulse Width ($\overline{G}$ Low)	t_{WLWH}	9	—	10	—	13	—	ns	
Write Pulse Width ($\overline{G}$ High)	t_{WLWH}	8	—	9	—	12	—		
Write Pulse Width	t_{WLEH}	9	—	10	—	13	—		5
Enable to End of Write	t_{ELWH}	9	—	10	—	13	—		6
Enable to End of Write	t_{ELEH}	9	—	10	—	13	—		5, 6
Output Buffer Control: $\overline{W}$ High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	7
$\overline{W}$ Low to Output High–Z	t_{WLQZ}	0	5	0	6	0	9		7, 8

NOTES:
1. W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. AL and DL are equal to V_{IH} for all asynchronous cycles.
3. Both Write Enables must be equal to V_{IH} for all address transitions.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
6. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
7. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.
8. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.

ASYNCHRONOUS WRITE CYCLE



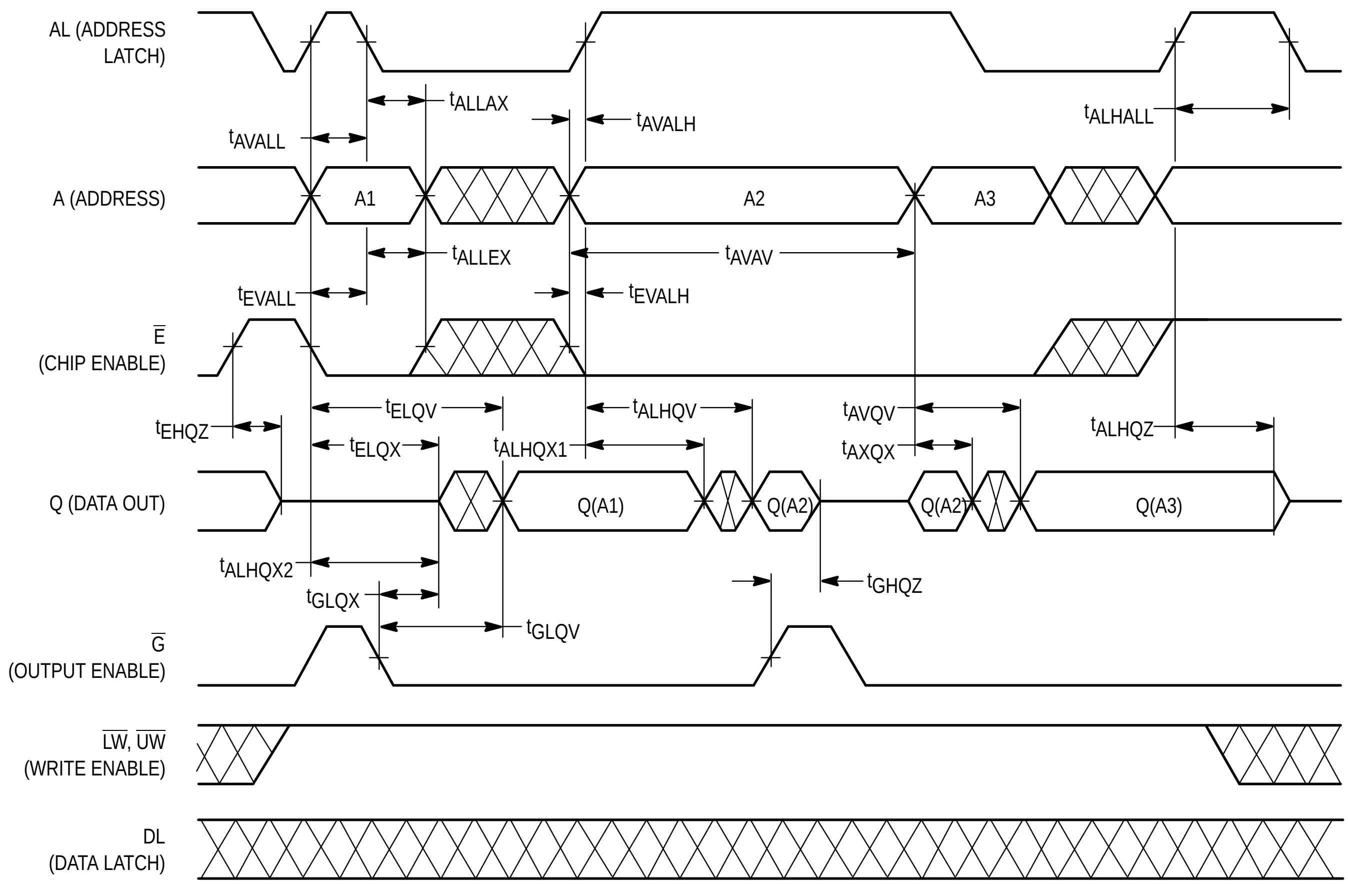
LATCHED READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM67A618–10		MCM67A618–12		MCM67A618–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	10	—	12	—	15	—	ns	3
Access Times:								ns	
Address Valid to Output Valid	t_{AVQV}	—	10	—	12	—	15		
$\overline{E}$ Low to Output Valid	t_{ELQV}	—	10	—	12	—	15		3
AL High to Output Valid	t_{ALHQV}	—	10	—	12	—	15		4
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	7		
Setup Times:								ns	
Address Valid to AL Low	t_{AVALL}	2	—	2	—	2	—		4
$\overline{E}$ Valid to AL Low	t_{EVALL}	2	—	2	—	2	—		4
Address Valid to AL High	t_{AVALH}	0	—	0	—	0	—		
$\overline{E}$ Valid to AL High	t_{EVALH}	0	—	0	—	0	—		
Hold Times:								ns	4
AL Low to Address Invalid	t_{ALLAX}	2	—	2	—	3	—		
AL Low to $\overline{E}$ Invalid	t_{ALLEX}	2	—	2	—	3	—		
Output Hold:								ns	
Address Invalid to Output Invalid	t_{AXQX}	4	—	4	—	4	—		
AL High to Output Invalid	t_{ALHQX1}	4	—	4	—	4	—		
Address Latch Pulse Width	t_{ALHALL}	5	—	5	—	5	—	ns	
Output Buffer Control:								ns	5
$\overline{E}$ Low to Output Active	t_{ELQX}	3	—	3	—	3	—		
$\overline{G}$ Low to Output Active	t_{GLQX}	1	—	1	—	1	—		
AL High to Output Active	t_{ALHQX2}	3	—	3	—	3	—		
$\overline{E}$ High to Output High–Z	t_{EHQZ}	2	5	2	6	2	9		
AL High to Output High–Z	t_{ALHQZ}	2	5	2	6	2	9		
$\overline{G}$ High to Output High–Z	t_{GHQZ}	2	5	2	6	2	7		

NOTES:

1. Both Write Enable Signals ($\overline{LW}$, $\overline{UW}$) are equal to V_{IH} for all read cycles.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of address latch (AL) and data latch (DL).
5. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EHQZ} is less than t_{ELQX} and t_{ALHQZ} is less than t_{ALHQX2} and t_{GHQZ} is less than t_{GLQX} for a given device.

LATCHED READ CYCLES

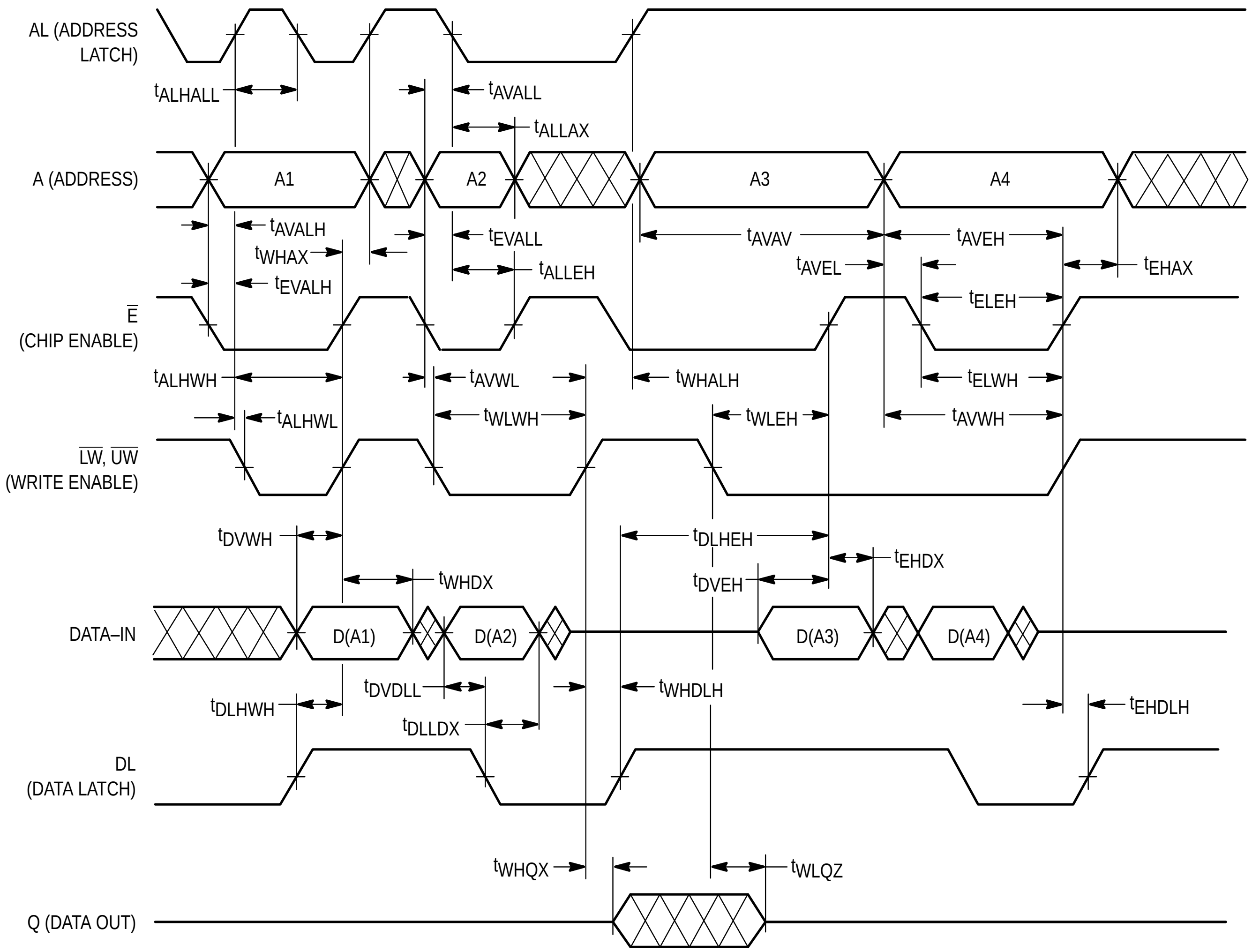


LATCHED WRITE CYCLE TIMING (See Notes 1, 2, and 3)

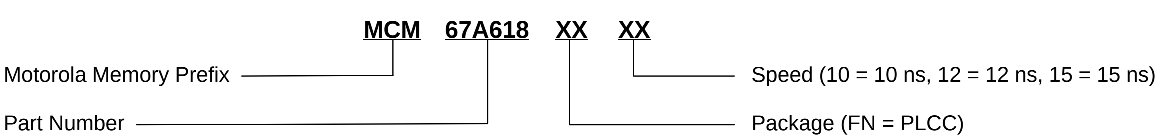
Parameter	Symbol	MCM67A618–10		MCM67A618–12		MCM67A618–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Times: Address Valid to Address Valid	t_{AVAV}	10	—	12	—	15	—	ns	4
Setup Times:								ns	
Address Valid to End of Write	t_{AVWH}	9	—	10	—	13	—		
Address Valid to End of Write	t_{AVEH}	9	—	10	—	13	—		
$\overline{E}$ Valid to AL Low	t_{EVALL}	2	—	2	—	2	—		
Address Valid to AL Low	t_{AVALL}	2	—	2	—	2	—		
$\overline{E}$ Valid to AL High	t_{EVALH}	0	—	0	—	0	—		
Address Valid to AL High	t_{AVALH}	0	—	0	—	0	—		
AL High to $\overline{W}$ Low	t_{ALHWL}	0	—	0	—	0	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—		
Address Valid to $\overline{E}$ Low	t_{AVEL}	0	—	0	—	0	—		
Data Valid to DL Low	t_{DVDLL}	2	—	2	—	2	—		
Data Valid to $\overline{W}$ High	t_{DVWH}	5	—	6	—	7	—		
Data Valid to $\overline{E}$ High	t_{DVEH}	5	—	6	—	7	—		
DL High to $\overline{W}$ High	t_{DLHWH}	5	—	6	—	7	—		
DL High to $\overline{E}$ High	t_{DLHEH}	5	—	6	—	7	—		
Hold Times:								ns	
AL Low to $\overline{E}$ High	t_{ALLEH}	2	—	2	—	3	—		4
AL Low to Address Invalid	t_{ALLAX}	2	—	2	—	3	—		4
DL Low to Data Invalid	t_{DLLDX}	2	—	2	—	3	—		
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—		
$\overline{E}$ High to Address Invalid	t_{EHAX}	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—		
$\overline{E}$ High to Data Invalid	t_{EHDX}	0	—	0	—	0	—		
$\overline{W}$ High to DL High	t_{WHDLH}	0	—	0	—	0	—		
$\overline{E}$ High to DL High	t_{EHDLH}	0	—	0	—	0	—		
$\overline{W}$ High to AL High	t_{WHALH}	0	—	0	—	0	—		
Write Pulse Width:								ns	
AL High to $\overline{W}$ High	t_{ALHWH}	9	—	10	—	13	—		5
Write Pulse Width ($\overline{G}$ Low)	t_{WLWH}	9	—	10	—	13	—		
Write Pulse Width ($\overline{G}$ High)	t_{WLWH}	8	—	9	—	12	—		
Write Pulse Width	t_{WLEH}	9	—	10	—	13	—		6
Enable to End of Write	t_{ELWH}	9	—	10	—	13	—		7
Enable to End of Write	t_{ELEH}	9	—	10	—	13	—		6, 7
Address Latch Pulse Width	t_{ALHALL}	5	—	5	—	5	—	ns	4
Output Buffer Control:								ns	
$\overline{W}$ High to Output Active	t_{WHQX}	3	—	3	—	3	—		8
$\overline{W}$ Low to Output High–Z	t_{WLQZ}	0	5	0	6	0	9		8, 9

NOTES:
1. $\overline{W}$ refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
3. Both Write Enables must be equal to V_{IH} for all address transitions.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of address latch (AL) and data latch (DL).
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
7. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
8. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.
9. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.

LATCHED WRITE CYCLES



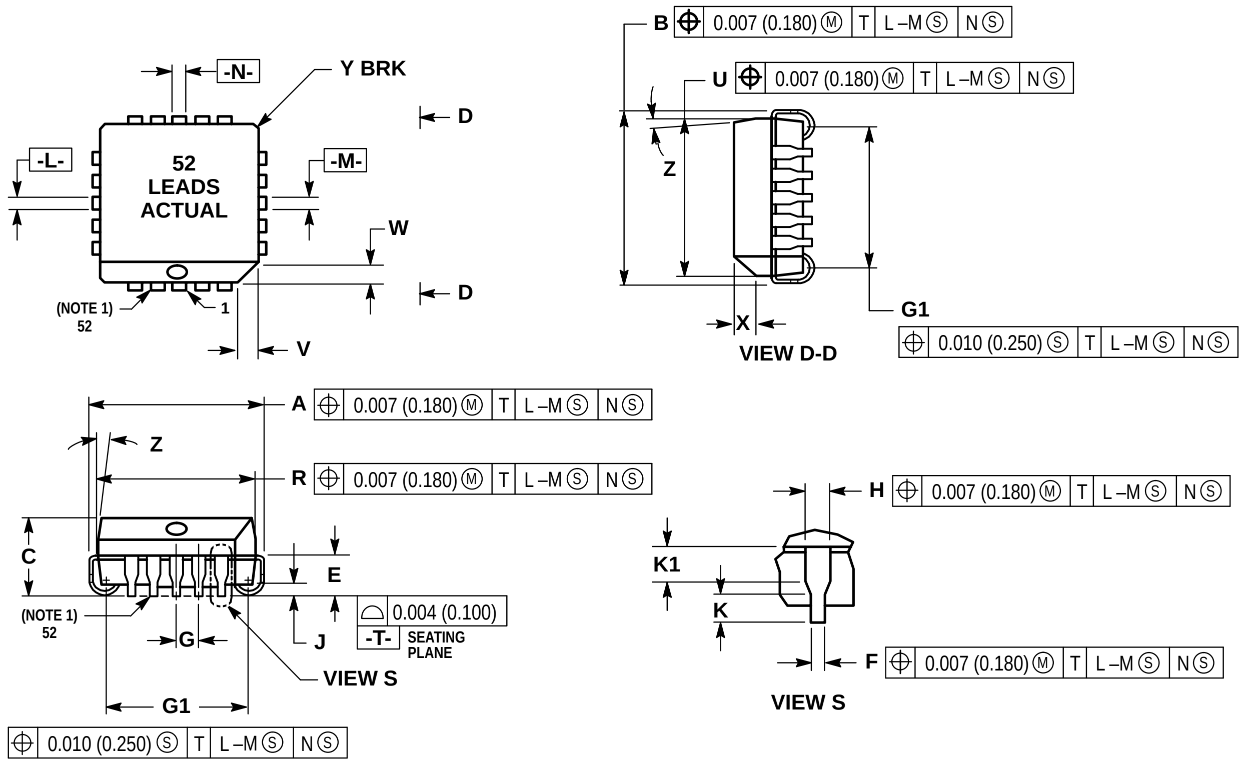
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM67A618FN10 MCM67A618FN12 MCM67A618FN15

PACKAGE DIMENSIONS

FN PACKAGE
52–LEAD PLCC
CASE 778–02



NOTES:
1. **DUE TO SPACE LIMITATION, CASE 778-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 52 LEADS.**
2. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.
7. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
8. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.785	0.795	19.94	20.19
B	0.785	0.795	19.94	20.19
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.750	0.756	19.05	19.20
U	0.750	0.756	19.05	19.20
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.710	0.730	18.04	18.54
K1	0.040	—	1.02	—

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