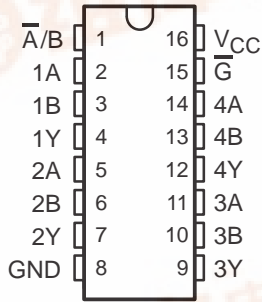# QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS
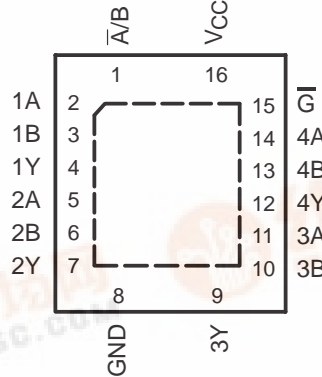
SCAS292O – JANUARY 1993 – REVISED FEBRUARY 2004

- **Operate From 1.65 V to 3.6 V**
- **Specified From –40°C to 85°C, –40°C to 125°C, and –55°C to 125°C**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 5.2 ns at 3.3 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**

- **Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
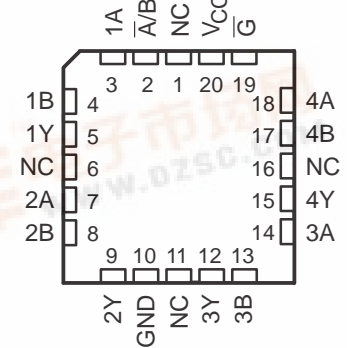 - **1000-V Charged-Device Model (C101)**

SN54LVC157A . . . J OR W PACKAGE
SN74LVC157A . . . D, DB, NS, OR PW PACKAGE
(TOP VIEW)

$\overline{A}$/B	1	16 V_{CC}
1A	2	15 $\overline{G}$
1B	3	14 4A
1Y	4	13 4B
2A	5	12 4Y
2B	6	11 3A
2Y	7	10 3B
GND	8	9 3Y

SN74LVC157A . . . RGY PACKAGE
(TOP VIEW)

$\overline{A}$/B V_{CC}

1A	2	15 $\overline{G}$
1B	3	14 4A
1Y	4	13 4B
2A	5	12 4Y
2B	6	11 3A
2Y	7	10 3B

GND   3Y

SN54LVC157A . . . FK PACKAGE
(TOP VIEW)

1A $\overline{A}$/B NC V_{CC} $\overline{G}$
3 2 1 20 19

1B	4	18 4A
1Y	5	17 4B
NC	6	16 NC
2A	7	15 4Y
2B	8	14 3A

9 10 11 12 13
2Y GND NC 3Y 3B

NC – No internal connection

description/ordering information

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 1.65-V to 3.6-V V_{CC} operation.

The 'LVC157A devices feature a common strobe ($\overline{G}$) input. When $\overline{G}$ is high, all outputs are low. When $\overline{G}$ is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The devices provide true data.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC157ARGYR	LC157A
–40°C to 125°C	SOIC – D	Tube of 40	SN74LVC157AD	LVC157A
		Reel of 2500	SN74LVC157ADR	
		Reel of 250	SN74LVC157ADT	
	SOP – NS	Reel of 2000	SN74LVC157ANSR	LVC157A
	SSOP – DB	Reel of 2000	SN74LVC157ADBR	LC157A
	TSSOP – PW	Tube of 90	SN74LVC157APW	LC157A
		Reel of 2000	SN74LVC157APWR	
		Reel of 250	SN74LVC157APWT	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LVC157AJ	SNJ54LVC157AJ
	CFP – W	Tube of 150	SNJ54LVC157AW	SNJ54LVC157AW
	LCCC – FK	Tube of 55	SNJ54LVC157AFK	SNJ54LVC157AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

description/ordering information (continued)

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{G}$	$\overline{A}/B$	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

logic diagram (positive logic)
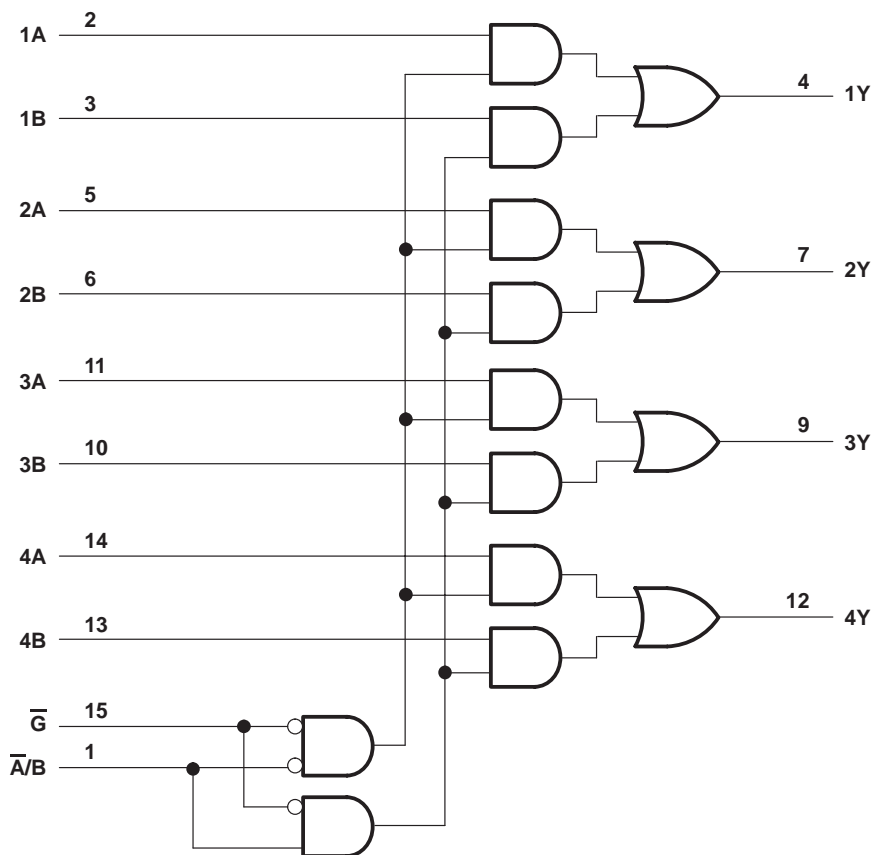
Pin numbers shown are for the D, DB, J, NS, PW, RGY, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 6.5 V
Input voltage range, V_I (see Note 1) .... –0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2) .... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) .... –50 mA
Output clamp current, I_{OK} ($V_O < 0$) .... –50 mA
Continuous output current, I_O .... ±50 mA
Continuous current through V_{CC} or GND .... ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package .... 73°C/W
(see Note 3): DB package .... 82°C/W
(see Note 3): NS package .... 64°C/W
(see Note 3): PW package .... 108°C/W
(see Note 4): RGY package .... 39°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C
Power dissipation, P_{tot} ($T_A = -40°C$ to 125°C) (see Notes 5 and 6) .... 500 mW

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.
5. For the D package, above 70°C the value of P_{tot} derates linearly with 8 mW/K.
6. For the DB, NS, and PW packages, above 60°C the value of P_{tot} derates linearly with 5.5 mW/K.

recommended operating conditions (see Note 7)

			SN54LVC157A		UNIT
			−55 TO 125°C		
			MIN	MAX	
V_{CC}	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	

NOTE 7:   All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions (see Note 7)

			SN74LVC157A						UNIT
			T_A = 25°C		−40 TO 85°C		−40 TO 125°C		
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		$0.65 \times V_{CC}$		$0.65 \times V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V	1.7		1.7		1.7		
		V_{CC} = 2.7 V to 3.6 V	2		2		2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$		$0.35 \times V_{CC}$		$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V		0.7		0.7		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8		0.8		0.8	
V_I	Input voltage		0	5.5	0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		−4		−4		−4	mA
		V_{CC} = 2.3 V		−8		−8		−8	
		V_{CC} = 2.7 V		−12		−12		−12	
		V_{CC} = 3 V		−24		−24		−24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4		4		4	mA
		V_{CC} = 2.3 V		8		8		8	
		V_{CC} = 2.7 V		12		12		12	
		V_{CC} = 3 V		24		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10		10		10	ns/V

NOTE 7:   All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	SN54LVC157A −55 TO 125°C		UNIT
					MIN	MAX	
V_{OH}		I_{OH} = −100 µA		2.7 V to 3.6 V	V_{CC}−0.2		V
		I_{OH} = −12 mA		2.7 V	2.2		
				3 V	2.4		
		I_{OH} = −24 mA		3 V	2.2		
V_{OL}		I_{OL} = 100 µA		2.7 V to 3.6 V		0.2	V
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3 V		0.55	
I_I	All inputs	V_I = 5.5 V or GND		3.6 V		±5	µA
I_{CC}		V_I = V_{CC} or GND	I_O = 0	3.6 V		10	µA
ΔI_{CC}		One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V		500	µA

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	SN74LVC157A						UNIT
					T_A = 25°C			−40 TO 85°C		−40 TO 125°C	
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −100 µA		1.65 V to 3.6 V	V_{CC}−0.2			V_{CC}−0.2		V_{CC}−0.3		V
		I_{OH} = −4 mA		1.65 V	1.29			1.2		1.05		
		I_{OH} = −8 mA		2.3 V	1.9			1.7		1.55		
		I_{OH} = −12 mA		2.7 V	2.2			2.2		2.05		
				3 V	2.4			2.4		2.25		
		I_{OH} = −24 mA		3 V	2.3			2.2		2		
V_{OL}		I_{OL} = 100 µA		1.65 V to 3.6 V			0.1		0.2		0.3	V
		I_{OL} = 4 mA		1.65 V			0.24		0.45		0.6	
		I_{OL} = 8 mA		2.3 V			0.3		0.7		0.75	
		I_{OL} = 12 mA		2.7 V			0.4		0.4		0.6	
		I_{OL} = 24 mA		3 V			0.55		0.55		0.8	
I_I	All inputs	V_I = 5.5 V or GND		3.6 V			±1		±5		±20	µA
I_{CC}		V_I = V_{CC} or GND	I_O = 0	3.6 V			1		10		40	µA
ΔI_{CC}		One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			500		500		5000	µA
C_i		V_I = V_{CC} or GND		3.3 V		5						pF

TEXAS
INSTRUMENTS

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN54LVC157A −55 TO 125°C MIN	MAX	UNIT
t_{pd}	A or B	Y	2.7 V		6.2	ns
			3.3 V ± 0.3 V	0.8	5.4	
	$\overline{A}/B$		2.7 V		8.2	
			3.3 V ± 0.3 V	0.8	7	
	$\overline{G}$		2.7 V		7.8	
			3.3 V ± 0.3 V	0.8	6.5	

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C MIN	TYP	MAX	−40 TO 85°C MIN	MAX	−40 TO 125°C MIN	MAX	UNIT
t_{pd}	A or B	Y	1.8 V ± 0.15 V	1	5.5	13.5	1	14	1	15.5	ns
			2.5 V ± 0.2 V	1	3.2	7.4	1	7.9	1	10	
			2.7 V	1	3.6	5.7	1	5.9	1	7.4	
			3.3 V ± 0.3 V	1	3	5	1	5.2	1	6.4	
	$\overline{A}/B$		1.8 V ± 0.15 V	1	6	15.5	1	16	1	17.5	
			2.5 V ± 0.2 V	1	3.7	9.6	1	10.1	1	12.2	
			2.7 V	1	4.1	7.9	1	8.1	1	10	
			3.3 V ± 0.3 V	1	3.4	6.6	1	6.8	1	8.4	
	$\overline{G}$		1.8 V ± 0.15 V	1	5.9	13.5	1	14	1	15.5	
			2.5 V ± 0.2 V	1	3.5	9.3	1	9.8	1	11.9	
			2.7 V	1	3.9	7.6	1	7.8	1	9.3	
			3.3 V ± 0.3 V	1	3.3	6.3	1	6.5	1	7.9	
$t_{sk(o)}$			1.8 V ± 0.15 V					2		2.5	ns
			3.3 V ± 0.3 V					1		1.5	

operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	f = 10 MHz	1.8 V	14*	pF
		2.5 V	15*	
		3.3 V	16	

* On products compliant to MIL-PRF-38535, this parameter does not apply.

PARAMETER MEASUREMENT INFORMATION
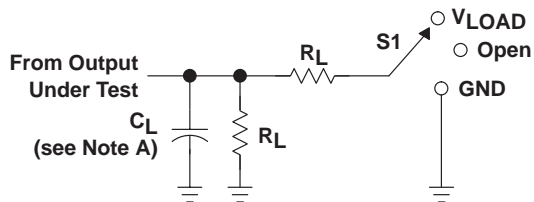
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

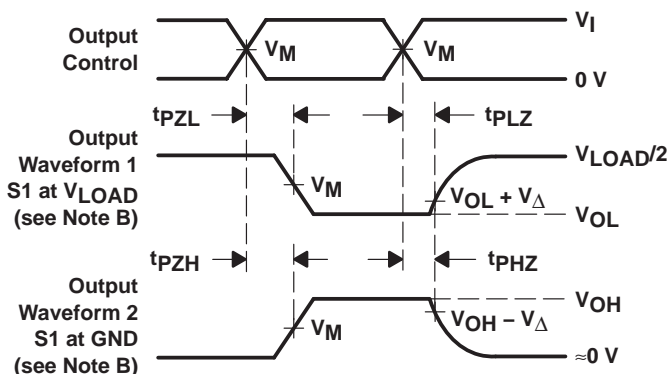| V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
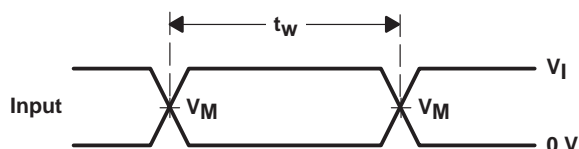
VOLTAGE WAVEFORMS
PULSE DURATION
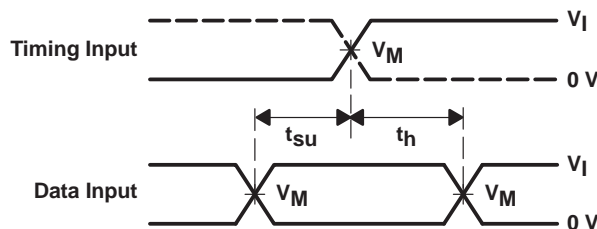
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
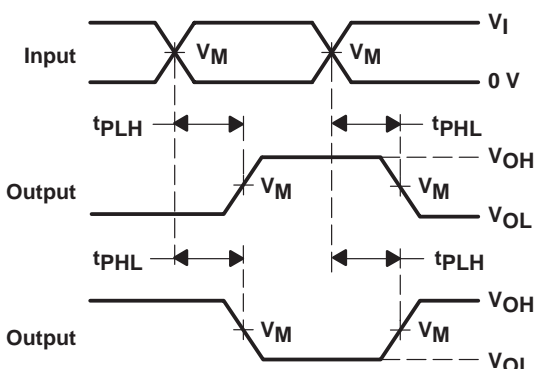
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
      B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
         Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
      C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
      D. The outputs are measured one at a time, with one transition per measurement.
      E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
      F. t_{PZL} and t_{PZH} are the same as t_{en}.
      G. t_{PLH} and t_{PHL} are the same as t_{pd}.
      H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

TEXAS
INSTRUMENTS

J (R–GDIP–T**)   CERAMIC DUAL IN–LINE PACKAGE
14 LEADS SHOWN

PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

$\frac{0.065\ (1,65)}{0.045\ (1,14)}$

0.005 (0,13) MIN

$\frac{0.060\ (1,52)}{0.015\ (0,38)}$

0.200 (5,08) MAX

Seating Plane

A

0.130 (3,30) MIN

$\frac{0.026\ (0,66)}{0.014\ (0,36)}$

0.100 (2,54)

0°–15°

$\frac{0.014\ (0,36)}{0.008\ (0,20)}$

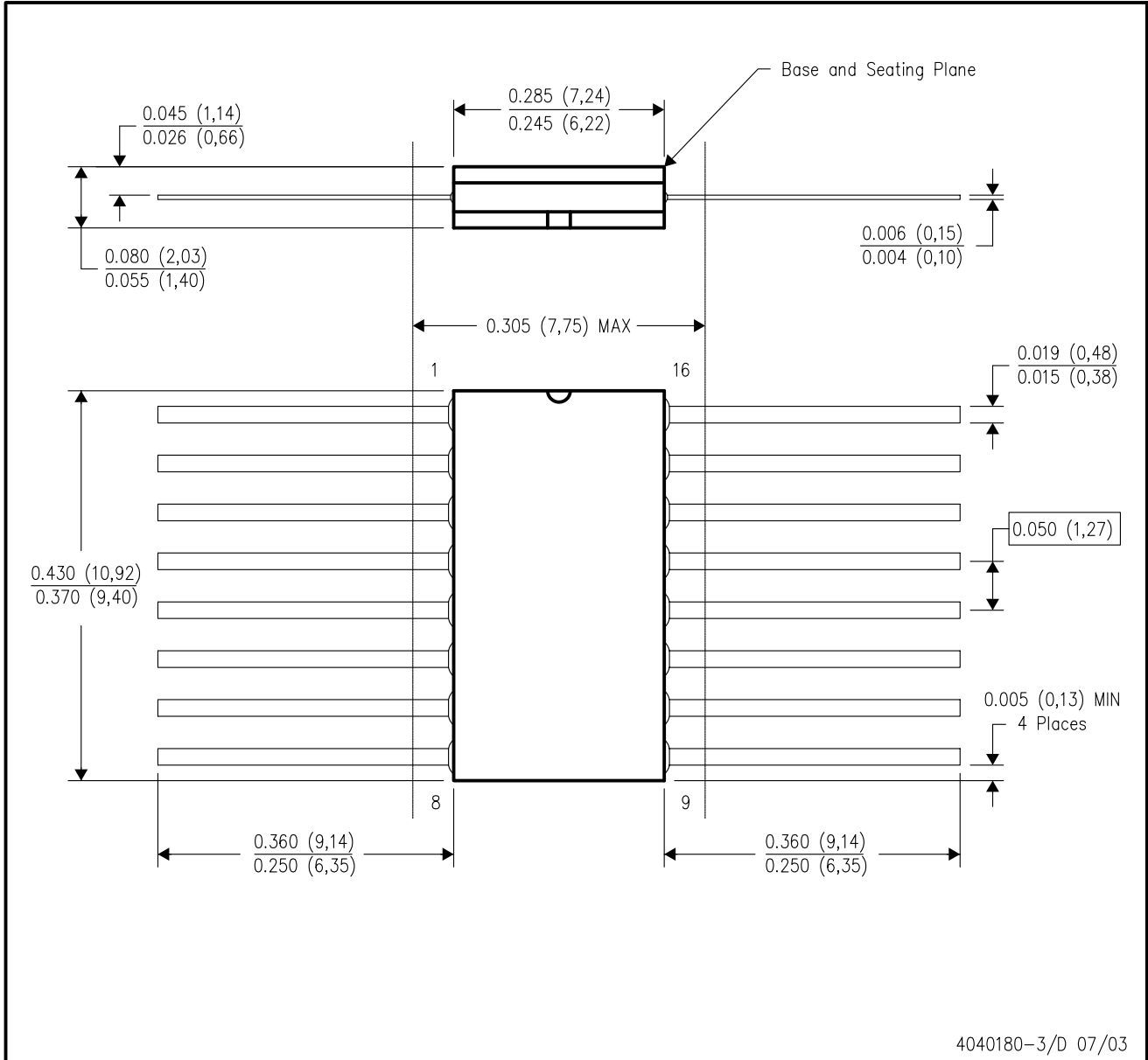4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   This package is hermetically sealed with a ceramic lid using glass frit.
          D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
          E.   Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

W (R−GDFP−F16)   CERAMIC DUAL FLATPACK

Base and Seating Plane

$\dfrac{0.045\ (1,14)}{0.026\ (0,66)}$

$\dfrac{0.285\ (7,24)}{0.245\ (6,22)}$

$\dfrac{0.080\ (2,03)}{0.055\ (1,40)}$

$\dfrac{0.006\ (0,15)}{0.004\ (0,10)}$

0.305 (7,75) MAX

$\dfrac{0.019\ (0,48)}{0.015\ (0,38)}$

1   16

$\dfrac{0.430\ (10,92)}{0.370\ (9,40)}$

0.050 (1,27)

0.005 (0,13) MIN
4 Places

8   9

$\dfrac{0.360\ (9,14)}{0.250\ (6,35)}$ $\dfrac{0.360\ (9,14)}{0.250\ (6,35)}$

4040180−3/D 07/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only.
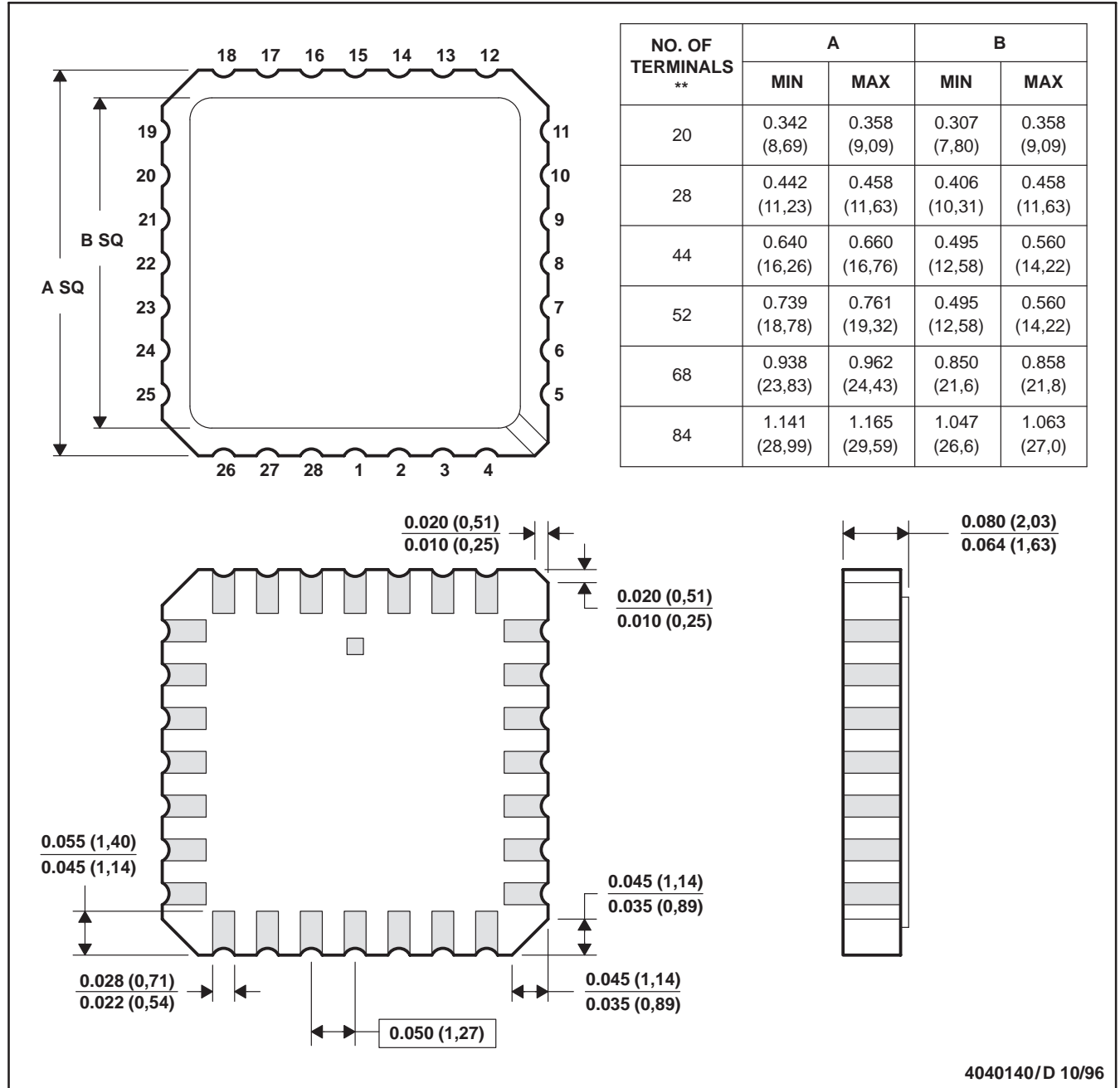   E.   Falls within MIL STD 1835 GDFP1−F16 and JEDEC MO−092AC

MECHANICAL DATA

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

0.020 (0,51) / 0.010 (0,25)

0.020 (0,51) / 0.010 (0,25)

0.080 (2,03) / 0.064 (1,63)

0.055 (1,40) / 0.045 (1,14)

0.045 (1,14) / 0.035 (0,89)

0.028 (0,71) / 0.022 (0,54)

0.045 (1,14) / 0.035 (0,89)
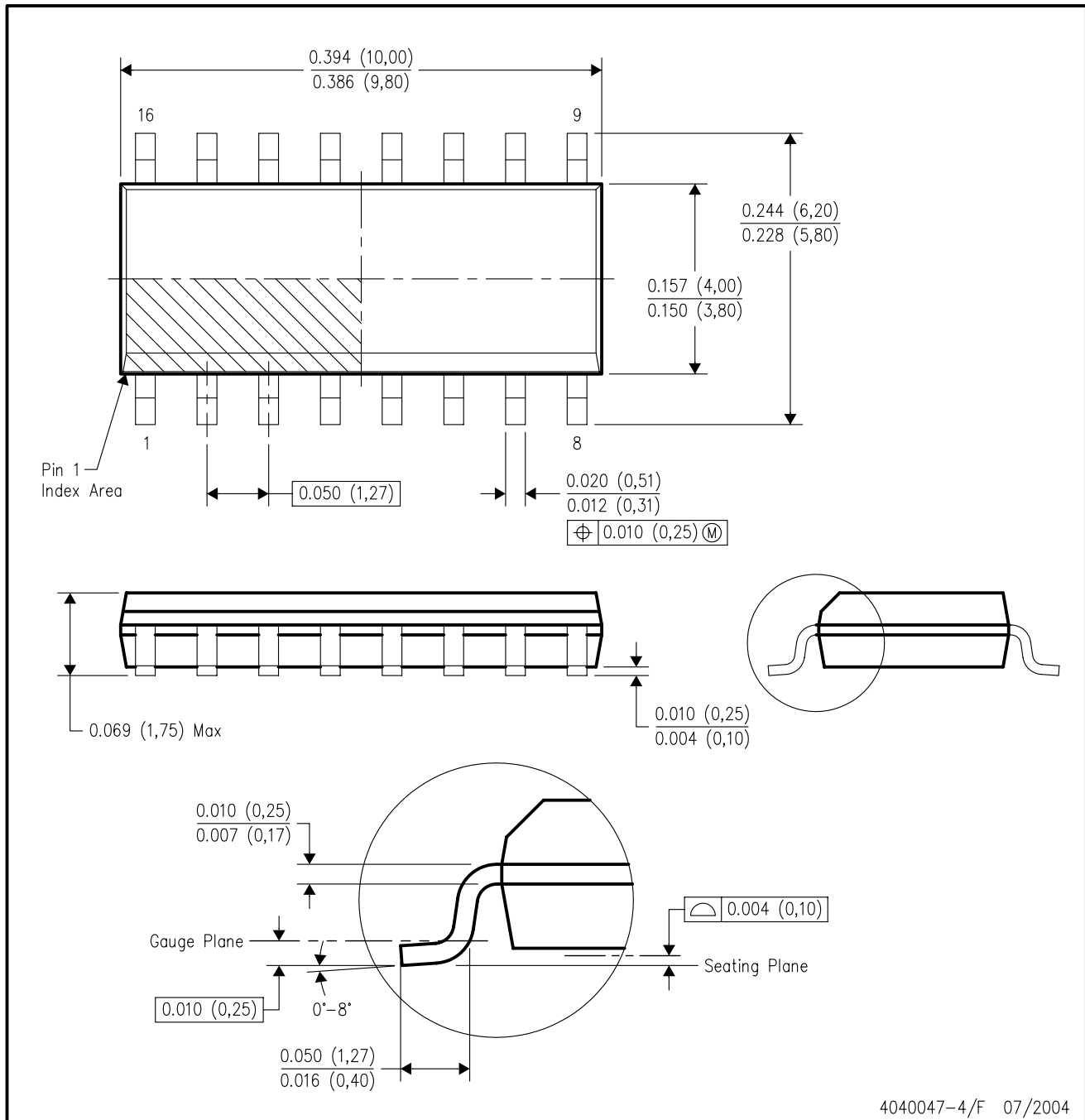
0.050 (1,27)

4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

TEXAS
INSTRUMENTS

D (R−PDSO−G16)　　　　　　　PLASTIC SMALL−OUTLINE PACKAGE

0.394 (10,00)
0.386 (9,80)

16　　　　　　　9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1　　　　　　　8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

Gauge Plane

⌒ 0.004 (0,10)

Seating Plane

0.010 (0,25)　　0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−4/F　07/2004

NOTES:　A.　All linear dimensions are in inches (millimeters).
　　　　　B.　This drawing is subject to change without notice.
　　　　　C.　Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
　　　　　D.　Falls within JEDEC MS−012 variation AC.

RGY (R−PQFP−N16)   PLASTIC QUAD FLATPACK

Pin 1 Index Area
Top and Bottom
/E\

0,20 Nominal
Lead Frame

Seating Plane

0,05
0,00
Seating Height

Exposed Thermal Pad
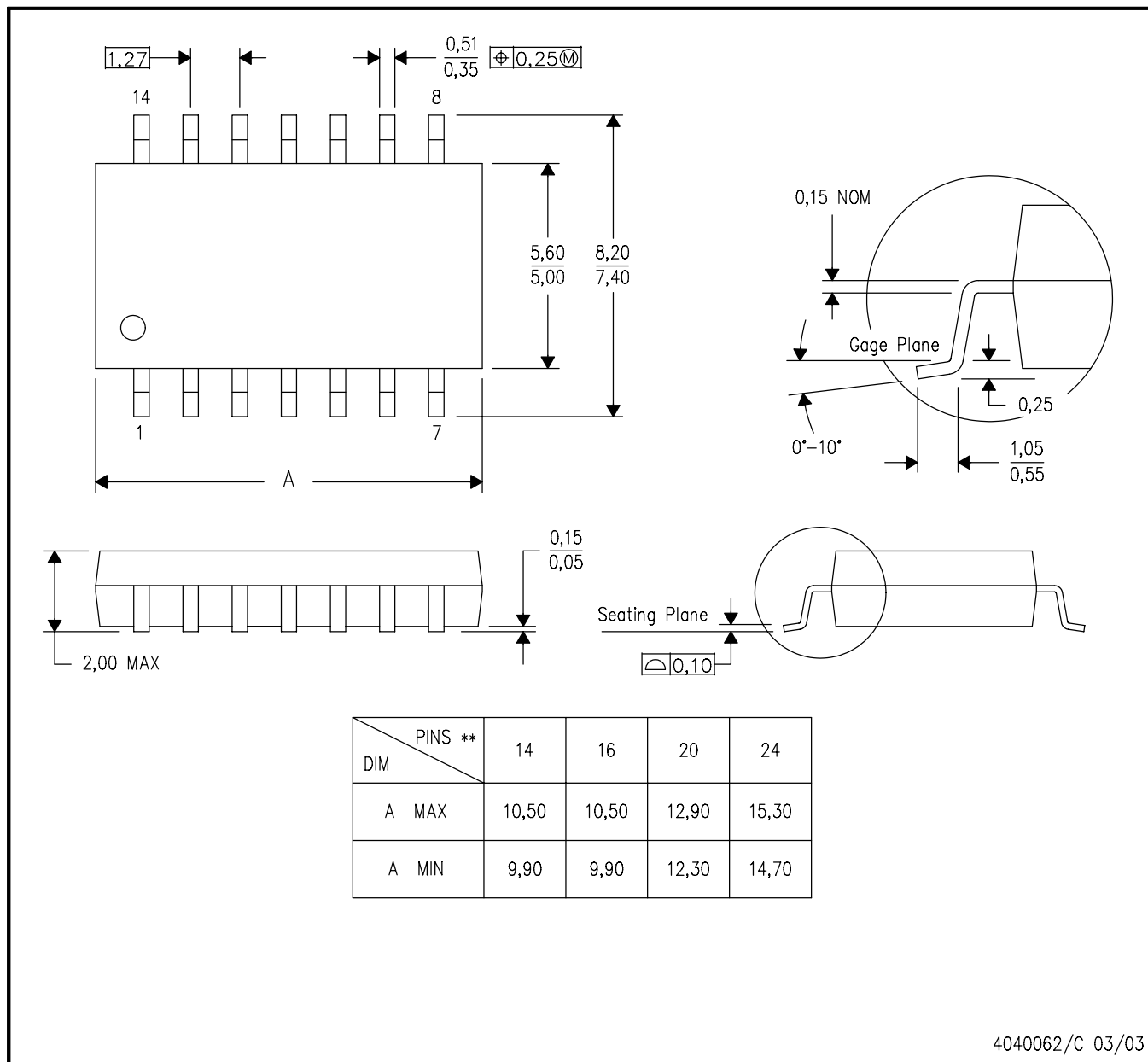/D\

Bottom View

4203539−3/F 02/2005
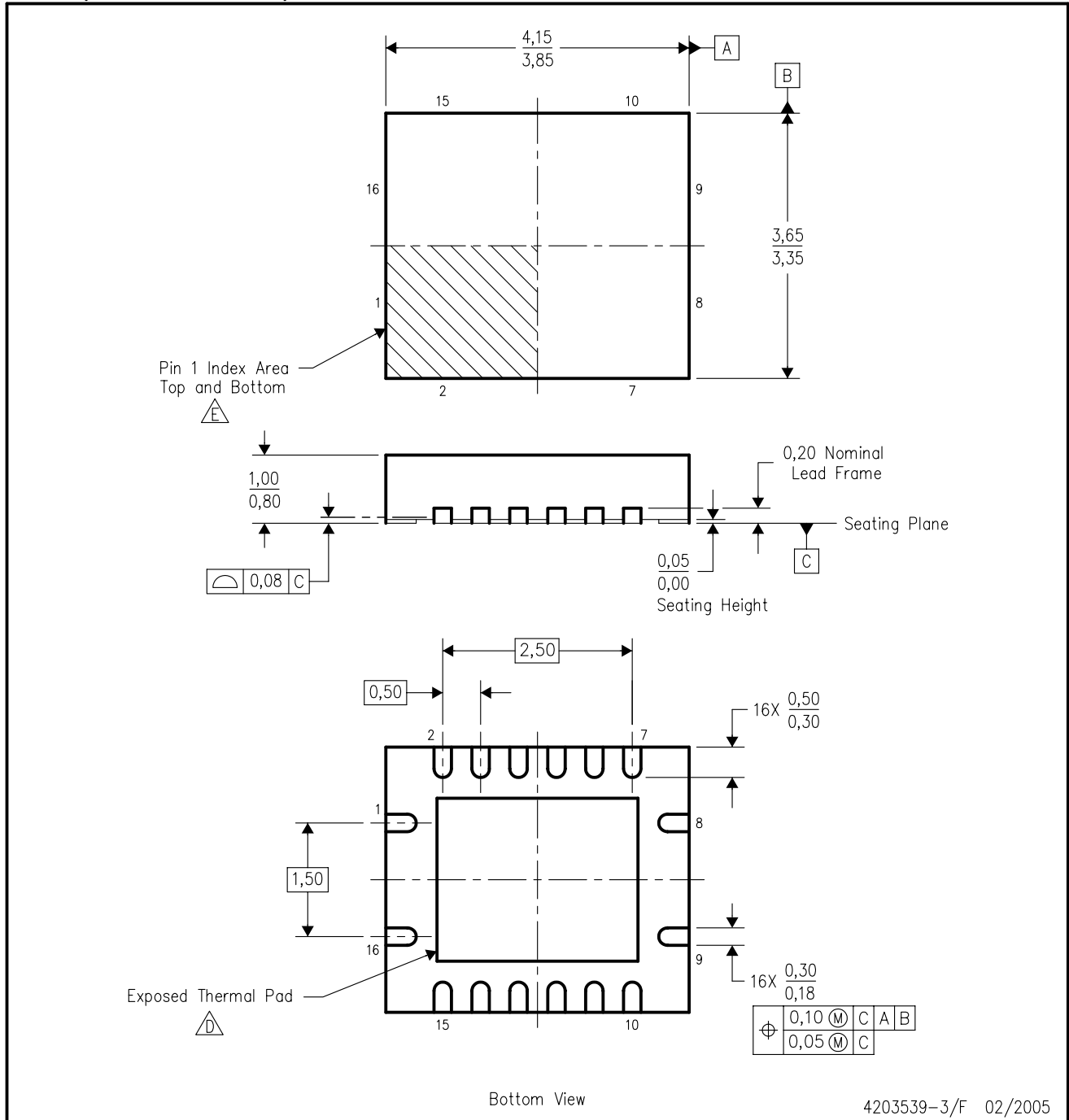
NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
          B.   This drawing is subject to change without notice.
          C.   QFN (Quad Flatpack No−Lead) package configuration.

     /D\ The package thermal pad must be soldered to the board for thermal and mechanical performance.
          See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

     /E\ Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
          The Pin 1 identifiers are either a molded, marked, or metal feature.

          F.   Package complies to JEDEC MO−241 variation BB.

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MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

DIM / PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
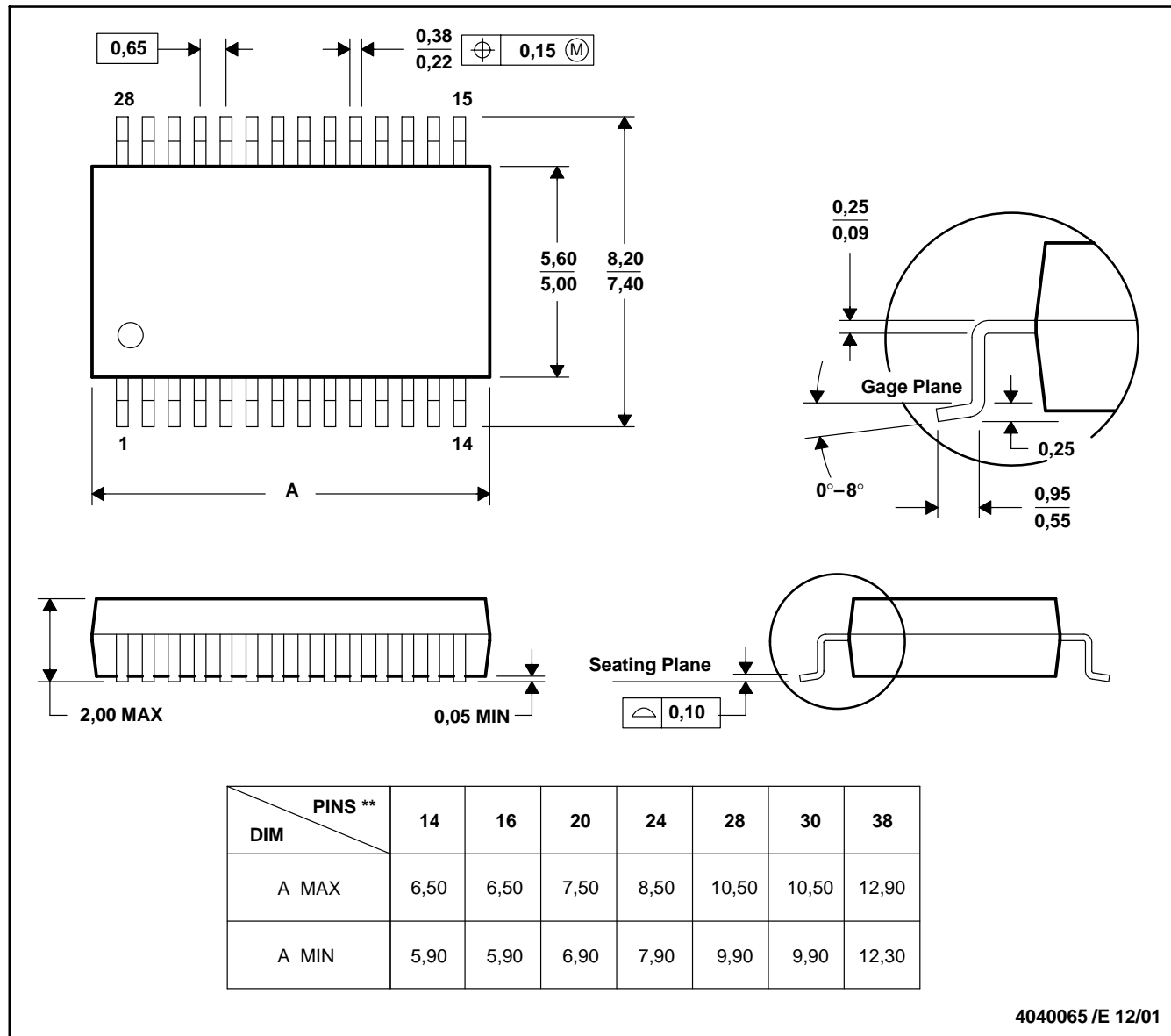   C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
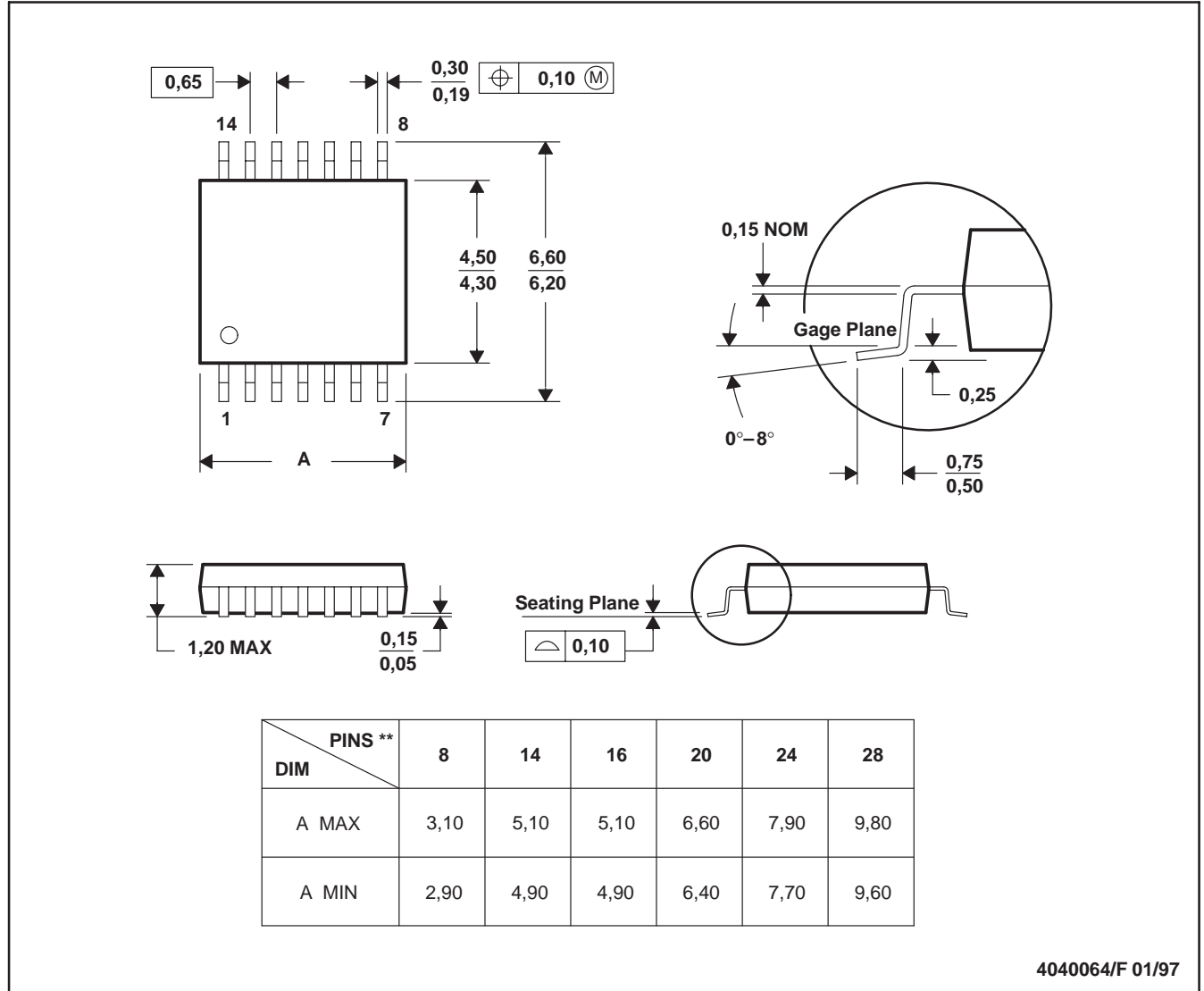   D. Falls within JEDEC MO-150

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MECHANICAL DATA

PW (R-PDSO-G**) **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

	PINS **	8	14	16	20	24	28
DIM							
A MAX		3,10	5,10	5,10	6,60	7,90	9,80
A MIN		2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

TEXAS INSTRUMENTS

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Mailing Address: Texas Instruments
                                  Post Office Box 655303 Dallas, Texas 75265

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