

**INTEGRATED CIRCUITS**

# DATA SHEET

## **74AHC573; 74AHCT573**

**Octal D-type transparent latch;  
3-state**

Product specification  
File under Integrated Circuits, IC06

1999 Sep 27

## Octal D-type transparent latch; 3-state

## 74AHC573; 74AHCT573

## FEATURES

- ESD protection:  
HBM EIA/JESD22-A114-A  
exceeds 2000 V  
MM EIA/JESD22-A115-A  
exceeds 200 V  
CDM EIA/JESD22-C101  
exceeds 1000 V
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Common 3-state output enable input
- Functionally identical to the '563' and '373'
- Inputs accepts voltages higher than  $V_{CC}$
- For AHC only:  
operates with CMOS input levels
- For AHCT only:  
operates with TTL input levels
- Specified from  
-40 to +85 and +125 °C.

## DESCRIPTION

The 74AHC/AHCT573 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7A.

The 74AHC/AHCT573 are octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A Latch Enable (LE) input and an Output Enable ( $\overline{OE}$ ) input are common to all latches.

The '573' consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When  $\overline{OE}$  is LOW, the contents of the 8 latches are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high-impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the latches.

The '573' is functionally identical to the '533', '563' and '373', but the '533' and '563' have inverted outputs and the '563' and '373' have a different pin arrangement.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ °C}$ ;  $t_r = t_f \leq 3.0\text{ ns}$ .

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			AHC	AHCT	
$t_{PHL}/t_{PLH}$	propagation delay $D_n$ to $Q_n$ ; LE to $Q_n$	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	4.2	3.9	ns
$C_I$	input capacitance	$V_I = V_{CC}$ or GND	3.0	3.0	pF
$C_O$	output capacitance		4.0	4.0	pF
$C_{PD}$	power dissipation capacitance	$C_L = 50\text{ pF}$ ; $f = 1\text{ MHz}$ ; notes 1 and 2	12	18	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs;  
 $C_L$  = output load capacitance in pF;  
 $V_{CC}$  = supply voltage in Volts.
2. The condition is  $V_I = \text{GND to } V_{CC}$ .

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## FUNCTION TABLE

See note 1.

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	$D_n$		$Q_0$ to $Q_7$
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

## Note

- H = HIGH voltage level;  
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;  
L = LOW voltage level;  
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;  
Z = high-impedance OFF-state.

## ORDERING INFORMATION

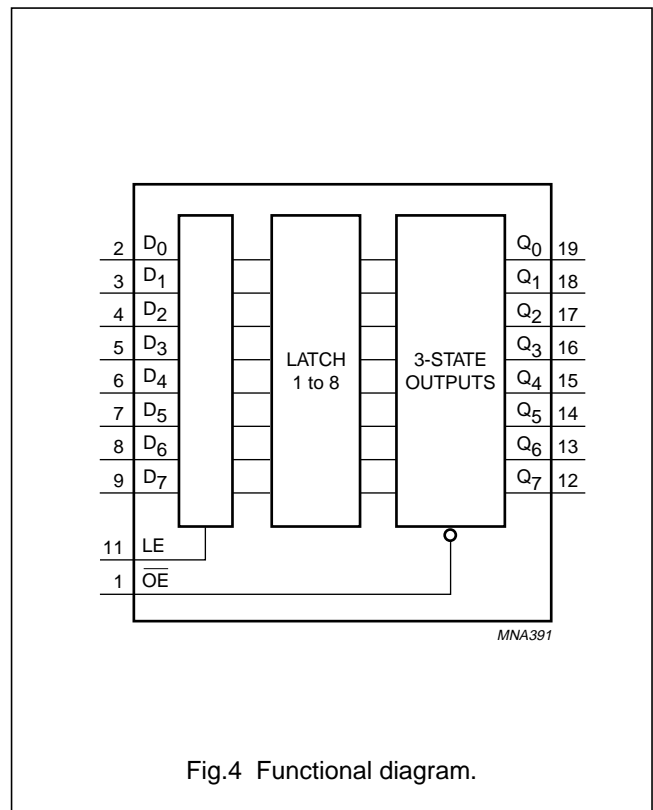
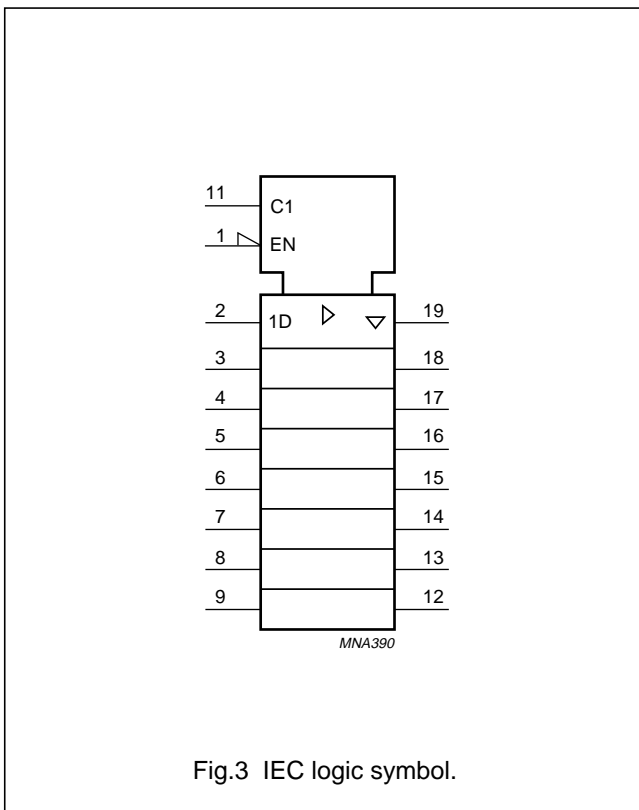
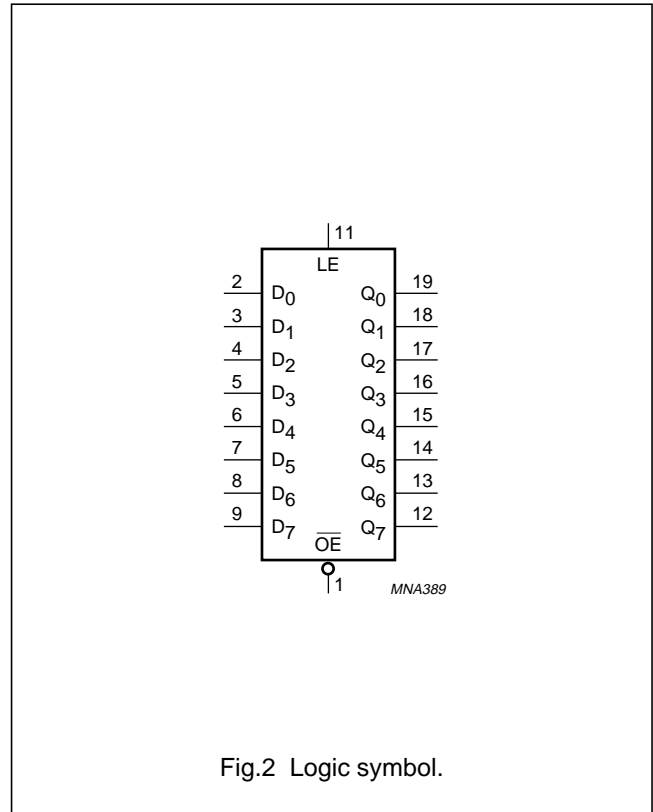
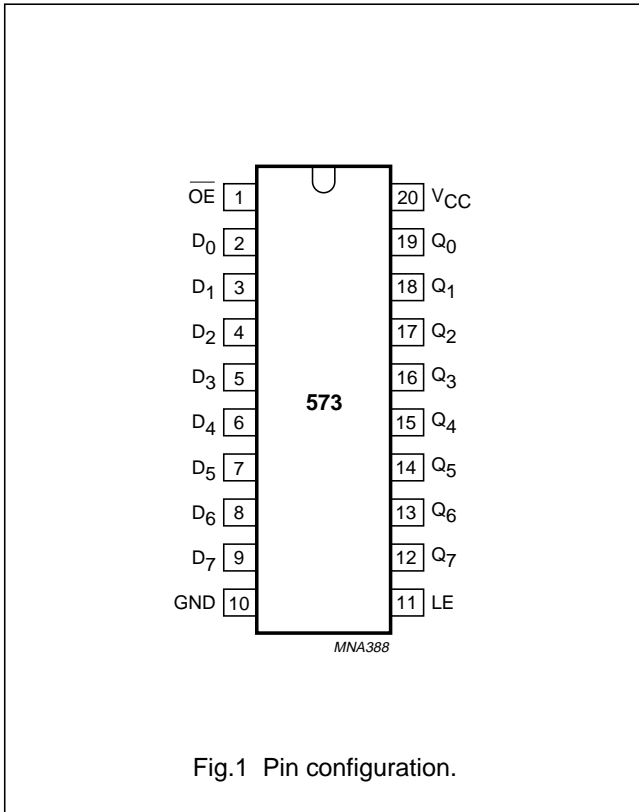
OUTSIDE NORTH AMERICA	NORTH AMERICA	PACKAGES			
		PINS	PACKAGE	MATERIAL	CODE
74AHC573D	74AHC573D	20	SO	plastic	SOT163-1
74AHC573PW	74AHC573PW DH	20	TSSOP	plastic	SOT360-1
74AHCT573D	74AHCT573D	20	SO	plastic	SOT163-1
74AHCT573PW	74AHCT573PW DH	20	TSSOP	plastic	SOT360-1

## PINNING

PIN	SYMBOL	DESCRIPTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2 to 9	$D_0$ to $D_7$	data inputs
10	GND	ground (0 V)
11	LE	latch enable input (active HIGH)
12 to 19	$Q_7$ to $Q_0$	3-state latch outputs
20	$V_{CC}$	DC supply voltage

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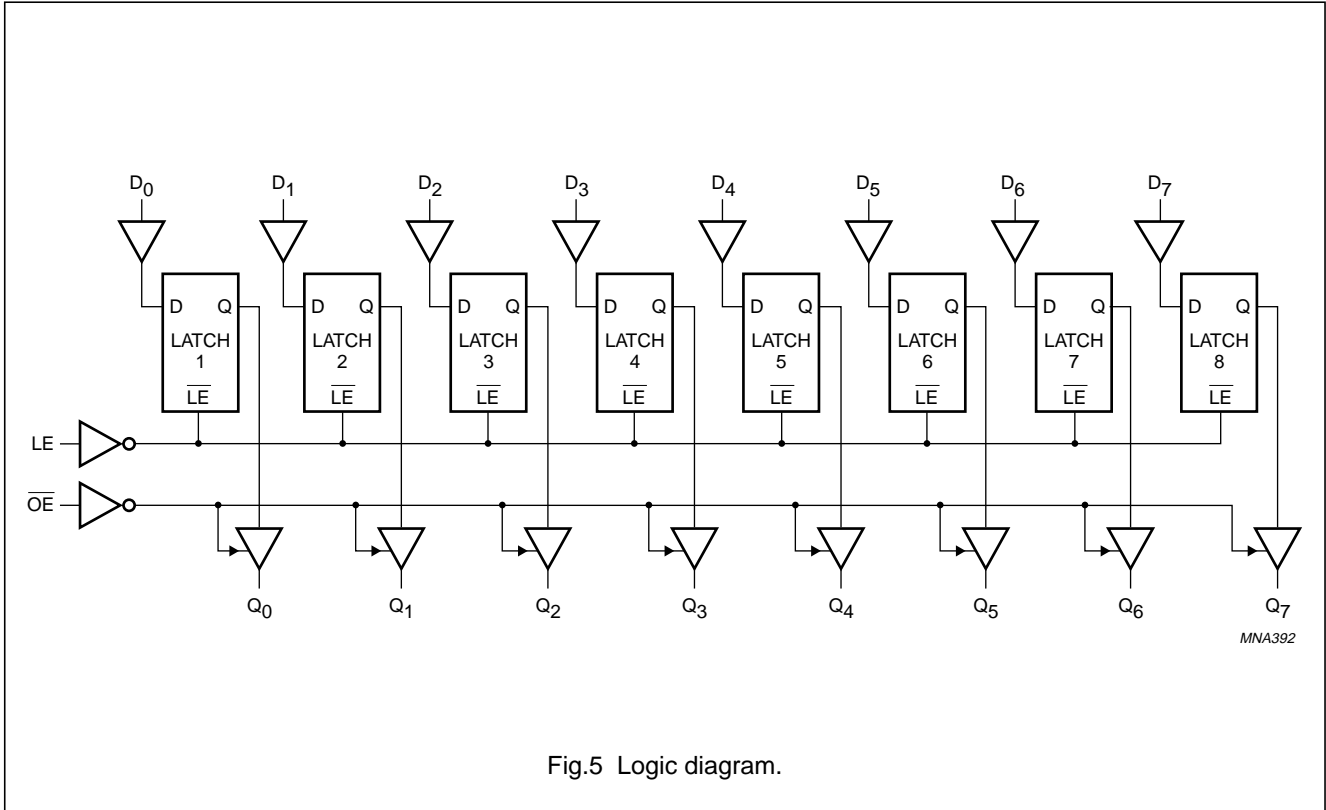


Fig.5 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC			74AHCT			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V <sub>CC</sub>	DC supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	–	5.5	0	–	5.5	V
V <sub>O</sub>	output voltage		0	–	V <sub>CC</sub>	0	–	V <sub>CC</sub>	V
T <sub>amb</sub>	operating ambient temperature range	see DC and AC characteristics per device	–40	+25	+85	–40	+25	+85	°C
			–40	+25	+125	–40	+25	+125	°C
t <sub>r</sub> , t <sub>f</sub> (Δt/Δf)	input rise and fall rates	V <sub>CC</sub> = 3.3 V ±0.3 V	–	–	100	–	–	–	ns/V
		V <sub>CC</sub> = 5 V ±0.5 V	–	–	20	–	–	20	

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	DC supply voltage		-0.5	+7.0	V
$V_I$	input voltage range		-0.5	+7.0	V
$I_{IK}$	DC input diode current	$V_I < -0.5$ V; note 1	-	-20	mA
$I_{OK}$	DC output diode current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V; note 1	-	$\pm 20$	mA
$I_O$	DC output source or sink current	$-0.5$ V $< V_O < V_{CC} + 0.5$ V	-	$\pm 25$	mA
$I_{CC}$	DC $V_{CC}$ or GND current		-	$\pm 75$	mA
$T_{stg}$	storage temperature range		-65	+150	°C
$P_D$	power dissipation per package	for temperature range: -40 to +125 °C; note 2	-	500	mW

**Notes**

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO packages: above 70 °C the value of  $P_D$  derates linearly with 8 mW/K.  
For TSSOP packages: above 60 °C the value of  $P_D$  derates linearly with 5.5 mW/K.

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## DC CHARACTERISTICS

## 74AHC family

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	T <sub>amb</sub> (°C)								UNIT	
			OTHER	V <sub>CC</sub> (V)	25			-40 to +85		-40 to +125		
					MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	–	–	1.5	–	1.5	–	V	
			3.0	2.1	–	–	2.1	–	2.1	–		
			5.5	3.85	–	–	3.85	–	3.85	–		
V <sub>IL</sub>	LOW-level input voltage		2.0	–	–	0.5	–	0.5	–	0.5	V	
			3.0	–	–	0.9	–	0.9	–	0.9		
			5.5	–	–	1.65	–	1.65	–	1.65		
V <sub>OH</sub>	HIGH-level output voltage; all outputs	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -50 µA	2.0	1.9	2.0	–	1.9	–	1.9	–	V	
			3.0	2.9	3.0	–	2.9	–	2.9	–		
			4.5	4.4	4.5	–	4.4	–	4.4	–		
	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -4.0 mA	3.0	2.58	–	–	2.48	–	2.40	–	V	
			4.5	3.94	–	–	3.8	–	3.70	–		
V <sub>OL</sub>	LOW-level output voltage; all outputs	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 50 µA	2.0	–	0	0.1	–	0.1	–	0.1	V	
			3.0	–	0	0.1	–	0.1	–	0.1		
			4.5	–	0	0.1	–	0.1	–	0.1		
	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 4 mA	3.0	–	–	0.36	–	0.44	–	0.55	V	
			4.5	–	–	0.36	–	0.44	–	0.55		
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	0.1	–	1.0	–	2.0	µA	
I <sub>OZ</sub>	3-state output OFF current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	–	–	±0.25	–	±2.5	–	±10.0	µA	
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	4.0	–	40	–	80	µA	
C <sub>I</sub>	input capacitance		–	–	3	10	–	10	–	10	pF	

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**74AHCT family**

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T <sub>amb</sub> (°C)						UNIT	
		OTHER	V <sub>CC</sub> (V)	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	2.0	–	2.0	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	–	0.8	–	0.8	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage; all outputs	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –50 µA	4.5	4.4	4.5	–	4.4	–	4.4	–	V
	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –8.0 mA	4.5	3.94	–	–	3.8	–	3.70	–	V
V <sub>OL</sub>	LOW-level output voltage; all outputs	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 50 µA	4.5	–	0	0.1	–	0.1	–	0.1	V
	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 8 mA	4.5	–	–	0.36	–	0.44	–	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	5.5	–	–	0.1	–	1.0	–	2.0	µA
I <sub>OZ</sub>	3-state output OFF current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND per input pin; other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	±0.25	–	±2.5	–	±10.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	4.0	–	40	–	80	µA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> – 2.1 V other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0	4.5 to 5.5	–	–	1.35	–	1.5	–	1.5	mA
C <sub>I</sub>	input capacitance		–	–	3	10	–	10	–	10	pF



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## AC CHARACTERISTICS

## 74AHC573

GND = 0 V;  $t_r = t_f \leq 3.0$  ns.

SYMBOL	PARAMETER	TEST CONDITIONS		$T_{amb}$ (°C)						UNIT	
		WAVEFORMS	$C_L$	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
<b><math>V_{CC} = 3.0</math> to <math>3.6</math> V; note 1</b>											
$t_{PHL}/t_{PLH}$	propagation delay $D_n$ to $Q_n$	see Figs 6 and 9	15 pF	–	5.5	11.0	1.0	13.0	1.0	14.0	ns
	propagation delay LE to $Q_n$	see Figs 7 and 9		–	5.8	11.9	1.0	14.0	1.0	15.0	ns
$t_{PZH}/t_{PZL}$	propagation delay $\overline{OE}$ to $Q_n$	see Figs 8 and 9		–	5.8	11.5	1.0	13.5	1.0	14.5	ns
$t_{PHZ}/t_{PLZ}$	propagation delay $\overline{OE}$ to $Q_n$			–	6.8	11.0	1.0	13.0	1.0	14.0	ns
$t_{PHL}/t_{PLH}$	propagation delay $D_n$ to $Q_n$	see Figs 6 and 9	50 pF	–	7.8	14.5	1.0	16.5	1.0	18.5	ns
	propagation delay LE to $Q_n$	see Figs 7 and 9		–	8.3	15.4	1.0	17.5	1.0	19.5	ns
$t_{PZH}/t_{PZL}$	propagation delay $\overline{OE}$ to $Q_n$	see Figs 8 and 9		–	8.3	15.0	1.0	17.0	1.0	19.0	ns
$t_{PHZ}/t_{PLZ}$	propagation delay $\overline{OE}$ to $Q_n$			–	9.7	14.5	1.0	16.5	1.0	18.5	ns
$t_W$	enable pulse width HIGH	see Figs 7 and 9		5.0	–	–	5.0	–	5.0	–	ns
$t_{su}$	set-up time $D_n$ to LE	see Fig.9		3.5	–	–	3.5	–	3.5	–	ns
$t_h$	hold time $D_n$ to LE			1.5	–	–	1.5	–	1.5	–	ns

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SYMBOL	PARAMETER	TEST CONDITIONS		T <sub>amb</sub> (°C)						UNIT	
		WAVEFORMS	C <sub>L</sub>	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
<b>V<sub>CC</sub> = 4.5 to 5.5 V; note 2</b>											
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub>	see Figs 6 and 9	15 pF	–	3.9	6.8	1.0	8.0	1.0	8.5	ns
	propagation delay LE to Q <sub>n</sub>	see Figs 7 and 9		–	4.2	7.7	1.0	9.0	1.0	10.0	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	propagation delay OE to Q <sub>n</sub>	see Figs 8 and 9		–	4.4	7.7	1.0	9.0	1.0	10.0	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	propagation delay OE to Q <sub>n</sub>			–	4.6	7.7	1.0	9.0	1.0	10.0	ns
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub>	see Figs 6 and 9	50 pF	–	5.5	8.8	1.0	10.0	1.0	11.0	ns
	propagation delay LE to Q <sub>n</sub>	see Figs 7 and 9		–	5.9	9.7	1.0	11.0	1.0	12.5	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	propagation delay OE to Q <sub>n</sub>	see Figs 8 and 9		–	6.3	9.7	1.0	11.0	1.0	12.5	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	propagation delay OE to Q <sub>n</sub>			–	7.4	9.7	1.0	11.0	1.0	12.5	ns
t <sub>w</sub>	enable pulse width HIGH	see Figs 7 and 9		5.0	–	–	5.0	–	5.0	–	ns
t <sub>su</sub>	set-up time D <sub>n</sub> to LE	see Fig.9		3.5	–	–	3.5	–	3.5	–	ns
t <sub>h</sub>	hold time D <sub>n</sub> to LE			1.5	–	–	1.5	–	1.5	–	ns

**Notes**

1. Typical values at V<sub>CC</sub> = 3.3 V.
2. Typical values at V<sub>CC</sub> = 5.0 V.

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**74AHCT573**GND = 0 V;  $t_r = t_f \leq 3.0$  ns.

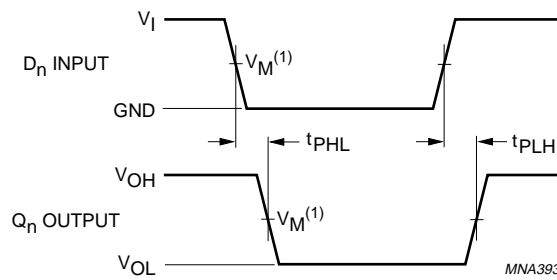
SYMBOL	PARAMETER	TEST CONDITIONS		$T_{amb}$ (°C)						UNIT	
		WAVEFORMS	$C_L$	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
<b><math>V_{CC} = 4.5</math> to <math>5.5</math> V; note 1</b>											
$t_{PHL}/t_{PLH}$	propagation delay $D_n$ to $Q_n$	see Figs 6 and 9	15 pF	–	3.5	5.5	1	6.5	1	7.0	ns
	propagation delay LE to $Q_n$	see Figs 7 and 9		–	3.9	6.0	1	7.0	1	7.5	ns
$t_{PZH}/t_{PZL}$	propagation delay OE to $Q_n$	see Figs 8 and 9		–	4.1	6.5	1	7.5	1	8.5	ns
$t_{PHZ}/t_{PLZ}$	propagation delay OE to $Q_n$			–	4.5	6.5	1	7.5	1	8.5	ns
$t_{PHL}/t_{PLH}$	propagation delay $D_n$ to $Q_n$	see Figs 6 and 9	50 pF	–	4.9	7.5	1	8.5	1	9.5	ns
	propagation delay LE to $Q_n$	see Figs 7 and 9		–	5.5	8.5	1	9.5	1	11.0	ns
$t_{PZH}/t_{PZL}$	propagation delay OE to $Q_n$	see Figs 8 and 9		–	5.9	8.5	1	10.0	1	11.0	ns
$t_{PHZ}/t_{PLZ}$	propagation delay OE to $Q_n$			–	6.4	9.0	1	10.0	1	11.5	ns
$t_W$	enable pulse width HIGH	see Figs 7 and 9		5.0	–	–	5.0	–	5.0	–	ns
$t_{su}$	set-up time $D_n$ to LE	see Fig.9		3.5	–	–	3.5	–	3.5	–	ns
$t_h$	hold time $D_n$ to LE			1.5	–	–	1.5	–	1.5	–	ns

**Note**1. Typical values at  $V_{CC} = 5.0$  V.

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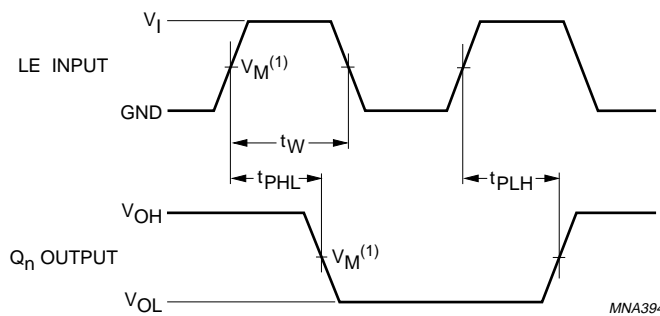
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AC WAVEFORMS



FAMILY	V <sub>I</sub> INPUT REQUIREMENTS	V <sub>M</sub> <sup>(1)</sup> INPUT	V <sub>M</sub> <sup>(1)</sup> OUTPUT
AHC	GND to V <sub>CC</sub>	50% V <sub>CC</sub>	50% V <sub>CC</sub>
AHCT	GND to 3.0 V	1.5 V	50% V <sub>CC</sub>

Fig.6 The data input (D<sub>n</sub>) to output (Q<sub>n</sub>) propagation delays.

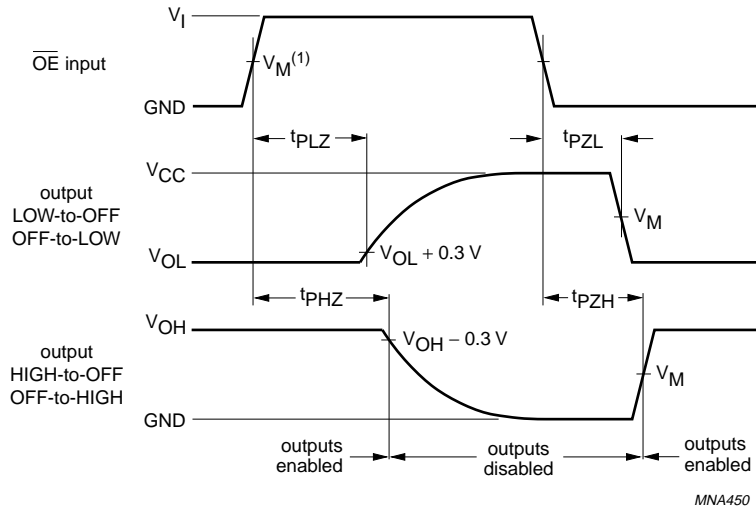


FAMILY	V <sub>I</sub> INPUT REQUIREMENTS	V <sub>M</sub> <sup>(1)</sup> INPUT	V <sub>M</sub> <sup>(1)</sup> OUTPUT
AHC	GND to V <sub>CC</sub>	50% V <sub>CC</sub>	50% V <sub>CC</sub>
AHCT	GND to 3.0 V	1.5 V	50% V <sub>CC</sub>

Fig.7 The latch enable input (LE) pulse width, the latch enable input to output (Q<sub>n</sub>) propagation delays.

Octal D-type transparent latch; 3-state

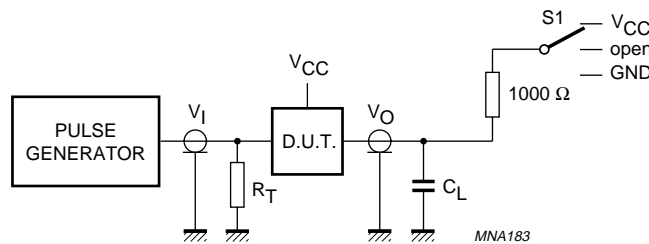
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MNA450

FAMILY	V <sub>I</sub> INPUT REQUIREMENTS	V <sub>M</sub> <sup>(1)</sup> INPUT	V <sub>M</sub> <sup>(1)</sup> OUTPUT
AHC	GND to V <sub>CC</sub>	50% V <sub>CC</sub>	50% V <sub>CC</sub>
AHCT	GND to 3.0 V	1.5 V	50% V <sub>CC</sub>

Fig.8 The 3-state enable and disable times.



MNA183

TEST	S <sub>1</sub>
t <sub>PLH</sub> /t <sub>PHL</sub>	open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>CC</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

Fig.9 Load circuitry for switching times.

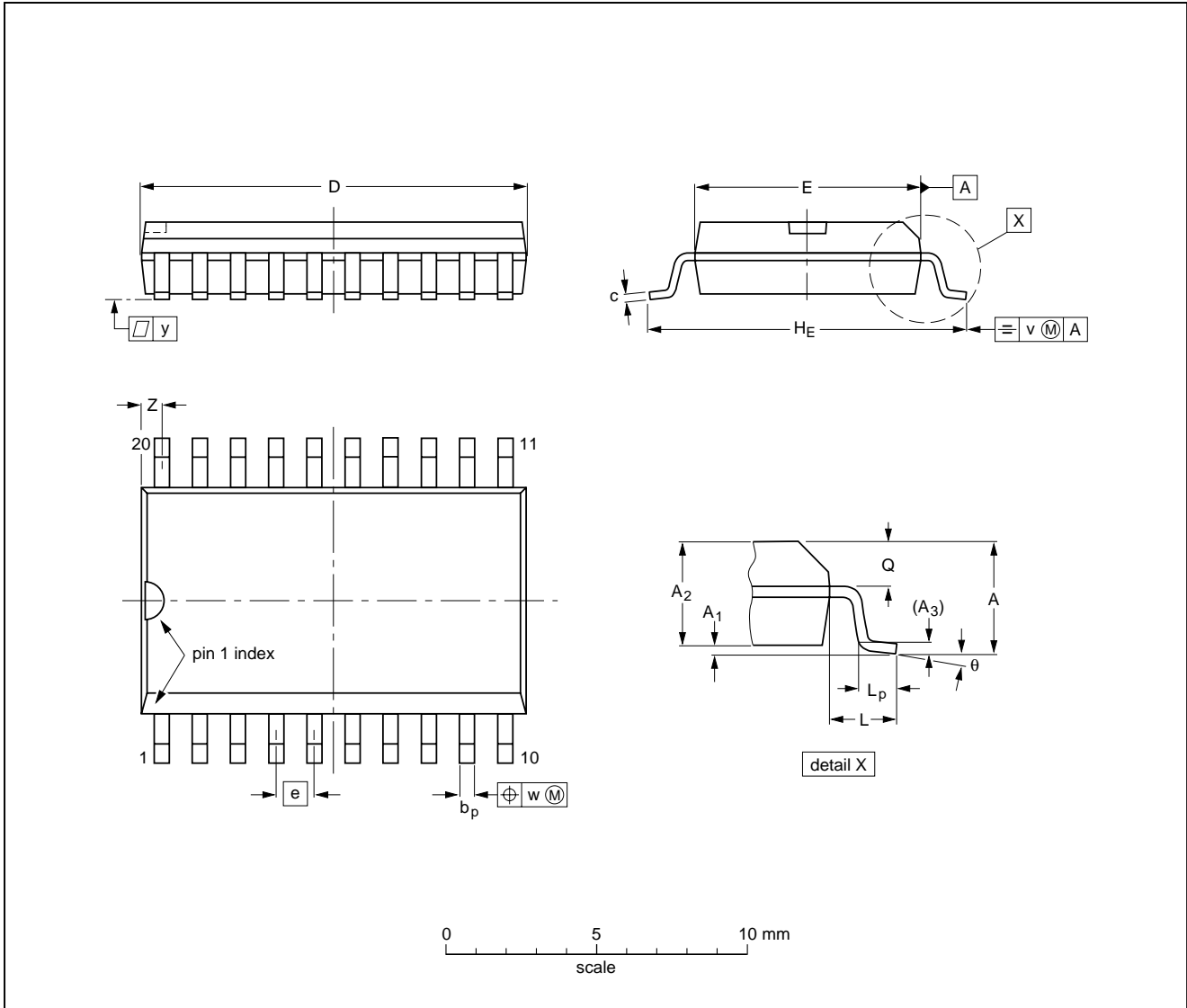
Octal D-type transparent latch; 3-state

74AHC573; 74AHCT573

PACKAGE OUTLINES

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	$\theta$
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

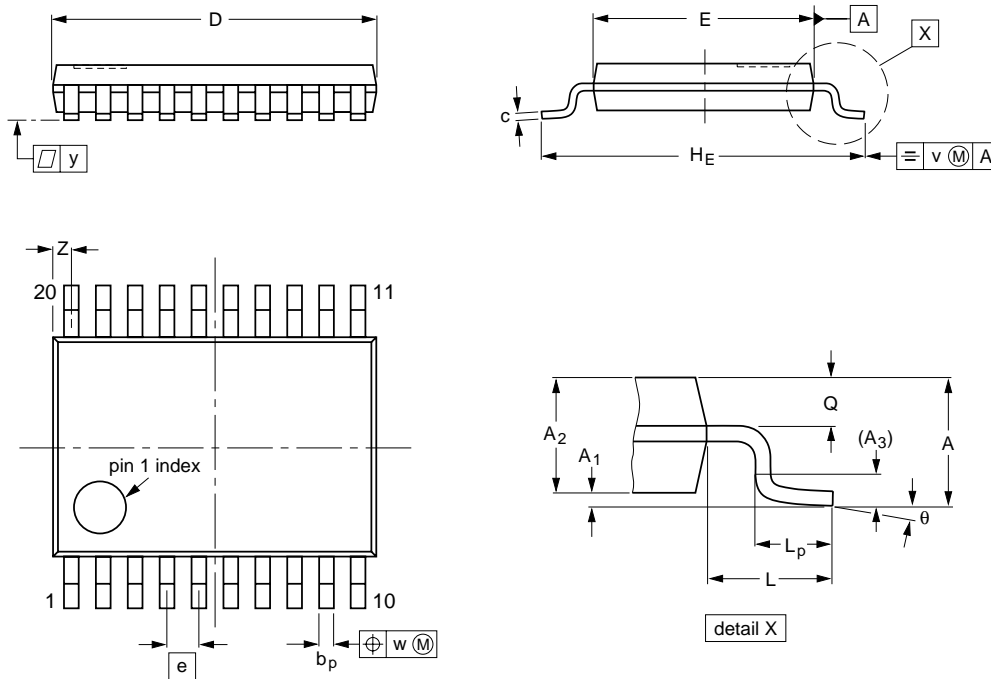
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT163-1	075E04	MS-013AC			95-01-24 97-05-22

Octal D-type transparent latch; 3-state

74AHC573; 74AHCT573

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				93-06-16 95-02-04

## Octal D-type transparent latch; 3-state

## 74AHC573; 74AHCT573

**SOLDERING****Introduction to soldering surface mount packages**

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

**Reflow soldering**

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

**Wave soldering**

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

**Manual soldering**

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.



## Octal D-type transparent latch; 3-state

## 74AHC573; 74AHCT573

**Suitability of surface mount IC packages for wave and reflow soldering methods**

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW <sup>(1)</sup>
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable <sup>(2)</sup>	suitable
PLCC <sup>(3)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(3)(4)</sup>	suitable
SSOP, TSSOP, VSO	not recommended <sup>(5)</sup>	suitable

**Notes**

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

**DEFINITIONS**

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Octal D-type transparent latch; 3-state

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**NOTES**

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**NOTES**

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