

intersil

CD4517BMS

CMOS Dual 64-Stage Static Shift Register

December 1992

Features

- High-Voltage Types (20-Volt Rating)
- Low Quiescent Current - 10nA/pkg (Typ.) at VDD = 5V
- Clock Frequency 12MHz (Typ.) at VDD = 10V
- Schmitt Trigger Clock Inputs Allow Operation with Very Slow Clock Rise and Fall Times
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load, or Two HTL Loads
- 3-State Outputs
- 100% Tested for Quiescent Current at 20V
- Standardized, Symmetrical Output Characteristics
- 5V, 10V, and 15V Parametric Ratings
- Meets all Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Time-delay Circuits
- Scratch-pad Memories
- General-purpose Serial Shift-register Applications

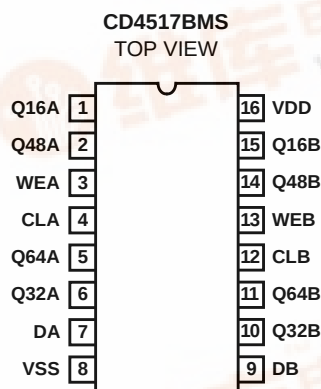
Description

CD4517BMS dual 64-stage static shift register consists of two independent registers each having a clock, data, and write enable input and outputs accessible at taps following the 16th, 32nd, 48th, and 64th stages. These taps also serve as input points allowing data to be inputted at the 17th, 33rd, and 49th stages when the write enable input is a logic 1 and the clock goes through a low-to-high transition. The truth table indicates how the clock and write enable inputs control the operation of the CD4517BMS. Inputs at the intermediate taps allow entry of 64 bits into the register with 16 clock pulses. The 3-state outputs permit connection of this device to an external bus.

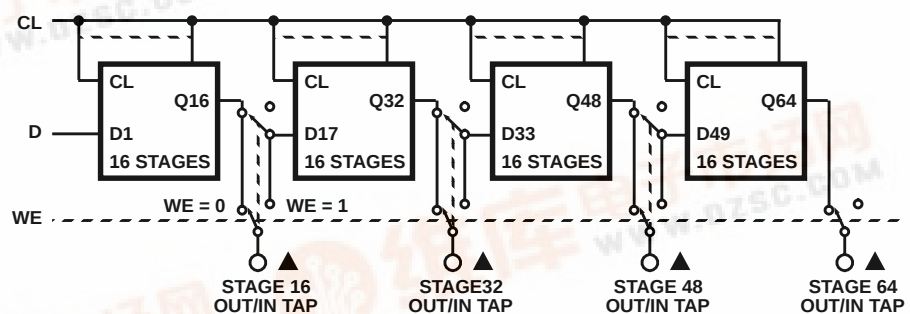
The CD4517BMS is supplied in these 16 lead outline packages:

Braze Seal DIP	H4X
Frit Seal DIP	H1F
Ceramic Flatpack	H6P

Pinout



Functional Diagram



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Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) -0.5V to +20V
 (Voltage Referenced to VSS Terminals)
 Input Voltage Range, All Inputs -0.5V to VDD +0.5V
 DC Input Current, Any One Input $\pm 10\text{mA}$
 Operating Temperature Range -55°C to $+125^{\circ}\text{C}$
 Package Types D, F, K, H
 Storage Temperature Range (TSTG) -65°C to $+150^{\circ}\text{C}$
 Lead Temperature (During Soldering) $+265^{\circ}\text{C}$
 At Distance $1/16 \pm 1/32$ Inch ($1.59\text{mm} \pm 0.79\text{mm}$) from case for
 10s Maximum

Reliability Information

Thermal Resistance θ_{ja} θ_{jc}
 Ceramic DIP and FRIT Package 80°C/W 20°C/W
 Flatpack Package 70°C/W 20°C/W
 Maximum Package Power Dissipation (PD) at $+125^{\circ}\text{C}$
 For $T_A = -55^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ (Package Type D, F, K) 500mW
 For $T_A = +100^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ (Package Type D, F, K) Derate
 Linearity at $12\text{mW}/^{\circ}\text{C}$ to 200mW
 Device Dissipation per Output Transistor 100mW
 For $T_A = \text{Full Package Temperature Range (All Package Types)}$
 Junction Temperature $+175^{\circ}\text{C}$

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
						MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	$+25^{\circ}\text{C}$	-	10	μA
				2	$+125^{\circ}\text{C}$	-	1000	μA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	μA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	$+25^{\circ}\text{C}$	-100	-	nA
				2	$+125^{\circ}\text{C}$	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	$+25^{\circ}\text{C}$	-	100	nA
				2	$+125^{\circ}\text{C}$	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	$+25^{\circ}\text{C}, +125^{\circ}\text{C}, -55^{\circ}\text{C}$	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	$+25^{\circ}\text{C}, +125^{\circ}\text{C}, -55^{\circ}\text{C}$	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	$+25^{\circ}\text{C}$	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	$+25^{\circ}\text{C}$	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	$+25^{\circ}\text{C}$	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	$+25^{\circ}\text{C}$	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	$+25^{\circ}\text{C}$	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	$+25^{\circ}\text{C}$	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	$+25^{\circ}\text{C}$	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = $-10\mu\text{A}$		1	$+25^{\circ}\text{C}$	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = $10\mu\text{A}$		1	$+25^{\circ}\text{C}$	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	$+25^{\circ}\text{C}$	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	$+25^{\circ}\text{C}$			
		VDD = 18V, VIN = VDD or GND		8A	$+125^{\circ}\text{C}$			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	$+25^{\circ}\text{C}, +125^{\circ}\text{C}, -55^{\circ}\text{C}$	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	$+25^{\circ}\text{C}, +125^{\circ}\text{C}, -55^{\circ}\text{C}$	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	$+25^{\circ}\text{C}, +125^{\circ}\text{C}, -55^{\circ}\text{C}$	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	$+25^{\circ}\text{C}, +125^{\circ}\text{C}, -55^{\circ}\text{C}$	11	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	$+25^{\circ}\text{C}$	-0.4	-	μA
				2	$+125^{\circ}\text{C}$	-12	-	μA
			VDD = 18V	3	-55°C	-0.4	-	μA
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	$+25^{\circ}\text{C}$	-	0.4	μA
				2	$+125^{\circ}\text{C}$	-	12	μA
			VDD = 18V	3	-55°C	-	0.4	μA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented. 3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.
 2. Go/No Go test with limits applied to inputs.

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TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (Note 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Clock to 16	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	3	-	MHz
			10, 11	+125°C, -55°C	2.22	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	μA
				+125°C	-	150	μA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	μA
				+125°C	-	300	μA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	μA
				+125°C	-	600	μA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V

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TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Clock to Q16	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	220	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Propagation Delay 3-State WE to Q16	TPHZ, ZH TPLZ, ZL	VDD = 5V	1, 2, 5	+25°C	-	150	ns
		VDD = 10V	1, 2, 4	+25°C	-	80	ns
		VDD = 15V	1, 2, 4	+25°C	-	60	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2	+25°C	6	-	MHz
		VDD = 15V	1, 2	+25°C	8	-	MHz
Minimum Data to Clock Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	20	ns
		VDD = 10V	1, 2, 3	+25°C	-	10	ns
		VDD = 15V	1, 2, 3	+25°C	-	10	ns
Minimum Data to Clock Hold Time	TH	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	180	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Write Enable - to-Clock Release Time	TR	VDD = 5V	1, 2, 3	+25°C	-	100	ns
		VDD = 10V	1, 2, 3	+25°C	-	50	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Write Enable-to-Clock Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	0	-	ns
		VDD = 10V	1, 2, 3	+25°C	0	-	ns
		VDD = 15V	1, 2, 3	+25°C	0	-	ns
Maximum Clock Input Rise and Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3, 5	+25°C	-	15	μs
		VDD = 10V	1, 2, 3, 5	+25°C	-	5	μs
		VDD = 15V	1, 2, 3, 5	+25°C	-	5	μs
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. Measured at the point of 10% change in output with an output load 50pF, RL = 1KΩ to VDD for TPZL and TPLZ and RL = 1KΩ to VSS for TPZH and TPHZ
5. If more than one unit is cascaded, TRCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	μA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10μA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	0.2	2.8	V

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TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
P Threshold Voltage Delta	ΔV_{TP}	VSS = 0V, IDD = 10 μ A	1, 4	+25°C	-	± 1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND. 3. See Table 2 for +25°C limit.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns. 4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	$\pm 1.0\mu$ A
Output Current (Sink)	IOL5	$\pm 20\%$ x Pre-Test Reading
Output Current (Source)	IOH5A	$\pm 20\%$ x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parametric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V $\pm$ -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	1, 2, 5, 6, 10, 11, 14, 15	3, 4, 7-9, 12, 13	16			
Static Burn-In 2 (Note 1)	1, 2, 5, 6, 10, 11, 14, 15	8	3, 4, 7, 9, 12, 13, 16			
Dynamic Burn-In (Note 1)	-	3, 8, 13	16	1, 2, 5, 6, 10, 11, 14, 15	4, 12	7, 9

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TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS (Continued)

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Irradiation (Note 2)	1, 2, 5, 6, 10, 11, 14, 15	8	3, 4, 7, 9, 12, 13, 16			

NOTES:

- Each pin except VDD and GND will have a series resistor of $10K \pm 5\%$, VDD = $18V \pm 0.5V$
- Each pin except VDD and GND will have a series resistor of $47K \pm 5\%$; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = $10V \pm 0.5V$

Logic Diagram

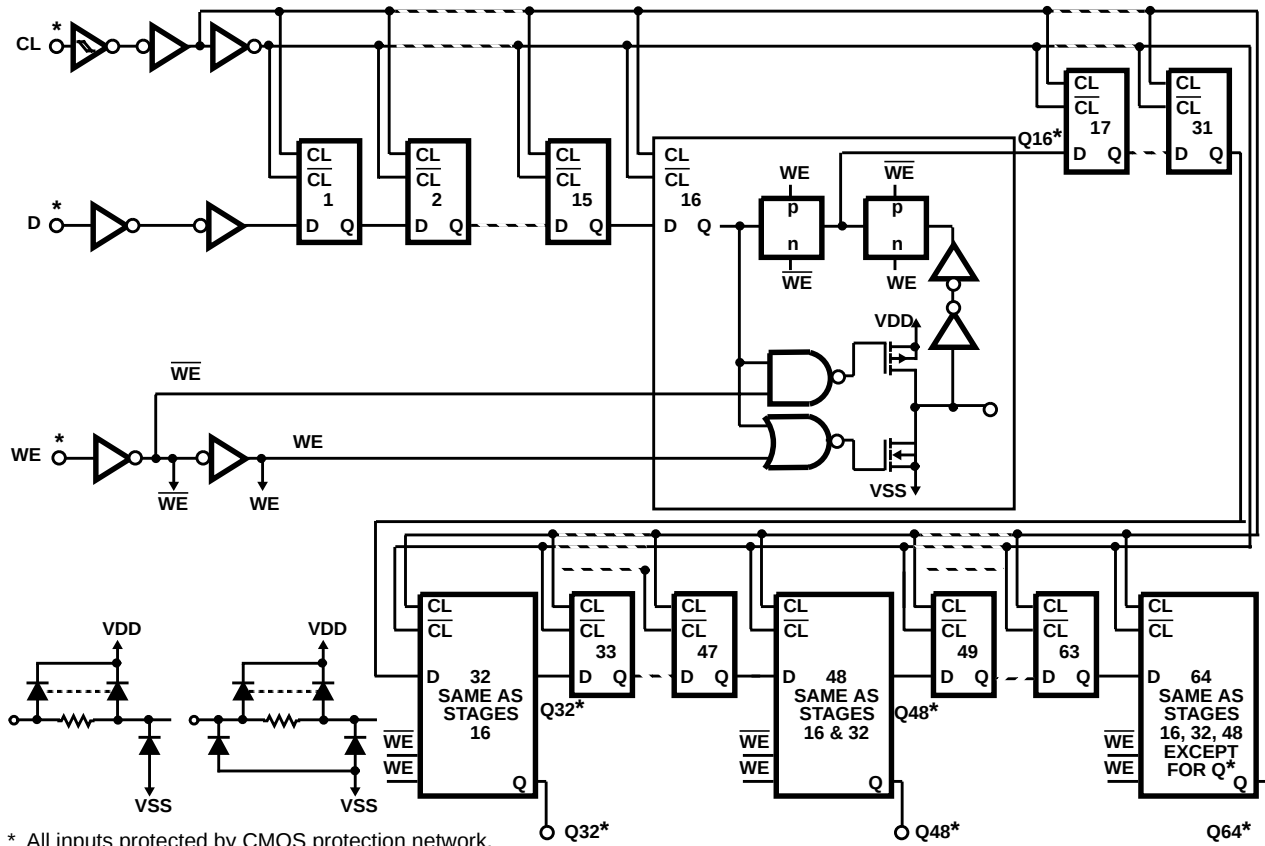


FIGURE 1. LOGIC BLOCK DIAGRAM

TRUTH TABLE

CLOCK	WRITE ENABLE	DATA	STAGE 16 TAP	STAGE 32 TAP	STAGE 48 TAP	STAGE 64 TAP
0	0	X	Q16	Q32	Q48	Q64
0	1	X	Z	Z	Z	Z
1	0	X	Q16	Q32	Q48	Q64
1	1	X	Z	Z	Z	Z
	0	DI In	Q16	Q32	Q48	Q64
	1	DI In	D17 In	D33 In	D49 In	Z
	0	X	Q16	Q32	Q48	Q64
	1	X	Z	Z	Z	Z

1 = HIGH LEVEL
0 = LOW LEVEL

X = DON'T CARE
Z = HIGH IMPEDANCE

CD4517BMS

Typical Performance Characteristics

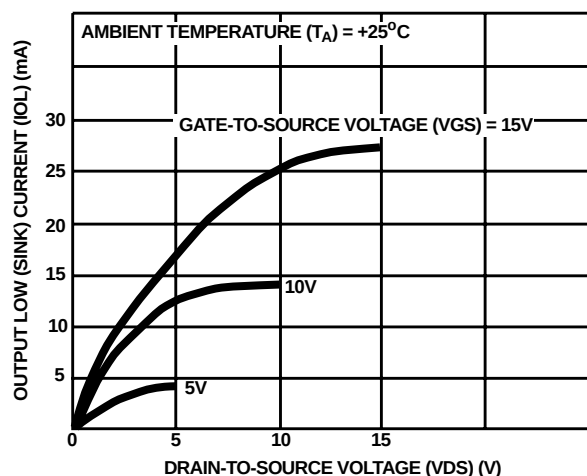


FIGURE 2. TYPICAL N-CHANNEL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

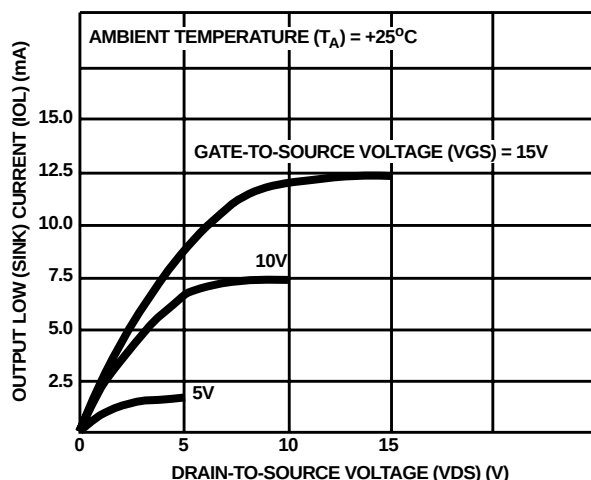


FIGURE 3. MINIMUM N-CHANNEL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

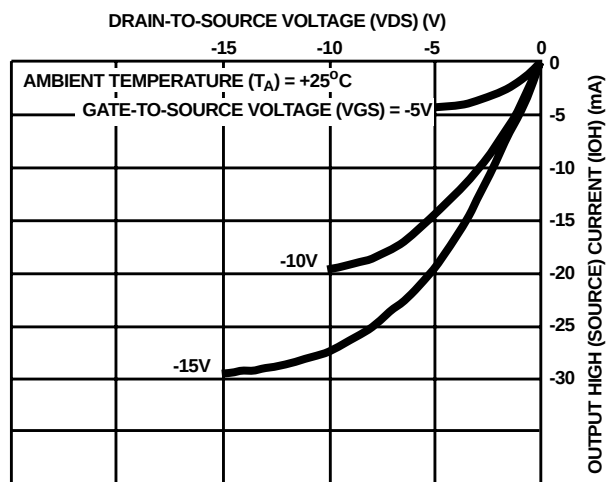


FIGURE 4. TYPICAL P-CHANNEL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

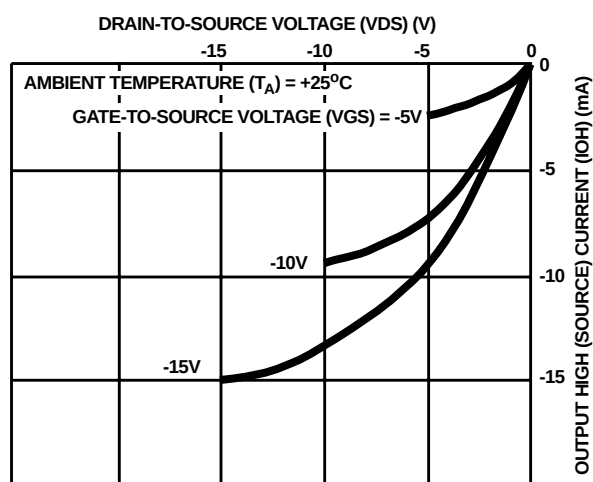


FIGURE 5. MINIMUM P-CHANNEL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

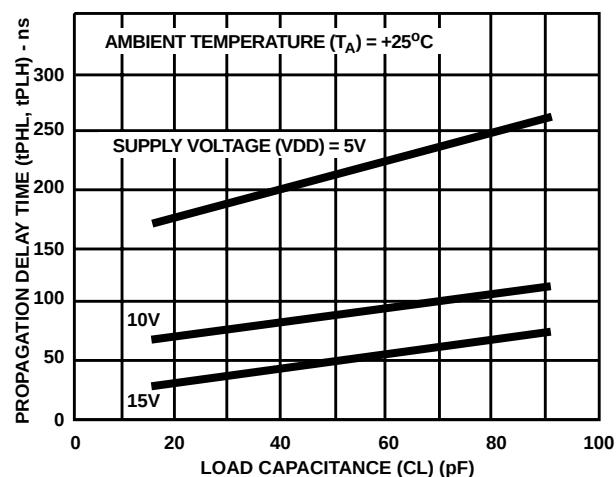


FIGURE 6. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

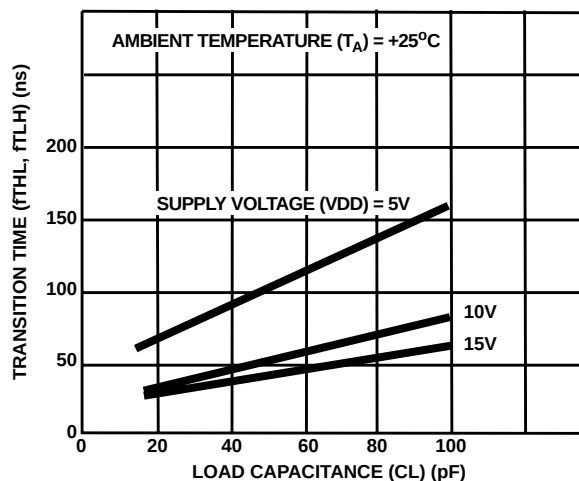


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

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Typical Performance Characteristics (Continued)

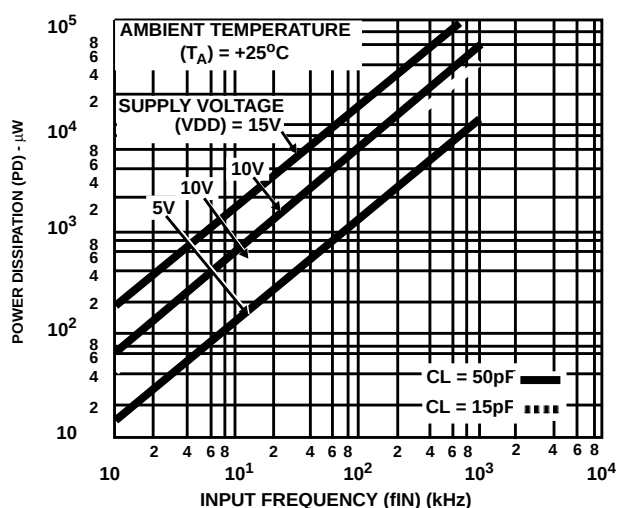


FIGURE 8. TYPICAL POWER DISSIPATION AS A FUNCTION OF FREQUENCY

Waveforms and Test Circuits

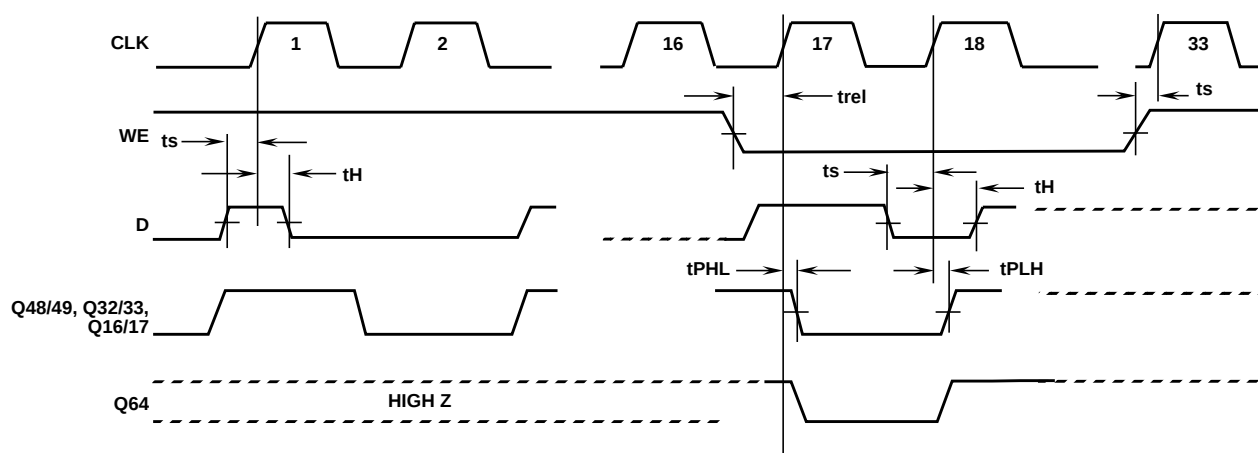


FIGURE 9. DYNAMIC TEST WAVEFORMS

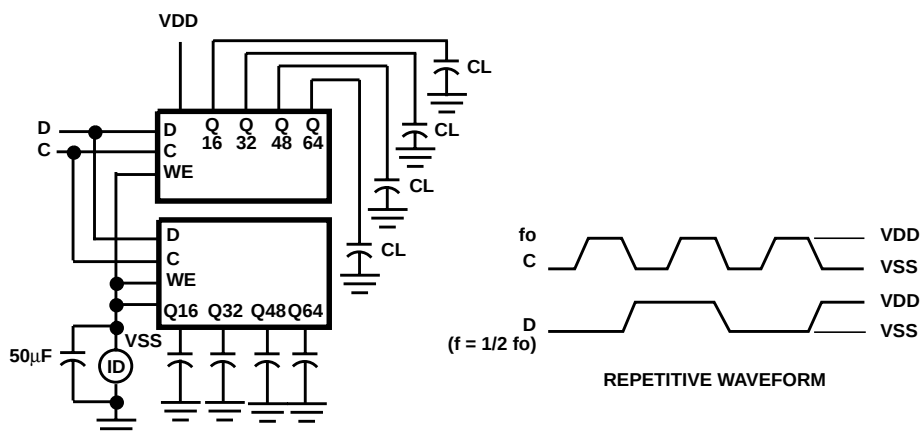
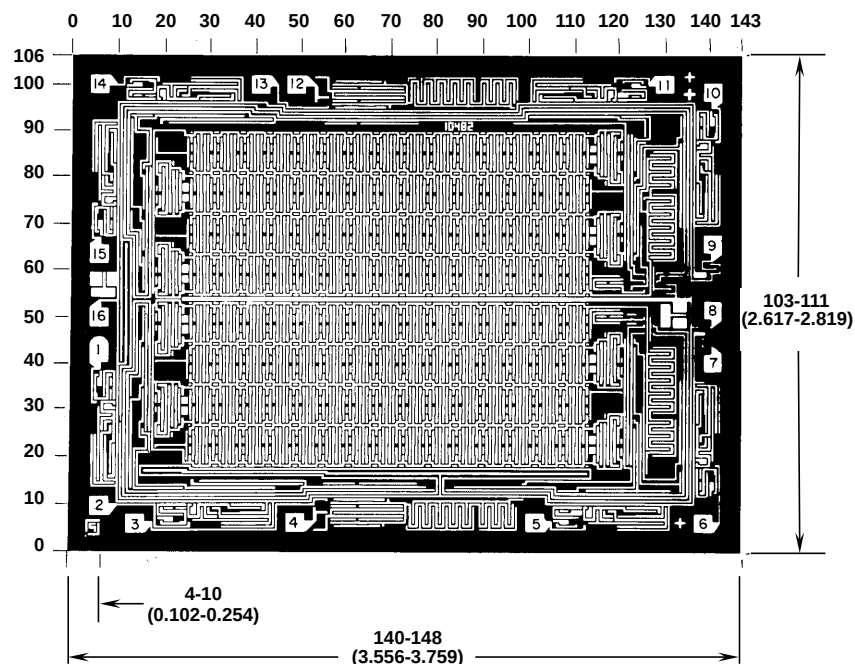


FIGURE 10. DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

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Chip Dimensions and Pad Layouts



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch.)

METALLIZATION: Thickness: $11\text{k}\text{\AA} - 14\text{k}\text{\AA}$, AL.

PASSIVATION: $10.4\text{k}\text{\AA} - 15.6\text{k}\text{\AA}$, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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