SGS-THOMSON MICROELECTRONICS

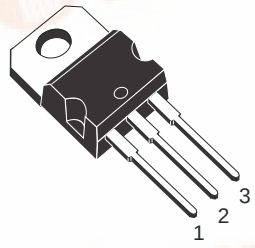
STP7NB40
STP7NB40FP

N - CHANNEL ENHANCEMENT MODE PowerMESH™ MOSFET

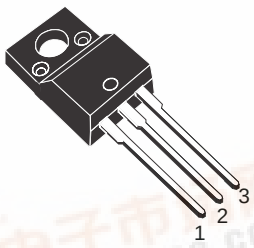
PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STP7NB40	400 V	< 0.9 Ω	7.0 A
STP7NB40FP	400 V	< 0.9 Ω	4.4 A

- TYPICAL $R_{DS(on)}$ = 0.75 Ω
- EXTREMELY HIGH dV/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED



TO-220

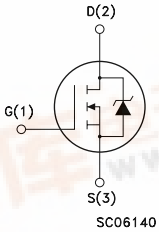


TO-220FP

DESCRIPTION

Using the latest high voltage MESH OVERLAY™ process, SGS-Thomson has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest RDS(on) per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP7NB40	STP7NB40FP	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	400		V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	400		V
V_{GS}	Gate-source Voltage	± 30		V
I_D	Drain Current (continuous) at T_c = 25 °C	7	4.4	A
I_D	Drain Current (continuous) at T_c = 100 °C	4.4	2.8	A
I_{DM}(•)	Drain Current (pulsed)	28	28	A
P_{tot}	Total Dissipation at T_c = 25 °C	100	35	W
	Derating Factor	0.8	0.28	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	4.5	4.5	V/ns
V_{ISO}	Insulation Withstand Voltage (DC)	—	2000	V
T_{stg}	Storage Temperature	-65 to 150		°C
T_j	Max. Operating Junction Temperature	150		°C

(•) Pulse width limited by safe operating area (1) $I_{SD} \le 7A$, $di/dt \le 200$ A/µs, $V_{DD} \le V_{(BR)DSS}$, $Tj \le T_{JMAX}$

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

THERMAL DATA

			TO-220	TO-220FP	
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.25	3.57	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	62.5		°C/W
$R_{thc\text{-}sink}$	Thermal Resistance Case-sink	Typ	0.5		°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	7	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	300	mJ

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA V_{GS} = 0	400			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0) V_{DS} = Max Rating V_{DS} = Max Rating T_c = 125 °C				1 50	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 30 V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V I_D = 3.5 A		0.75	0.9	Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ V_{GS} = 10 V	7			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ I_D = 3.5 A	2.5	4.2		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		705 132 17	720 175 25	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	V_{DD} = 200 V I_D = 3.5 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 3)		11.5 7.5	16 11	ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 320 V I_D = 7 A V_{GS} = 10 V		21 7.3 8.5	30	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 320 V I_D = 7 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 5)		9.5 9 16.5	15 14 25	ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(•)	Source-drain Current Source-drain Current (pulsed)				7 28	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 7 A V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 7 A di/dt = 100 A/µs V_{DD} = 100 V T_j = 150 °C (see test circuit, figure 5)		300 2 13.7		ns µC A

(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

(•) Pulse width limited by safe operating area

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