CMOS single-chip 8-bit microcontrollers 80C31/80C51/87C51

DESCRIPTION

The Philips 80C31/80C51/87C51 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. The CMOS 8XC51 is functionally compatible with the NMOS 8031/8051 microcontrollers. The Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Philips epitaxial substrate minimizes latch-up sensitivity.

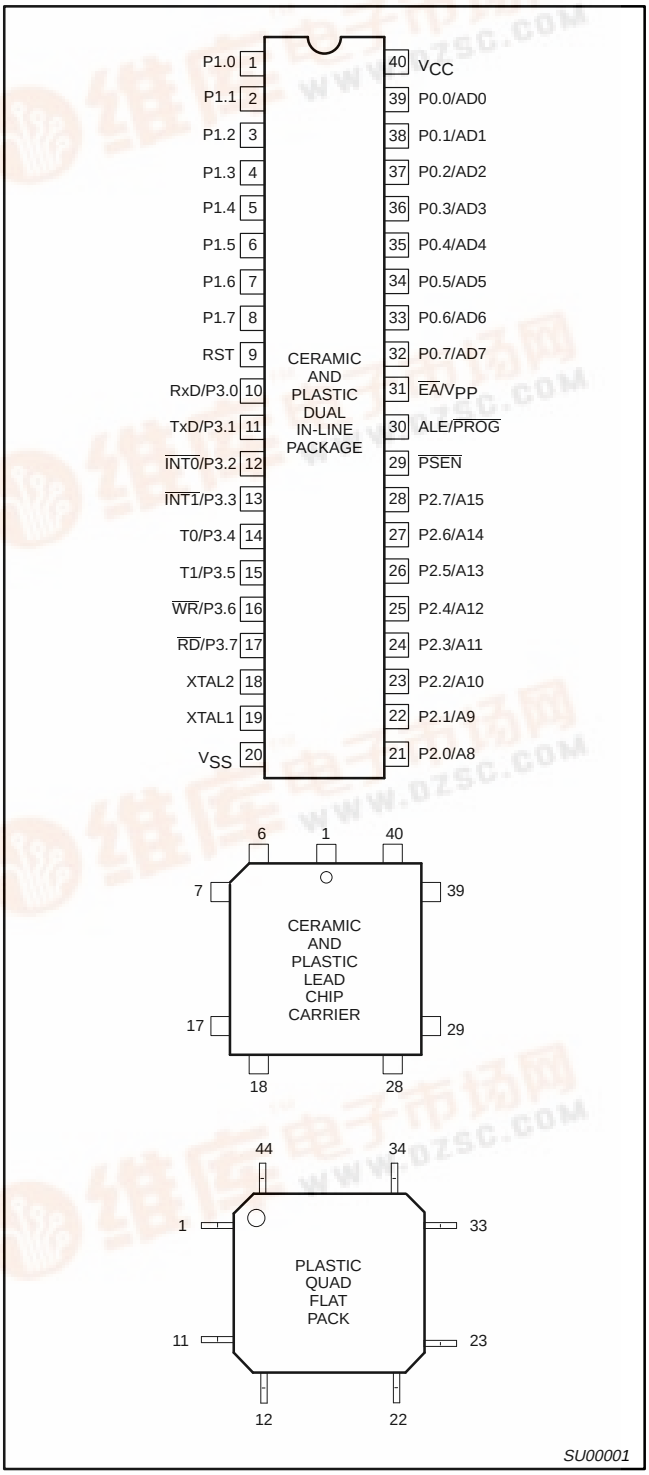
The 8XC51 contains a 4k × 8 ROM (80C51) EPROM (87C51), a 128 × 8 RAM, 32 I/O lines, two 16-bit counter/timers, a five-source, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the device has two software selectable modes of power reduction—idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

FEATURES

- 8031/8051 compatible
  - 4k × 8 ROM (80C51)
  - 4k × 8 EPROM (87C51)
  - ROMless (80C31)
  - 128 × 8 RAM
  - Two 16-bit counter/timers
  - Full duplex serial channel
  - Boolean processor
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- Five speed ranges at V_{CC} = 5V
  - 12MHz
  - 16MHz
  - 24MHz
  - 33MHz
- Five package styles
- Extended temperature ranges
- OTP package available

PIN CONFIGURATIONS



SEE PAGE 3-6 FOR QFP AND LCC PIN FUNCTIONS.

ORDERING INFORMATION

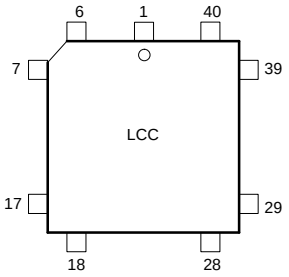
EPROM	DRAWING NUMBER	PHILIPS NORTH AMERICA				
		ROMless	ROM	DRAWING NUMBER	TEMPERATURE RANGE °C AND PACKAGE[1]	Freq MHz
SC87C51CCF40	0590B				0 to +70, Ceramic Dual In-line Package, UV	3.5 to 12
SC87C51CCK44	1472A				0 to +70, Ceramic Leaded Chip Carrier, UV	3.5 to 12
SC87C51CCN40	SOT129-1	SC80C31BCCN40	SC80C51BCCN40	SOT129-1	0 to +70, Plastic Dual In-line Package, OTP	3.5 to 12
SC87C51CCA44	SOT187-2	SC80C31BCCA44	SC80C51BCCA44	SOT187-2	0 to +70, Plastic Leaded Chip Carrier, OTP	3.5 to 12
SC87C51CCB44	SOT307-2	SC80C31BCCB44	SC80C51BCCB44	SOT307-2	0 to +70, Plastic Quad Flat Pack, OTP	3.5 to 12
SC87C51ACF40	0590B				–40 to +85, Ceramic Dual In-line Package, UV	3.5 to 12
SC87C51ACN40	SOT129-1	SC80C31BACN40	SC80C51BACN40	SOT129-1	–40 to +85, Plastic Dual In-line Package, OTP	3.5 to 12
SC87C51ACA44	SOT187-2	SC80C31BACA44	SC80C51BACA44	SOT187-2	–40 to +85, Plastic Leaded Chip Carrier, OTP	3.5 to 12
SC87C51ACB44	SOT307-2	SC80C31BACB44	SC80C51BACB44	SOT307-2	–40 to +85, Plastic Quad Flat Pack, OTP	3.5 to 12
SC87C51CGF40	0590B				0 to +70, Ceramic Dual In-line Package, UV	3.5 to 16
SC87C51CGK44	1472A				0 to +70, Ceramic Leaded Chip Carrier, UV	3.5 to 16
SC87C51CGN40	SOT129-1	SC80C31BCGN40	SC80C51BCGN40	SOT129-1	0 to +70, Plastic Dual In-line Package, OTP	3.5 to 16
SC87C51CGA44	SOT187-2	SC80C31BCGA44	SC80C51BCGA44	SOT187-2	0 to +70, Plastic Leaded Chip Carrier, OTP	3.5 to 16
SC87C51CGB44	SOT307-2	SC80C31BCGB44	SC80C51BCGB44	SOT307-2	0 to +70, Plastic Quad Flat Pack, OTP	3.5 to 16
SC87C51AGF40	0590B				–40 to +85, Ceramic Dual In-line Package, UV	3.5 to 16
SC87C51AGN40	SOT129-1	SC80C31BAGN40	SC80C51BAGN40	SOT129-1	–40 to +85, Plastic Dual In-line Package, OTP	3.5 to 16
SC87C51AGA44	SOT187-2	SC80C31BAGA44	SC80C51BAGA44	SOT187-2	–40 to +85, Plastic Leaded Chip Carrier, OTP	3.5 to 16
SC87C51AGB44	SOT307-2	SC80C31BAGB44	SC80C51BAGB44	SOT307-2	–40 to +85, Plastic Quad Flat Pack, OTP	3.5 to 16
SC87C51CPF40	0590B				0 to +70, Ceramic Dual In-line Package, UV	3.5 to 24
SC87C51CPK44	1472A				0 to +70, Ceramic Leaded Chip Carrier, UV	3.5 to 24
SC87C51CPN40	SOT129-1	SC80C31BCPN40	SC80C51BCPN40	SOT129-1	0 to +70, Plastic Dual In-line Package, OTP	3.5 to 24
SC87C51CPA44	SOT187-2	SC80C31BCPA44	SC80C51BCPA44	SOT187-2	0 to +70, Plastic Leaded Chip Carrier, OTP	3.5 to 24
SC87C51APF40	0590B				–40 to +85, Ceramic Dual In-line Package, UV	
SC87C51APN40	SOT129-1	SC80C31BAPN40	SC80C51BAPN40	SOT129-1	–40 to +85, Plastic Dual In-line Package, OTP	3.5 to 24
SC87C51APA44	SOT187-2	SC80C31BAPA44	SC80C51BAPA44	SOT187-2	–40 to +85, Plastic Leaded Chip Carrier, OTP	3.5 to 24
SC87C51CYF40	0590B				0 to +70, Ceramic Dual In-line Package, UV	3.5 to 33
SC87C51CYK44	1472A				0 to +70, Ceramic Leaded Chip Carrier, UV	3.5 to 33
SC87C51CYN40	SOT129-1	SC80C31BCYN40	SC80C51BCYN40	SOT129-1	0 to +70, Plastic Dual In-line Package, OTP	3.5 to 33
SC87C51CYA44	SOT187-2	SC80C31BCYA44	SC80C51BCYA44	SOT187-2	0 to +70, Plastic Leaded Chip Carrier, OTP	3.5 to 33

1. OTP = One Time Programmable EPROM. UV = UV Erasable EPROM
2. SOT311 replaced by SOT307-2.

ORDERING INFORMATION (Continued)

PHILIPS					
ROMless (ORDER NUMBER)	**ROMless (MARKING NUMBER)**	**ROM**	**DRAWING NUMBER**	**TEMPERATURE RANGE °C AND PACKAGE[1]**	**Freq MHz**
PCB80C31-2 N	PCB80C31BH2-12P	PCB80C51BH-2P	SOT129-1	0 to +70, Plastic Dual In-line Package, OTP	0.5 to 12
PCB80C31-2 A	PCB80C31BH2-12WP	PCB80C51BH-2WP	SOT187-2	0 to +70, Plastic Leaded Chip Carrier, OTP	0.5 to 12
	PCB80C31BH2-12H	PCB80C51BH-2H	SOT307-2[2]	0 to +70, Plastic Quad Flat Pack, OTP	0.5 to 12
PCB80C31-3 N	PCB80C31BH3-16P	PCB80C51BH-3P	SOT129-1	0 to +70, Plastic Dual In-line Package, OTP	1.2 to 16
PCB80C31-3 A	PCB80C31BH3-16WP	PCB80C51BH-3WP	SOT187-2	0 to +70, Plastic Leaded Chip Carrier, OTP	1.2 to 16
	PCB80C31BH3-16H	PCB80C51BH-3H	SOT307-2[2]	0 to +70, Plastic Quad Flat Pack, OTP	1.2 to 16
PCF80C31-3 N	PCF80C31BH3-16P	PCF80C51BH-3P	SOT129-1	–40 to +85, Plastic Dual In-line Package, OTP	1.2 to 16
PCF80C31-3 A	PCF80C31BH3-16WP	PCF80C51BH-3WP	SOT187-2	–40 to +85, Plastic Leaded Chip Carrier, OTP	1.2 to 16
	PCF80C31BH3-16H	PCF80C51BH-3H	SOT307-2[2]	–40 to +85, Plastic Quad Flat Pack, OTP	1.2 to 16
	PCA80C31BH3-16P	PCA80C51BH-3P	SOT129-1	–40 to +125, Plastic Dual In-line Package	1.2 to 16
	PCA80C31BH3-16WP	PCA80C51BH-3WP	SOT187-2	–40 to +125, Plastic Leaded Chip Carrier	1.2 to 16
PCB80C31-4 N	PCB80C31BH4-24P	PCB80C51BH-4P	SOT129-1	0 to +70, Plastic Dual In-line Package, OTP	1.2 to 24
PCB80C31-4 A	PCB80C31BH4-24WP	PCB80C51BH-4WP	SOT187-2	0 to +70, Plastic Leaded Chip Carrier, OTP	1.2 to 24
	PCB80C31BH4-24H	PCB80C51BH-4H	SOT307-2[2]	0 to +70, Plastic Quad Flat Pack, OTP	1.2 to 24
PCF80C31-4 N	PCF80C31BH4-24P	PCF80C51BH-4P	SOT129-1	–40 to +85, Plastic Dual In-line Package, OTP	1.2 to 24
PCF80C31-4 A	PCF80C31BH4-24WP	PCF80C51BH-4WP	SOT187-2	–40 to +85, Plastic Leaded Chip Carrier, OTP	1.2 to 24
	PCF80C31BH4-24H	PCF80C51BH-4H	SOT307-2[2]	–40 to +85, Plastic Leaded Chip Carrier, OTP	1.2 to 24
PCB80C31-5 N	PCB80C31BH5-30P	PCB80C51BH-5P	SOT129-1	0 to +70, Plastic Dual In-line Package	1.2 to 33
PCB80C31-5 A	PCB80C31BH5-30WP	PCB80C51BH-5WP	SOT187-2	0 to +70, Plastic Leaded Chip Carrier	1.2 to 33
PCB80C31-5 B	PCB80C31BH5-30H	PCB80C51BH-5H	SOT307-2[2]	0 to +70, Plastic Quad Flat Pack	1.2 to 33

CERAMIC AND PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS

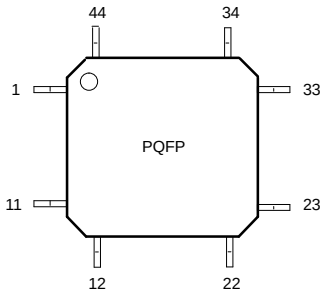


Pin	Function	Pin	Function	Pin	Function
1	NC*	16	P3.4/T0	31	P2.7/A15
2	P1.0	17	P3.5/T1	32	$\overline{PSEN}$
3	P1.1	18	P3.6/$\overline{WR}$	33	ALE/$\overline{PROG}$
4	P1.2	19	P3.7/$\overline{RD}$	34	NC*
5	P1.3	20	XTAL2	35	$\overline{EA}$/V_{PP}
6	P1.4	21	XTAL1	36	P0.7/AD7
7	P1.5	22	V_{SS}	37	P0.6/AD6
8	P1.6	23	NC*	38	P0.5/AD5
9	P1.7	24	P2.0/A8	39	P0.4/AD4
10	RST	25	P2.1/A9	40	P0.3/AD3
11	P3.0/RxD	26	P2.2/A10	41	P0.2/AD2
12	NC*	27	P2.3/A11	42	P0.1/AD1
13	P3.1/TxD	28	P2.4/A12	43	P0.0/AD0
14	P3.2/$\overline{INT0}$	29	P2.5/A13	44	V_{CC}
15	P3.3/$\overline{INT1}$	30	P2.6/A14		

* DO NOT CONNECT

SU00002

PLASTIC QUAD FLAT PACK PIN FUNCTIONS

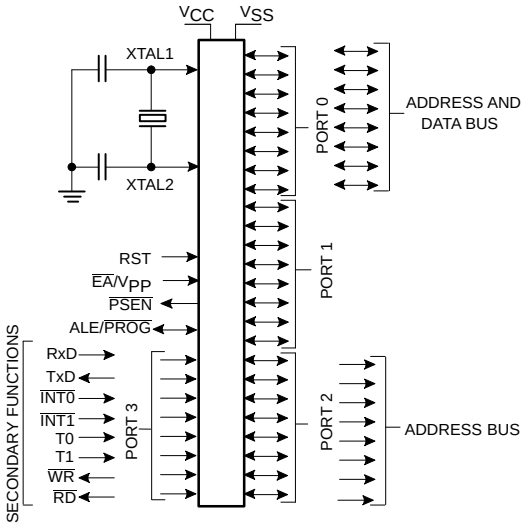


Pin	Function	Pin	Function	Pin	Function
1	P1.5	16	V_{SS}	31	P0.6/AD6
2	P1.6	17	NC*	32	P0.5/AD5
3	P1.7	18	P2.0/A8	33	P0.4/AD4
4	RST	19	P2.1/A9	34	P0.3/AD3
5	P3.0/RxD	20	P2.2/A10	35	P0.2/AD2
6	NC*	21	P2.3/A11	36	P0.1/AD1
7	P3.1/TxD	22	P2.4/A12	37	P0.0/AD0
8	P3.2/$\overline{INT0}$	23	P2.5/A13	38	V_{CC}
9	P3.3/$\overline{INT1}$	24	P2.6/A14	39	NC*
10	P3.4/T0	25	P2.7/A15	40	P1.0
11	P3.5/T1	26	$\overline{PSEN}$	41	P1.1
12	P3.6/$\overline{WR}$	27	ALE/$\overline{PROG}$	42	P1.2
13	P3.7/$\overline{RD}$	28	NC*	43	P.13
14	XTAL2	29	$\overline{EA}$/V_{PP}	44	P1.4
15	XTAL1	30	P0.7/AD7		

* DO NOT CONNECT

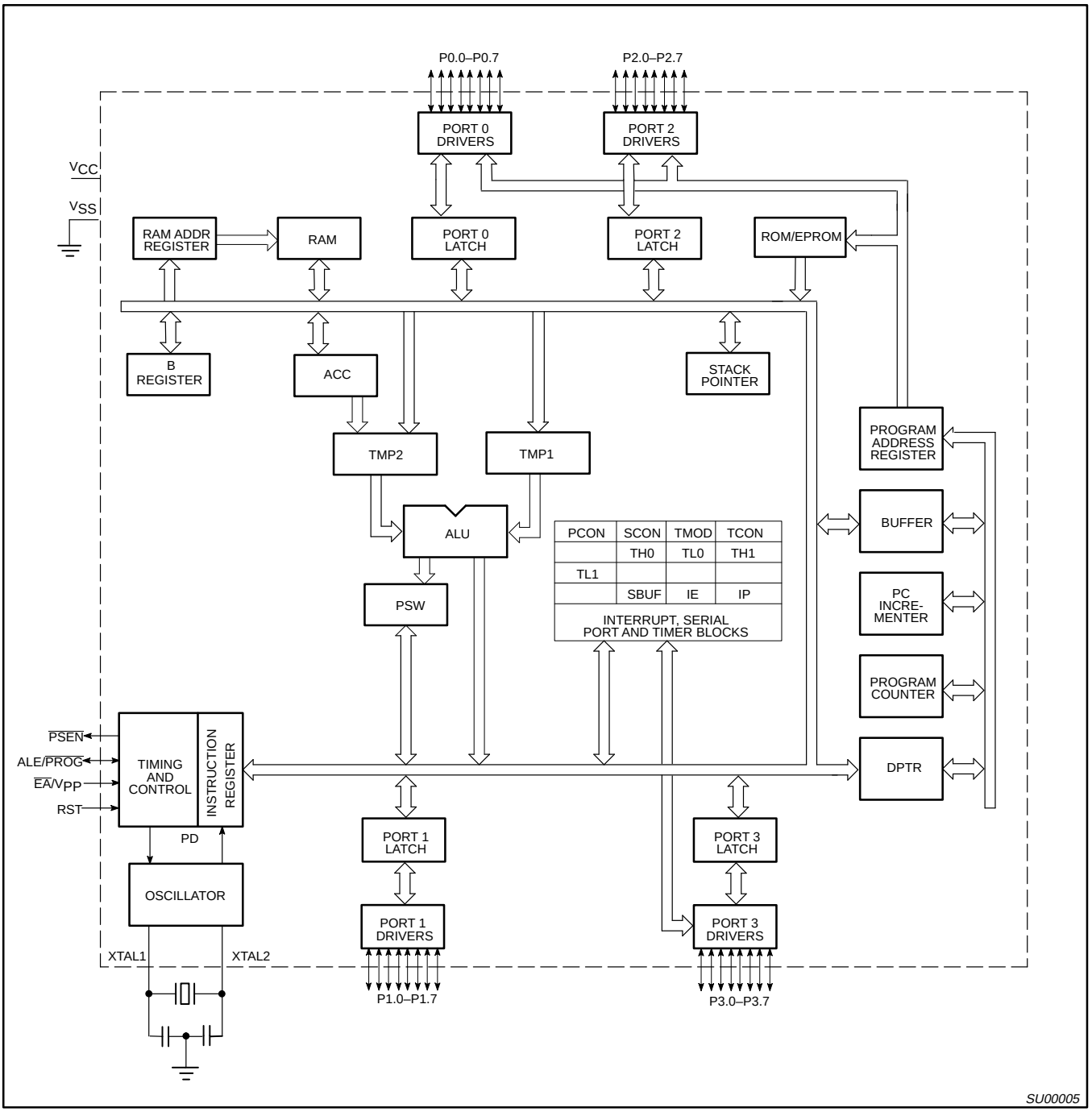
SU00003

LOGIC SYMBOL



SU00004

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO. DIP	PIN NO. LCC	PIN NO. QFP	TYPE	NAME AND FUNCTION
V_{SS}	20	22	16	I	**Ground:** 0V reference.
V_{CC}	40	44	38	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation.
P0.0–0.7	39–32	43–36	37–30	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification in the 87C51. External pull-ups are required during program verification.
P1.0–P1.7	1–8	2–9	40-44, 1–3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 1 also receives the low-order address byte during program memory verification.
P2.0–P2.7	21–28	24–31	18–25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0–P3.7	10–17	11, 13–19	5, 7–13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the 80C51 family, as listed below:
	10	11	5	I	**RxD (P3.0):** Serial input port
	11	13	7	O	**TxD (P3.1):** Serial output port
	12	14	8	I	**$\overline{INT0}$ (P3.2):** External interrupt
	13	15	9	I	**$\overline{INT1}$ (P3.3):** External interrupt
	14	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	18	12	O	**$\overline{WR}$ (P3.6):** External data memory write strobe
	17	19	13	O	**$\overline{RD}$ (P3.7):** External data memory read strobe
RST	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}.
ALE/$\overline{PROG}$	30	33	27	I/O	**Address Latch Enable/Program Pulse:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{PROG}$) during EPROM programming.
$\overline{PSEN}$	29	32	26	O	**Program Store Enable:** The read strobe to external program memory. When the device is executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.
$\overline{EA}$/V_{PP}	31	35	29	I	**External Access Enable/Programming Supply Voltage:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H to 0FFFH. If $\overline{EA}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than 0FFFH. This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming.
XTAL1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.

Table 1. 80C52/80C54/80C58 Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION MSB							LSB	RESET VALUE
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
AUXR#	Auxiliary	8EH	–	–	–	–	–	–	–	AO	xxxxxxx0B
AUXR1#	Auxiliary 1 (Note 2)	A2H	–	–	–	–	WUPD	0	–	DPS	xxxx00x0B
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
DPTR:	Data Pointer (2 bytes)										
DPH	Data Pointer High	83H									00H
DPL	Data Pointer Low	82H									00H
			AF	AE	AD	AC	AB	AA	A9	A8	
IE*	Interrupt Enable	A8H	EA	EC	ET2	ES	ET1	EX1	ET0	EX0	00H
			BF	BE	BD	BC	BB	BA	B9	B8	
IP*	Interrupt Priority	B8H	–	–	PT2	PS	PT1	PX1	PT0	PX0	x0000000B
			B7	B6	B5	B4	B3	B2	B1	B0	
IPH#	Interrupt Priority High	B7H	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	x0000000B
			87	86	85	84	83	82	81	80	
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH
			97	96	95	94	93	92	91	90	
P1*	Port 1	90H	–	–	–	–	–	–	T2EX	T2	FFH
			A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0H	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	FFH
			B7	B6	B5	B4	B3	B2	B1	B0	
P3*	Port 3	B0H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TxD	RxD	FFH
PCON#[1]	Power Control	87H	SMOD1	SMOD0	–	–	GF1	GF0	PD	IDL	00xx0000B
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	–	P	00H
SADDR#	Slave Address	A9H									00H
SADEN#	Slave Address Mask	B9H									00H
SBUF	Serial Data Buffer	99H									xxxxxxxxB
			9F	9E	9D	9C	9B	9A	99	98	
SCON*	Serial Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SP	Stack Pointer	81H									07H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
			CF	CE	CD	CC	CB	CA	C9	C8	
T2MOD#	Timer 2 Mode Control	C9H	–	–	–	–	–	–	T2OE	DCEN	xxxxxx00B
TH0	Timer High 0	8CH									00H
TH1	Timer High 1	8DH									00H
TL0	Timer Low 0	8AH									00H
TL1	Timer Low 1	8BH									00H
TMOD	Timer Mode	89H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	00H

* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.
– Reserved bits.
1. Reset value depends on reset source.
2. Available only on SC80C51.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-up reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles.

IDLE MODE

In idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. the control bits for the reduced power modes are in the special function register PCON.

Table 2 shows the state of I/O ports during low current operating modes.

Table 2. External Pin Status During Idle and Power-Down Modes

MODE	PROGRAM MEMORY	ALE	$\overline{\text{PSEN}}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

ROM CODE SUBMISSION

When submitting ROM code for the 80C51, the following must be specified:

1. 4k byte user ROM data
2. 64 byte ROM encryption key (SC80C51 only)
3. ROM security bits (SC80C51 only).

ADDRESS	CONTENT	BIT(S)	COMMENT
0000H to 0FFFH	DATA	7:0	User ROM Data
1000H to 101FH	KEY	7:0	ROM Encryption Key
1020H	SEC	0	ROM Security Bit 1
1020H	SEC	1	ROM Security Bit 2

Security Bit 1: When programmed, this bit has two effects on masked ROM parts:

1. External MOVC is disabled, and
2. EA# is latched on Reset.

Security Bit 2: When programmed, this bit inhibits Verify User ROM.

Electrical Deviations from Commercial Specifications for Extended Temperature Range (87C51)
DC and AC parameters not included here are the same as in the commercial temperature range table.

DC ELECTRICAL CHARACTERISTICS

T_{amb} = –40°C to +85°C, V_{CC} = 5V ±10%, V_{SS} = 0V (Philips North America SC87C51);
For SC87C51 (33MHz only), T_{amb} = 0°C to +70°C, V_{CC} = 5V ±5%
T_{amb} = –40°C to +85°C, V_{CC} = 5V ±10%, V_{SS} = 0V (PCB80C31/51 and PCF80C31/51 Philips Parts Only)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{IL}	Input low voltage, except $\overline{EA}$ (Philips North America)		–0.5	$0.2V_{CC}$–0.15	V
V_{IL}	Input low voltage, except $\overline{EA}$ (Philips)		–0.5	$0.2V_{CC}$–0.25	V
V_{IL1}	Input low voltage to $\overline{EA}$		–0.5	$0.2V_{CC}$–0.45	V
V_{IH}	Input high voltage, except XTAL1, RST		$0.2V_{CC}$+1	V_{CC}+0.5	V
V_{IH1}	Input high voltage to XTAL1, RST		$0.7V_{CC}$+0.1	V_{CC}+0.5	V
I_{IL}	Logical 0 input current, ports 1, 2, 3	V_{IN} = 0.45V		–75	µA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3	V_{IN} = 2.0V		–750	µA
I_{CC}	Power supply current:	V_{CC} = 4.5–5.5V			
	Active mode[1] @ 16MHz (Philips PCB80C31/51, PCF80C31/51)			25	mA
	Active mode @ 12MHz (Philips North America SC87C51)			20	mA
	Idle mode[2] @ 16MHz (Philips PCB80C31/51, PCF80C31/51)			6.5	mA
	Idle mode @ 12MHz (Philips North America SC87C51)			5	mA
	Power-down mode[3] (Philips PCB80C31/51, PCF80C31/51)			75	µA
	Power-down mode (Philips North America SC87C51)			50	µA

NOTES:
1. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 10ns; $V_{IL} = V_{SS}$ + 0.5V; $V_{IH} = V_{CC}$ – 0.5V; XTAL2 not connected; $\overline{EA}$ = RST = Port 0 = V_{CC}.
2. The idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 10ns; $V_{IL} = V_{SS}$ + 0.5V; $V_{IH} = V_{CC}$ – 0.5V; XTAL2 not connected; $\overline{EA}$ = Port 0 = V_{CC}; RST = V_{SS}.
3. The power-down current is measured with all output pins disconnected, XTAL2 not connected, $\overline{EA}$ = Port 0 = V_{CC}; RST = V_{SS}.

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70 or –40 to +85	°C
Storage temperature range	–65 to +150	°C
Voltage on $\overline{EA}/V_{PP}$ pin to V_{SS}	0 to +13.0	V
Voltage on any other pin to V_{SS}	–0.5 to +6.5	V
Maximum I_{OL} per I/O pin	15	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C or –40°C to +85°C, V_{CC} = 5V ±20%, V_{SS} = 0V (PCB80C31/51 and PCF80C31/51) (12, 16, and 24MHz versions)
T_{amb} = 0°C to +70°C or –40°C to +85°C, V_{CC} = 5V ±10%, V_{SS} = 0V (87C51 12, 16, and 24MHz versions) (PCB80C31/51 33MHz version);
For SC87C51 (33MHz only) T_{amb} = 0°C to +70°C, V_{CC} = 5V ±5%

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYPICAL[1]	MAX	
V_{IL}	Input low voltage, except $\overline{EA}$[7]		–0.5		$0.2V_{CC}$–0.1	V
V_{IL1}	Input low voltage to $\overline{EA}$[7]		0		$0.2V_{CC}$–0.3	V
V_{IH}	Input high voltage, except XTAL1, RST[7]		$0.2V_{CC}$+0.9		V_{CC}+0.5	V
V_{IH1}	Input high voltage, XTAL1, RST[7]		$0.7V_{CC}$		V_{CC}+0.5	V
V_{OL}	Output low voltage, ports 1, 2, 3[11]	I_{OL} = 1.6mA[2]			0.45	V
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$[11]	I_{OL} = 3.2mA[2]			0.45	V
V_{OH}	Output high voltage, ports 1, 2, 3, ALE, $\overline{PSEN}$[3]	I_{OH} = –60µA, I_{OH} = –25µA I_{OH} = –10µA	2.4 $0.75V_{CC}$ $0.9V_{CC}$			V V V
V_{OH1}	Output high voltage (port 0 in external bus mode)	I_{OH} = –800µA, I_{OH} = –300µA I_{OH} = –80µA	2.4 $0.75V_{CC}$ $0.9V_{CC}$			V V V
I_{IL}	Logical 0 input current, ports 1, 2, 3[7]	V_{IN} = 0.45V			–50	µA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3[7]	See note 4			–650	µA
I_{LI}	Input leakage current, port 0	V_{IN} = V_{IL} or V_{IH}			±10	µA
I_{CC}	Power supply current:[7] Active mode @ 12MHz[8] (Philips) Active mode @ 12MHz[5] (Philips North America) Idle mode @ 12MHz[9] (Philips) Idle mode @ 12MHz (Philips North America) Power-down mode[10] (Philips and Philips North America)	See note 6		 11.5 1.3 3	 18 19 4.4 4 50	 mA mA mA mA µA
R_{RST}	Internal reset pull-down resistor (Philips North America) (Philips)		 50 50		 300 150	 kΩ kΩ
C_{IO}	Pin capacitance[12]				10	pF

NOTES:

1. Typical ratings are not guaranteed. The values listed are at room temperature, 5V.
2. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
3. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
4. Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
5. I_{CCMAX} at other frequencies (for Philips North America parts) is given by: Active mode: I_{CCMAX} = 1.43 X FREQ + 1.90;
   Idle mode: I_{CCMAX} = 0.14 X FREQ +2.31, where FREQ is the external oscillator frequency in MHz. I_{CCMAX} is given in mA. See Figure 8.
6. See Figures 9 through 12 for I_{CC} test conditions.
7. For Philips North America parts when T_{amb} = –40°C to +85°C or Philips parts when T_{amb} = –40°C to +125°C, see DC Electrical Characteristics table on previous page.
8. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 10ns; $V_{IL} = V_{SS}$ + 0.5V; $V_{IH} = V_{CC}$ – 0.5V; XTAL2 not connected; $\overline{EA}$ = RST = Port 0 = V_{CC}.
9. The idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 10ns; $V_{IL} = V_{SS}$ + 0.5V; $V_{IH} = V_{CC}$ – 0.5V; XTAL2 not connected; $\overline{EA}$ = Port 0 = V_{CC}; RST = V_{SS}.
10. The power-down current is measured with all output pins disconnected, XTAL2 not connected, $\overline{EA}$ = Port 0 = V_{CC}; RST = V_{SS}.
11. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
    Maximum I_{OL} per port pin: 15mA
    Maximum I_{OL} per 8-bit port: 26mA
    Maximum I_{OL} total for all outputs: 67mA
    If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
12. Pin capacitance for the ceramic DIP package is 15pF maximum.

DC ELECTRICAL CHARACTERISTICS FOR PHILIPS NORTH AMERICA DEVICES (SC80C31 AND SC80C51)

T_{amb} = 0°C to +70°C or –40°C to +85°C, V_{CC} = 5V ±10%; V_{SS} = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
V_{IL}	Input low voltage	4.5V < V_{CC} < 5.5V	–0.5		$0.2V_{CC}$–0.1	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, $\overline{EA}$)		$0.2V_{CC}$+0.9		V_{CC}+0.5	V
V_{IH1}	Input high voltage, XTAL1, RST		$0.7V_{CC}$		V_{CC}+0.5	V
V_{OL}	Output low voltage, ports 1, 2, 3[8]	V_{CC} = 4.5V I_{OL} = 1.6mA[2]			0.4	V
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$[8, 7]	V_{CC} = 4.5V I_{OL} = 3.2mA[2]			0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 [3]	V_{CC} = 4.5V I_{OH} = –30µA	V_{CC} – 0.7			V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE[9], $\overline{PSEN}$[3]	V_{CC} = 4.5V I_{OH} = –3.2mA	V_{CC} – 0.7			V
I_{IL}	Logical 0 input current, ports 1, 2, 3	V_{IN} = 0.4V	–1		–50	µA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3[6]	V_{IN} = 2.0V See note 4			–650	µA
I_{LI}	Input leakage current, port 0	0.45 < V_{IN} < V_{CC} – 0.3			±10	µA
I_{CC}	Power supply current (see Figure 8): Active mode @ 16MHz[5] Idle mode @ 16MHz[5] Power-down mode	See note 5 T_{amb} = 0 to +70°C T_{amb} = –40 to +85°C		 11.5 1.3 3	 32 5 50 75	 µA µA µA µA
R_{RST}	Internal reset pull-down resistor		40		225	kΩ
C_{IO}	Pin capacitance[10] (except $\overline{EA}$)				15	pF

NOTES:

1. Typical ratings are not guaranteed. The values listed are at room temperature, 5V.
2. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
3. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the (V_{CC}–0.7) specification when the address bits are stabilizing.
4. Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
5. See Figures 9 through 12 for I_{CC} test conditions.
   Active Mode: $I_{CC} = 1.5 \times FREQ + 8.0$;
   Idle Mode: $I_{CC} = 0.14 \times FREQ + 2.31$; See Figure 8.
6. This value applies to T_{amb} = 0°C to +70°C. For T_{amb} = –40°C to +85°C, I_{TL} = –750µA.
7. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
8. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 15mA (*NOTE: This is 85°C specification.)
   Maximum I_{OL} per 8-bit port: 26mA
   Maximum total I_{OL} for all outputs: 71mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
9. ALE is tested to V_{OH1}, except when ALE is off then V_{OH} is the voltage specification.
10. Pin capacitance is characterized but not tested. Pin capacitance is less than 25pF. Pin capacitance of ceramic package is less than 15pF (except $\overline{EA}$ it is 25pF).

AC ELECTRICAL CHARACTERISTICS FOR SC87C51 12–33MHz PHILIPS NORTH AMERICA DEVICES

T_{amb} = 0°C to +70°C or –40°C to +85°C, V_{CC} = 5V ±10%, V_{SS} = 0V (SC87C51 12, 16 and 24MHz versions);
For SC87C51 (33MHz only) T_{amb} = = 0°C to +70°C, V_{CC} = 5V ±5%

SYMBOL	FIGURE	PARAMETER	VARIABLE CLOCK[3] MIN	VARIABLE CLOCK[3] MAX	UNIT
$1/t_{CLCL}$		Oscillator frequency: **Speed Versions** SC87C51 C G P Y	 3.5 3.5 3.5 3.5	 12 16 24 33	 MHz MHz MHz MHz
t_{LHLL}	1	ALE pulse width	$2t_{CLCL}$–40		ns
t_{AVLL}	1	Address valid to ALE low	t_{CLCL}–13		ns
t_{LLAX}	1	Address hold after ALE low	t_{CLCL}–20		ns
t_{LLIV}	1	ALE low to valid instruction in		$4t_{CLCL}$–65	ns
t_{LLPL}	1	ALE low to $\overline{PSEN}$ low	t_{CLCL}–13		ns
t_{PLPH}	1	$\overline{PSEN}$ pulse width	$3t_{CLCL}$–20		ns
t_{PLIV}	1	$\overline{PSEN}$ low to valid instruction in		$3t_{CLCL}$–45	ns
t_{PXIX}	1	Input instruction hold after $\overline{PSEN}$	0		ns
t_{PXIZ}	1	Input instruction float after $\overline{PSEN}$		t_{CLCL}–10	ns
t_{AVIV}	1	Address to valid instruction in		$5t_{CLCL}$–55	ns
t_{PLAZ}	1	$\overline{PSEN}$ low to address float		10	ns
Data Memory					
t_{RLRH}	2, 3	$\overline{RD}$ pulse width	$6t_{CLCL}$–100		ns
t_{WLWH}	2, 3	$\overline{WR}$ pulse width	$6t_{CLCL}$–100		ns
t_{RLDV}	2, 3	$\overline{RD}$ low to valid data in		$5t_{CLCL}$–90	ns
t_{RHDX}	2, 3	Data hold after $\overline{RD}$	0		ns
t_{RHDZ}	2, 3	Data float after $\overline{RD}$		$2t_{CLCL}$–28	ns
t_{LLDV}	2, 3	ALE low to valid data in		$8t_{CLCL}$–150	ns
t_{AVDV}	2, 3	Address to valid data in		$9t_{CLCL}$–165	ns
t_{LLWL}	2, 3	ALE low to $\overline{RD}$ or $\overline{WR}$ low	$3t_{CLCL}$–50	$3t_{CLCL}$+50	ns
t_{AVWL}	2, 3	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	$4t_{CLCL}$–75		ns
t_{QVWX}	2, 3	Data valid to $\overline{WR}$ transition	t_{CLCL}–20		ns
t_{WHQX}	2, 3	Data hold after $\overline{WR}$	t_{CLCL}–20		ns
t_{RLAZ}	2, 3	$\overline{RD}$ low to address float		0	ns
t_{WHLH}	2, 3	$\overline{RD}$ or $\overline{WR}$ high to ALE high	t_{CLCL}–20	t_{CLCL}+25	ns
External Clock					
t_{CHCX}	5	High time	12		ns
t_{CLCX}	5	Low time	12		ns
t_{CLCH}	5	Rise time		20	ns
t_{CHCL}	5	Fall time		20	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
3. For all Philips North America speed versions only.
4. Interfacing the 87C51 to devices with float times up to 50ns is permitted. This limited bus contention will not cause damage to port 0 drivers.

AC ELECTRICAL CHARACTERISTICS FOR PHILIPS DEVICES

T_{amb} = 0°C to +70°C, V_{CC} = 5V ±20%, V_{SS} = 0V (PCB80C31/51, PCF80C31/51)[1, 2, 4, 5]

SYMBOL	FIGURE	PARAMETER	VARIABLE CLOCK[3] MIN	VARIABLE CLOCK[3] MAX	UNIT
$1/t_{CLCL}$		Oscillator frequency: **Speed Versions** PCB8031/51 –2 PCA/PCB/PCF80C31/51 –3 PCB/PCF80C31/51 –4 PCB/FB80C31/51 –5	 0.5 1.2 1.2 1.2	 12 16 24 33	 MHz MHz MHz MHz
t_{LHLL}	1	ALE pulse width	$2t_{CLCL}$–40		ns
t_{AVLL}	1	Address valid to ALE low	t_{CLCL}–25		ns
t_{LLAX}	1	Address hold after ALE low	t_{CLCL}–25		ns
t_{LLIV}	1	ALE low to valid instruction in		$4t_{CLCL}$–65	ns
t_{LLPL}	1	ALE low to $\overline{PSEN}$ low	t_{CLCL}–25		ns
t_{PLPH}	1	$\overline{PSEN}$ pulse width	$3t_{CLCL}$–45		ns
t_{PLIV}	1	$\overline{PSEN}$ low to valid instruction in		$3t_{CLCL}$–60	ns
t_{PXIX}	1	Input instruction hold after $\overline{PSEN}$	0		ns
t_{PXIZ}	1	Input instruction float after $\overline{PSEN}$		t_{CLCL}–25	ns
t_{AVIV}	1	Address to valid instruction in		$5t_{CLCL}$–80	ns
t_{PLAZ}	1	$\overline{PSEN}$ low to address float		10	ns
Data Memory					
t_{RLRH}	2, 3	$\overline{RD}$ pulse width	$6t_{CLCL}$–100		ns
t_{WLWH}	2, 3	$\overline{WR}$ pulse width	$6t_{CLCL}$–100		ns
t_{RLDV}	2, 3	$\overline{RD}$ low to valid data in		$5t_{CLCL}$–90	ns
t_{RHDX}	2, 3	Data hold after $\overline{RD}$	0		ns
t_{RHDZ}	2, 3	Data float after $\overline{RD}$		$2t_{CLCL}$–28	ns
t_{LLDV}	2, 3	ALE low to valid data in		$8t_{CLCL}$–150	ns
t_{AVDV}	2, 3	Address to valid data in		$9t_{CLCL}$–165	ns
t_{LLWL}	2, 3	ALE low to $\overline{RD}$ or $\overline{WR}$ low	$3t_{CLCL}$–50	$3t_{CLCL}$+50	ns
t_{AVWL}	2, 3	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	$4t_{CLCL}$–75		ns
t_{QVWX}	2, 3	Data valid to $\overline{WR}$ transition	t_{CLCL}–30		ns
t_{WHQX}	2, 3	Data hold after $\overline{WR}$	t_{CLCL}–25		ns
t_{RLAZ}	2, 3	$\overline{RD}$ low to address float		0	ns
t_{WHLH}	2, 3	$\overline{RD}$ or $\overline{WR}$ high to ALE high	t_{CLCL}–25	t_{CLCL}+25	ns
External Clock					
t_{CHCX}	5	High time	15		ns
t_{CLCX}	5	Low time	15		ns
t_{CLCH}	5	Rise time		20	ns
t_{CHCL}	5	Fall time		20	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
3. For all Philips speed versions only.
4. Interfacing the 80C31/51 to devices with float times up to 30ns is permitted. This limited bus contention will not cause damage to port 0 drivers.
5. V_{CC} = 5V ±10% for 33MHz.

AC ELECTRICAL CHARACTERISTICS FOR PHILIPS NORTH AMERICA DEVICES (SC80C31 AND SC80C51)

T_{amb} = 0°C to +70°C or –40°C to +85°C, V_{CC} = 5V ±10%, V_{SS} = 0V[1, 2, 3]

SYMBOL	FIGURE	PARAMETER	16MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	1	Oscillator frequency Speed versions : C, G			3.5	16	MHz
t_{LHLL}	1	ALE pulse width	85		$2t_{CLCL}$–40		ns
t_{AVLL}	1	Address valid to ALE low	22		t_{CLCL}–40		ns
t_{LLAX}	1	Address hold after ALE low	32		t_{CLCL}–30		ns
t_{LLIV}	1	ALE low to valid instruction in		150		$4t_{CLCL}$–100	ns
t_{LLPL}	1	ALE low to $\overline{PSEN}$ low	32		t_{CLCL}–30		ns
t_{PLPH}	1	$\overline{PSEN}$ pulse width	142		$3t_{CLCL}$–45		ns
t_{PLIV}	1	$\overline{PSEN}$ low to valid instruction in[4]		82		$3t_{CLCL}$–105	ns
t_{PXIX}	1	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	1	Input instruction float after $\overline{PSEN}$		37		t_{CLCL}–25	ns
t_{AVIV}	1	Address to valid instruction in[4]		207		$5t_{CLCL}$–105	ns
t_{PLAZ}	1	$\overline{PSEN}$ low to address float		10		10	ns
Data Memory							
t_{RLRH}	2, 3	$\overline{RD}$ pulse width	275		$6t_{CLCL}$–100		ns
t_{WLWH}	2, 3	$\overline{WR}$ pulse width	275		$6t_{CLCL}$–100		ns
t_{RLDV}	2, 3	$\overline{RD}$ low to valid data in		147		$5t_{CLCL}$–165	ns
t_{RHDX}	2, 3	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	2, 3	Data float after $\overline{RD}$		65		$2t_{CLCL}$–60	ns
t_{LLDV}	2, 3	ALE low to valid data in		350		$8t_{CLCL}$–150	ns
t_{AVDV}	2, 3	Address to valid data in		397		$9t_{CLCL}$–165	ns
t_{LLWL}	2, 3	ALE low to $\overline{RD}$ or $\overline{WR}$ low	137	239	$3t_{CLCL}$–50	$3t_{CLCL}$+50	ns
t_{AVWL}	2, 3	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	122		$4t_{CLCL}$–130		ns
t_{QVWX}	2, 3	Data valid to $\overline{WR}$ transition	13		t_{CLCL}–50		ns
t_{WHQX}	2, 3	Data hold after $\overline{WR}$	13		t_{CLCL}–50		ns
t_{QVWH}	3	Data valid to $\overline{WR}$ high	287		$7t_{CLCL}$–150		ns
t_{RLAZ}	2, 3	$\overline{RD}$ low to address float		0		0	ns
t_{WHLH}	2, 3	$\overline{RD}$ or $\overline{WR}$ high to ALE high	23	103	t_{CLCL}–40	t_{CLCL}+40	ns
External Clock							
t_{CHCX}	5	High time	20		20	t_{CLCL}–t_{CLCX}	ns
t_{CLCX}	5	Low time	20		20	t_{CLCL}–t_{CHCX}	ns
t_{CLCH}	5	Rise time		20		20	ns
t_{CHCL}	5	Fall time		20		20	ns
Shift Register							
t_{XLXL}	4	Serial port clock cycle time	750		$12t_{CLCL}$		ns
t_{QVXH}	4	Output data setup to clock rising edge	492		$10t_{CLCL}$–133		ns
t_{XHQX}	4	Output data hold after clock rising edge	8		$2t_{CLCL}$–117		ns
t_{XHDX}	4	Input data hold after clock rising edge	0		0		ns
t_{XHDV}	4	Clock rising edge to input data valid		492		$10t_{CLCL}$–133	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
3. Interfacing the 80C31/51 to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.
4. See application note AN457 for external memory interfacing.

AC ELECTRICAL CHARACTERISTICS FOR PHILIPS NORTH AMERICA DEVICES (SC80C31 AND SC80C51)

T_{amb} = 0°C to +70°C or –40°C to +85°C, V_{CC} = 5V ±10%, V_{SS} = 0V[1, 2, 3]

SYMBOL	FIGURE	PARAMETER	24MHz CLOCK		VARIABLE CLOCK[4]		33MHz CLOCK		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	1	Oscillator frequency Speed versions : P (24MHz) : Y (33MHz)	3.5	24	3.5	33	 3.5	 33	MHz
t_{LHLL}	1	ALE pulse width	43		$2t_{CLCL}$–40		21		ns
t_{AVLL}	1	Address valid to ALE low	17		t_{CLCL}–25		5		ns
t_{LLAX}	1	Address hold after ALE low	17		t_{CLCL}–25				ns
t_{LLIV}	1	ALE low to valid instruction in		102		$4t_{CLCL}$–65		55	ns
t_{LLPL}	1	ALE low to $\overline{PSEN}$ low	17		t_{CLCL}–25		5		ns
t_{PLPH}	1	$\overline{PSEN}$ pulse width	80		$3t_{CLCL}$–45		45		ns
t_{PLIV}	1	$\overline{PSEN}$ low to valid instruction in		65		$3t_{CLCL}$–60		30	ns
t_{PXIX}	1	Input instruction hold after $\overline{PSEN}$	0		0		0		ns
t_{PXIZ}	1	Input instruction float after $\overline{PSEN}$		17		t_{CLCL}–25		5	ns
t_{AVIV}	1	Address to valid instruction in		128		$5t_{CLCL}$–80		70	ns
t_{PLAZ}	1	$\overline{PSEN}$ low to address float		10		10		10	ns
Data Memory									
t_{RLRH}	2, 3	$\overline{RD}$ pulse width	150		$6t_{CLCL}$–100		82		ns
t_{WLWH}	2, 3	$\overline{WR}$ pulse width	150		$6t_{CLCL}$–100		82		ns
t_{RLDV}	2, 3	$\overline{RD}$ low to valid data in		118		$5t_{CLCL}$–90		60	ns
t_{RHDX}	2, 3	Data hold after $\overline{RD}$	0		0		0		ns
t_{RHDZ}	2, 3	Data float after $\overline{RD}$		55		$2t_{CLCL}$–28		32	ns
t_{LLDV}	2, 3	ALE low to valid data in		183		$8t_{CLCL}$–150		90	ns
t_{AVDV}	2, 3	Address to valid data in		210		$9t_{CLCL}$–165		105	ns
t_{LLWL}	2, 3	ALE low to $\overline{RD}$ or $\overline{WR}$ low	75	175	$3t_{CLCL}$–50	$3t_{CLCL}$+50	40	140	ns
t_{AVWL}	2, 3	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	92		$4t_{CLCL}$–75		45		ns
t_{QVWX}	2, 3	Data valid to $\overline{WR}$ transition	12		t_{CLCL}–30		0		ns
t_{WHQX}	2, 3	Data hold after $\overline{WR}$	17		t_{CLCL}–25		5		ns
t_{QVWH}	3	Data valid to $\overline{WR}$ high	162		$7t_{CLCL}$–130		80		ns
t_{RLAZ}	2, 3	$\overline{RD}$ low to address float		0		0		0	ns
t_{WHLH}	2, 3	$\overline{RD}$ or $\overline{WR}$ high to ALE high	17	67	t_{CLCL}–25	t_{CLCL}+25	5	55	ns
External Clock									
t_{CHCX}	5	High time	17		17	t_{CLCL}–t_{CLCX}			ns
t_{CLCX}	5	Low time	17		17	t_{CLCL}–t_{CHCX}			ns
t_{CLCH}	5	Rise time		5		5			ns
t_{CHCL}	5	Fall time		5		5			ns
Shift Register									
t_{XLXL}	4	Serial port clock cycle time	505		$12t_{CLCL}$		360		ns
t_{QVXH}	4	Output data setup to clock rising edge	283		$10t_{CLCL}$–133		167		ns
t_{XHQX}	4	Output data hold after clock rising edge	3		$2t_{CLCL}$–80				ns
t_{XHDX}	4	Input data hold after clock rising edge	0		0		0		ns
t_{XHDV}	4	Clock rising edge to input data valid		283		$10t_{CLCL}$–133		167	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
3. Interfacing the SC80C31/51 to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.
4. Variable clock is specified for oscillator frequencies greater than 16MHz to 33MHz. For frequencies equal or less than 16MHz, see 16MHz "AC Electrial Characteristics", page 3-16.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address
C – Clock
D – Input data
H – Logic level high
I – Instruction (program memory contents)
L – Logic level low, or ALE
P – $\overline{\text{PSEN}}$
Q – Output data
R – $\overline{\text{RD}}$ signal
t – Time
V – Valid
W – $\overline{\text{WR}}$ signal
X – No longer a valid logic level
Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.
t_{LLPL} = Time for ALE low to $\overline{\text{PSEN}}$ low.

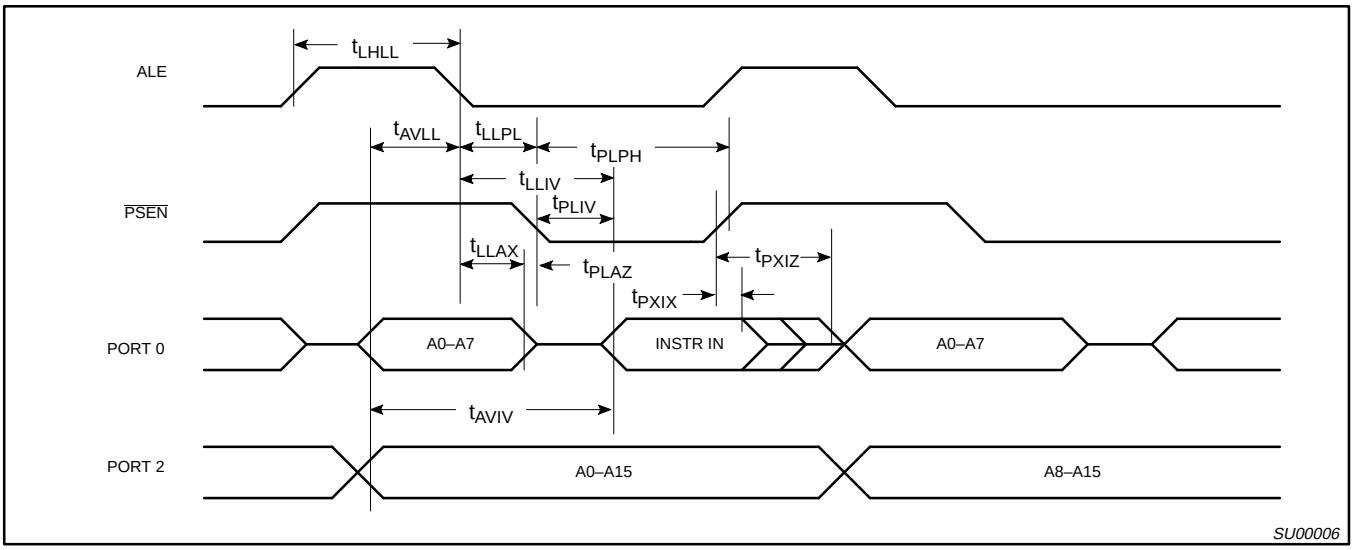


Figure 1. External Program Memory Read Cycle

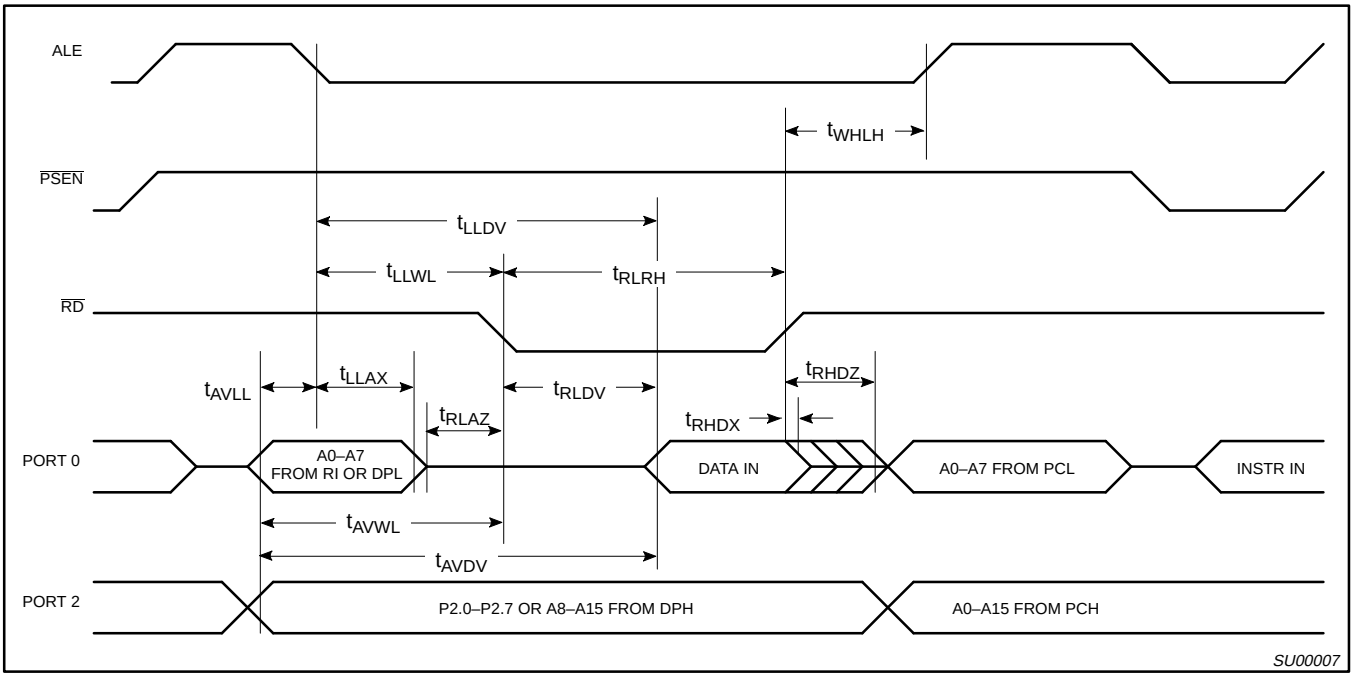


Figure 2. External Data Memory Read Cycle

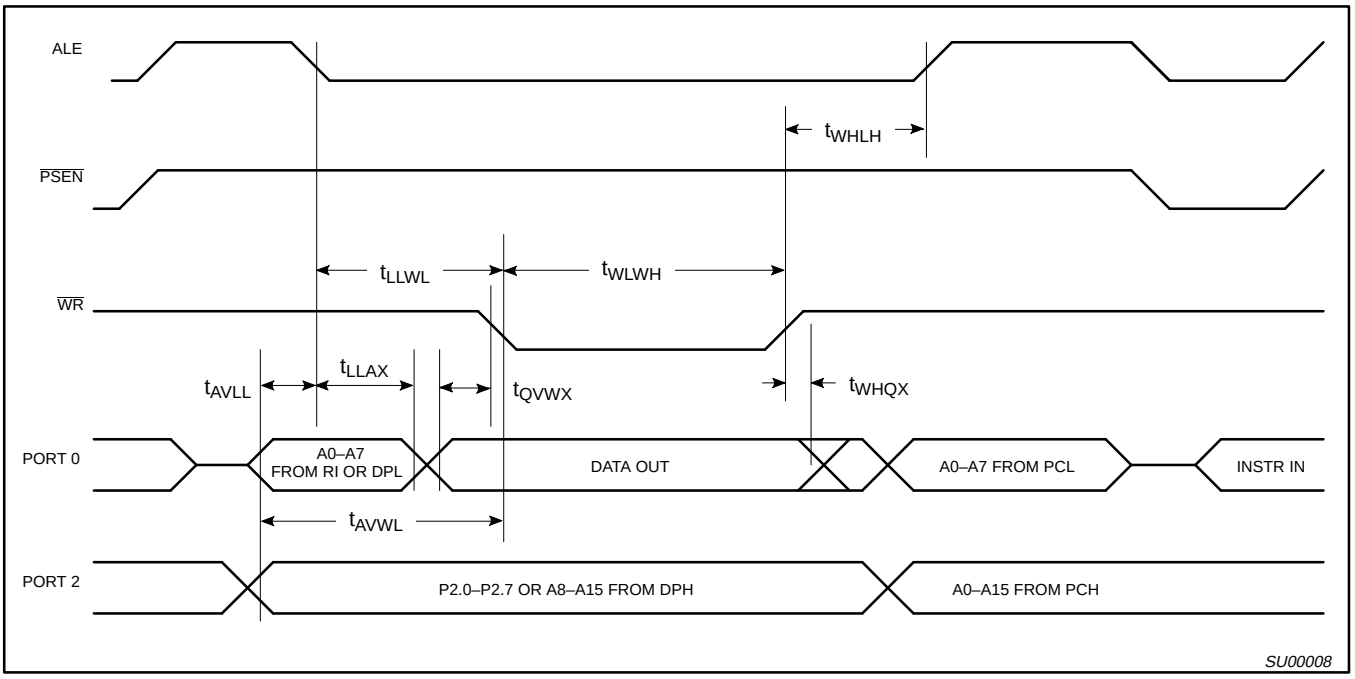


Figure 3. External Data Memory Write Cycle

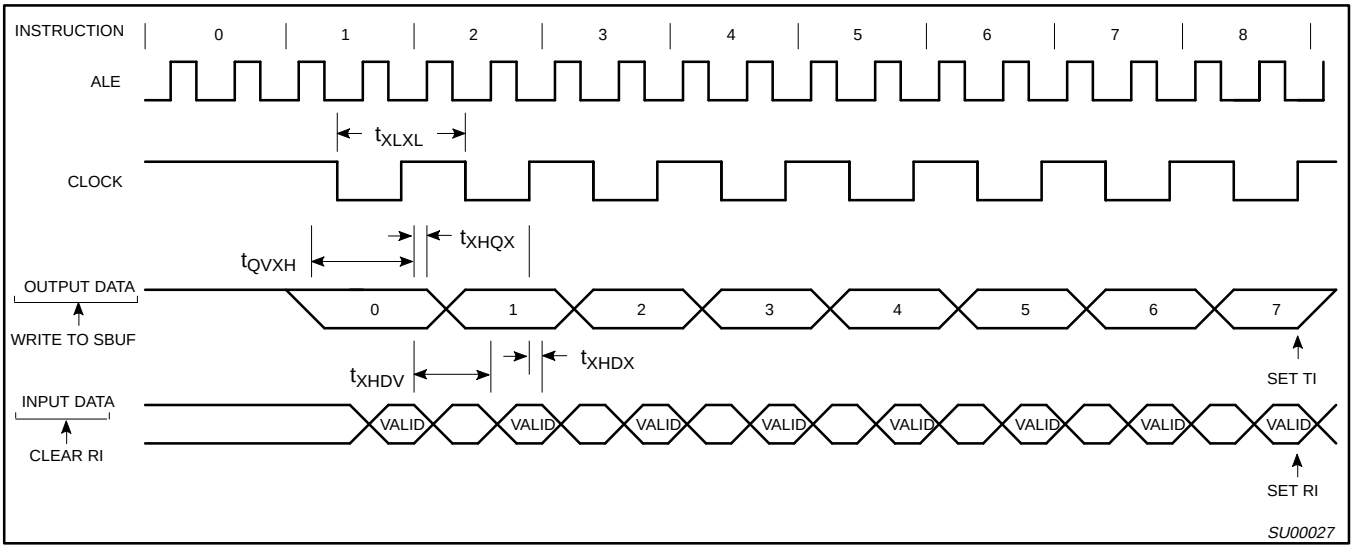


Figure 4. Shift Register Mode Timing

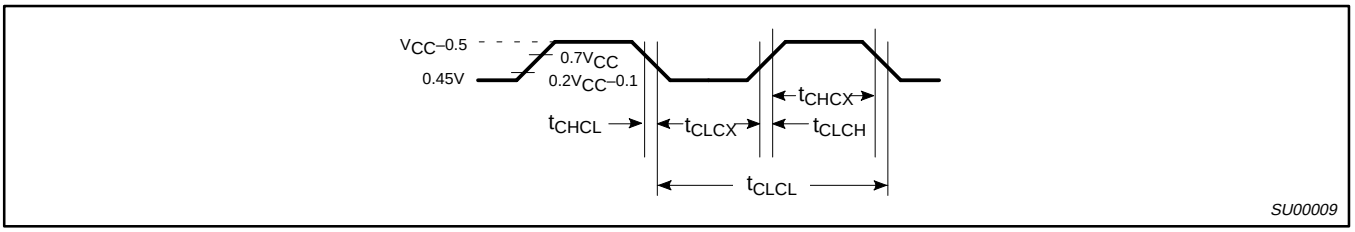
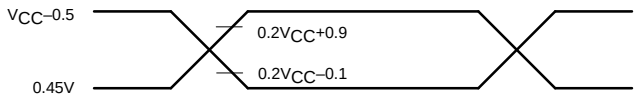


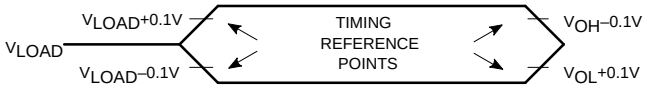
Figure 5. External Clock Drive



NOTE:
AC inputs during testing are driven at V_{CC} –0.5 for a logic '1' and 0.45V for a logic '0'.
Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} max for a logic '0'.

SU00010

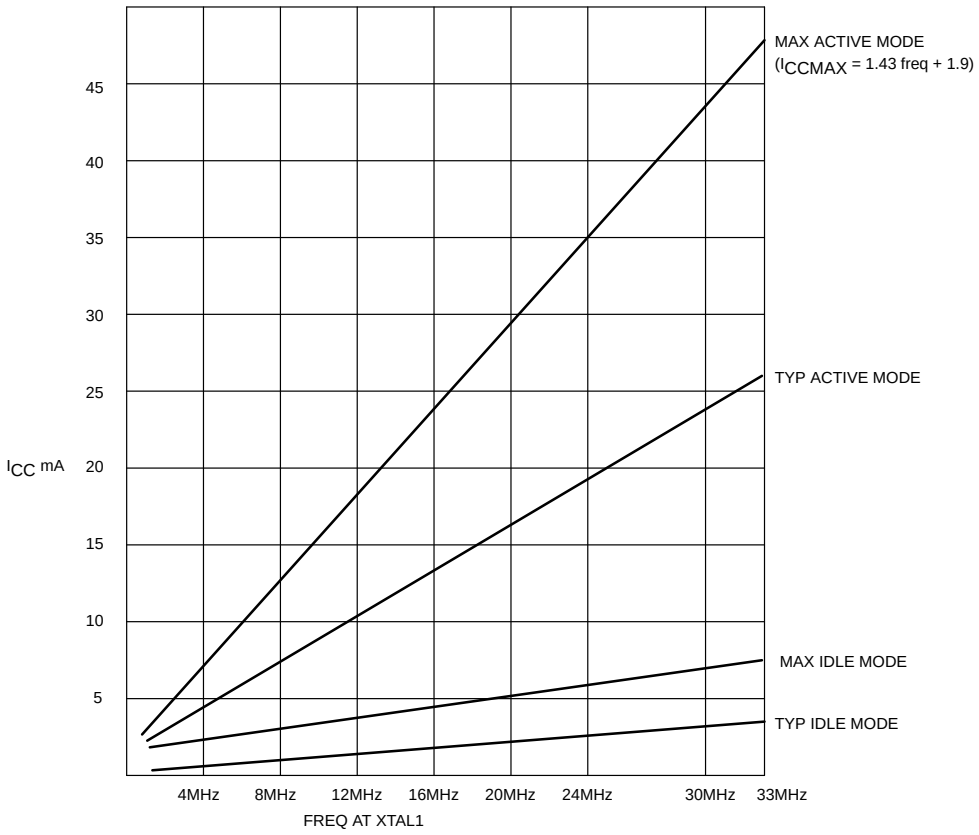
Figure 6. AC Testing Input/Output



NOTE:
For timing purposes, a port is no longer floating when a 100mV change from load voltage occurs, and begins to float when a 100mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OH}/I_{OL} \geq \pm 20$mA.

SU00011

Figure 7. Float Waveform



SU00012

Figure 8. I_{CC} vs. FREQ
Valid only within frequency specifications of the device under test

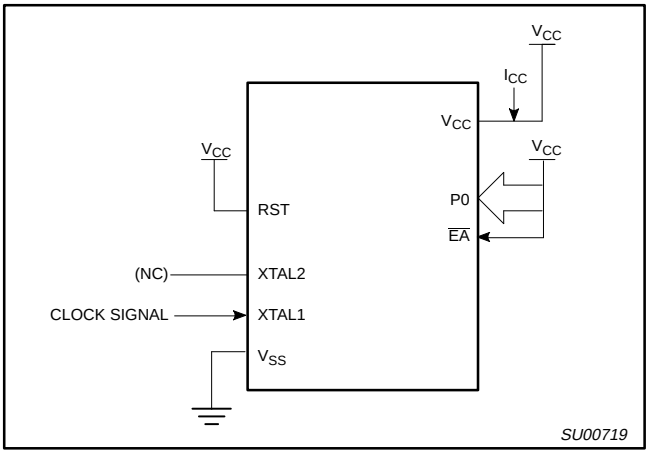


Figure 9. I_{CC} Test Condition, Active Mode
All other pins are disconnected

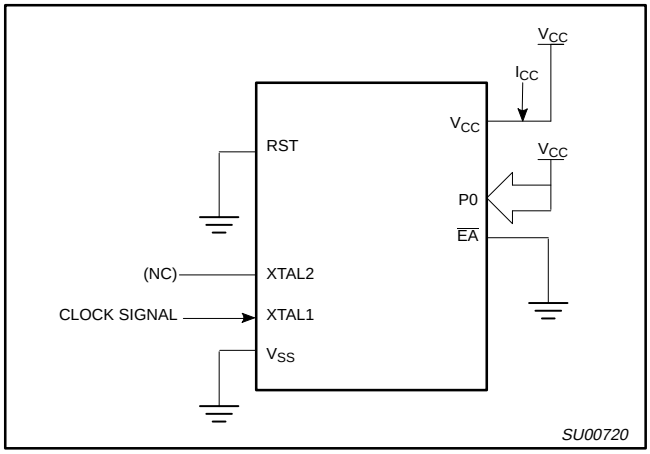


Figure 10. I_{CC} Test Condition, Idle Mode
All other pins are disconnected

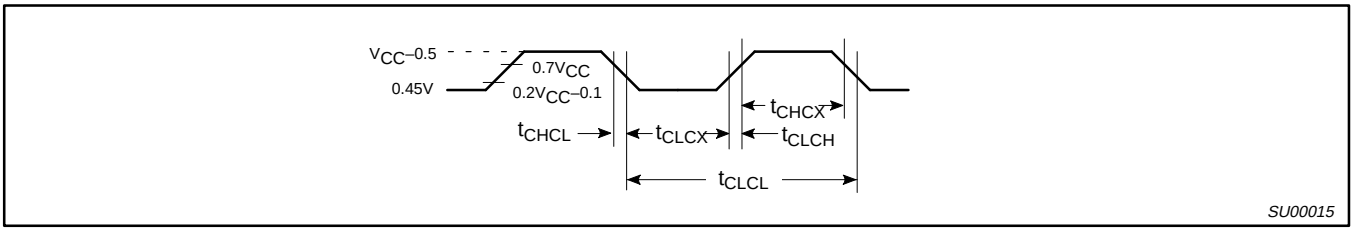


Figure 11. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes
$t_{CLCH} = t_{CHCL} = 5ns$

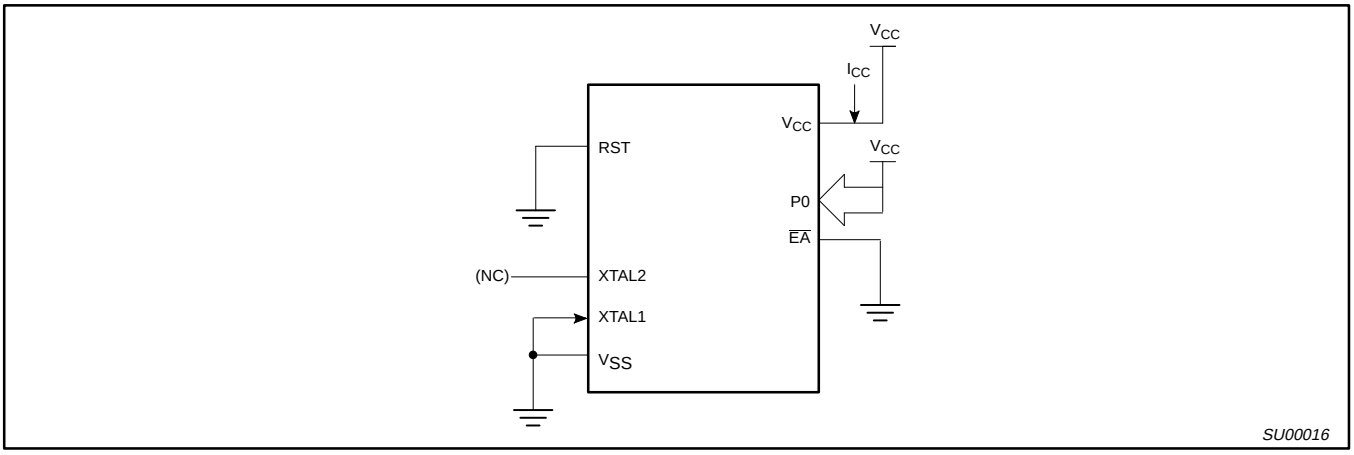


Figure 12. I_{CC} Test Condition, Power Down Mode
All other pins are disconnected. V_{CC} = 2V to 5.5V

EPROM CHARACTERISTICS

The 87C51 is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/$\overline{PROG}$ pulses.

The 87C51 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C51 manufactured by Philips Corporation.

Table 3 shows the logic levels for reading the signature bytes, and for programming the program memory, the encryption table, and the security bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 13 and 14. Figure 15 shows the circuit configuration for normal program memory verification.

Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 13. Note that the 87C51 is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 13. The code byte to be programmed into that location is applied to port 0. RST, $\overline{PSEN}$ and pins of ports 2 and 3 specified in Table 3 are held at the 'Program Code Data' levels indicated in Table 3. The ALE/$\overline{PROG}$ is pulsed low 25 times as shown in Figure 14.

To program the encryption table, repeat the 25 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the security bits, repeat the 25 pulse programming sequence using the 'Pgm Security Bit' levels. After one security bit is programmed, further programming of the code memory and encryption table is disabled. However, the other security bit can still be programmed.

Note that the $\overline{EA}/V_{PP}$ pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

Program Verification

If security bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 15. The other pins are held at the 'Verify Code Data' levels indicated in Table 3. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:
(030H) = 15H indicates manufactured by Philips
(031H) = 92H indicates 87C51

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 3, and which satisfies the timing specifications, is suitable.

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Fluorglas part number 2345–5, or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000µW/cm^2 rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

Table 3. EPROM Programming Modes

MODE	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.7	P2.6	P3.7	P3.6
Read signature	1	0	1	1	0	0	0	0
Program code data	1	0	0*	V_{PP}	1	0	1	1
Verify code data	1	0	1	1	0	0	1	1
Pgm encryption table	1	0	0*	V_{PP}	1	0	1	0
Pgm security bit 1	1	0	0*	V_{PP}	1	1	1	1
Pgm security bit 2	1	0	0*	V_{PP}	1	1	0	0

NOTES:
1. '0' = Valid low for that pin, '1' = valid high for that pin.
2. V_{PP} = 12.75V ±0.25V.
3. V_{CC} = 5V±10% during programming and verification.
4. *ALE/$\overline{PROG}$ receives 25 programming pulses while V_{PP} is held at 12.75V. Each programming pulse is low for 100µs (±10µs) and high for a minimum of 10µs.

™Trademark phrase of Intel Corporation.

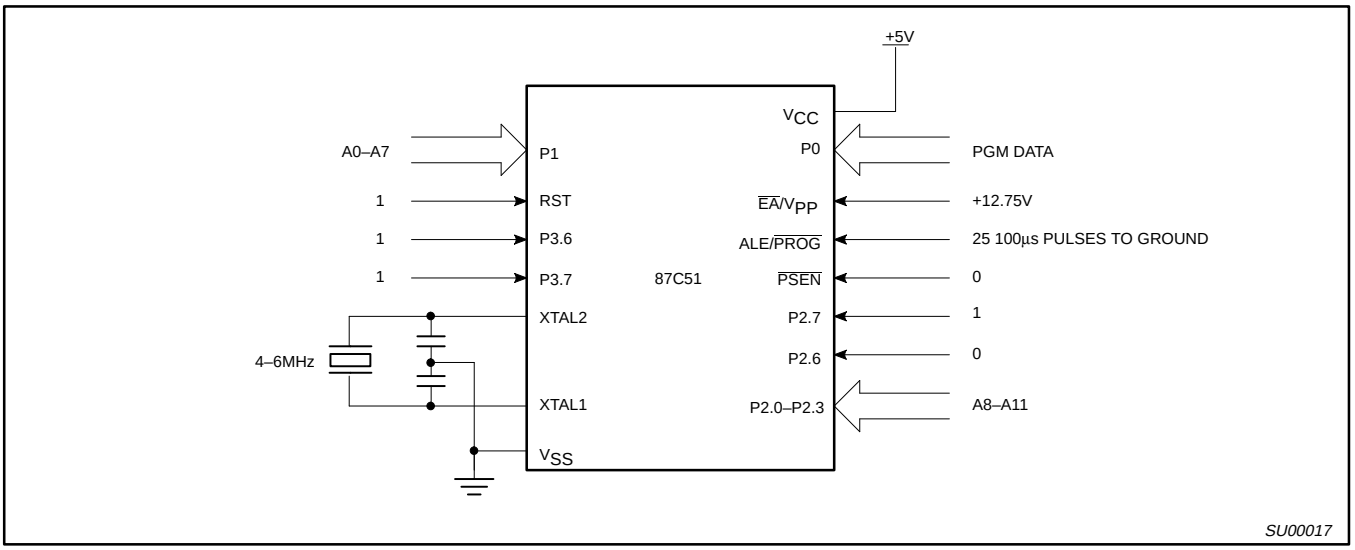


Figure 13. Programming Configuration

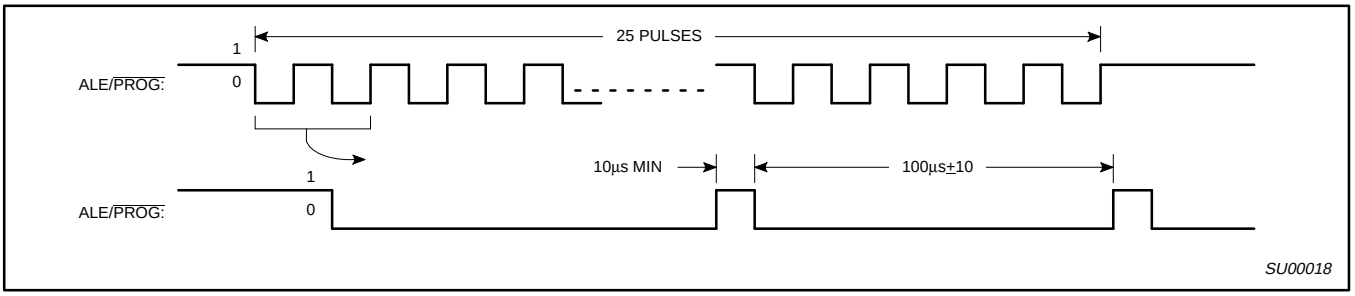


Figure 14. $\overline{\text{PROG}}$ Waveform

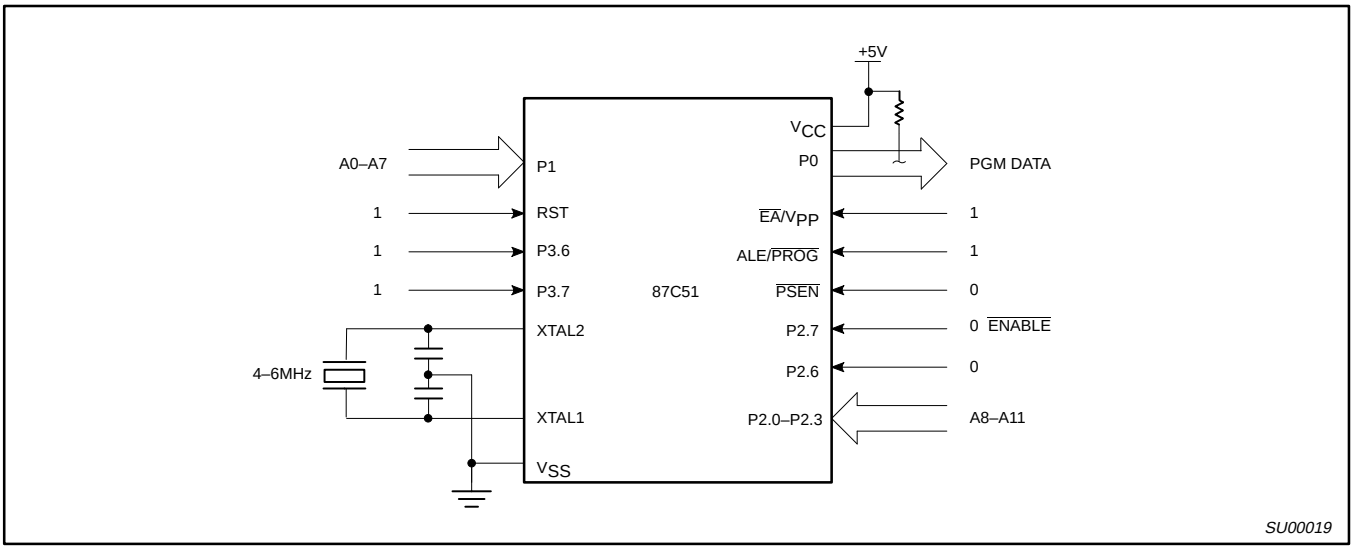
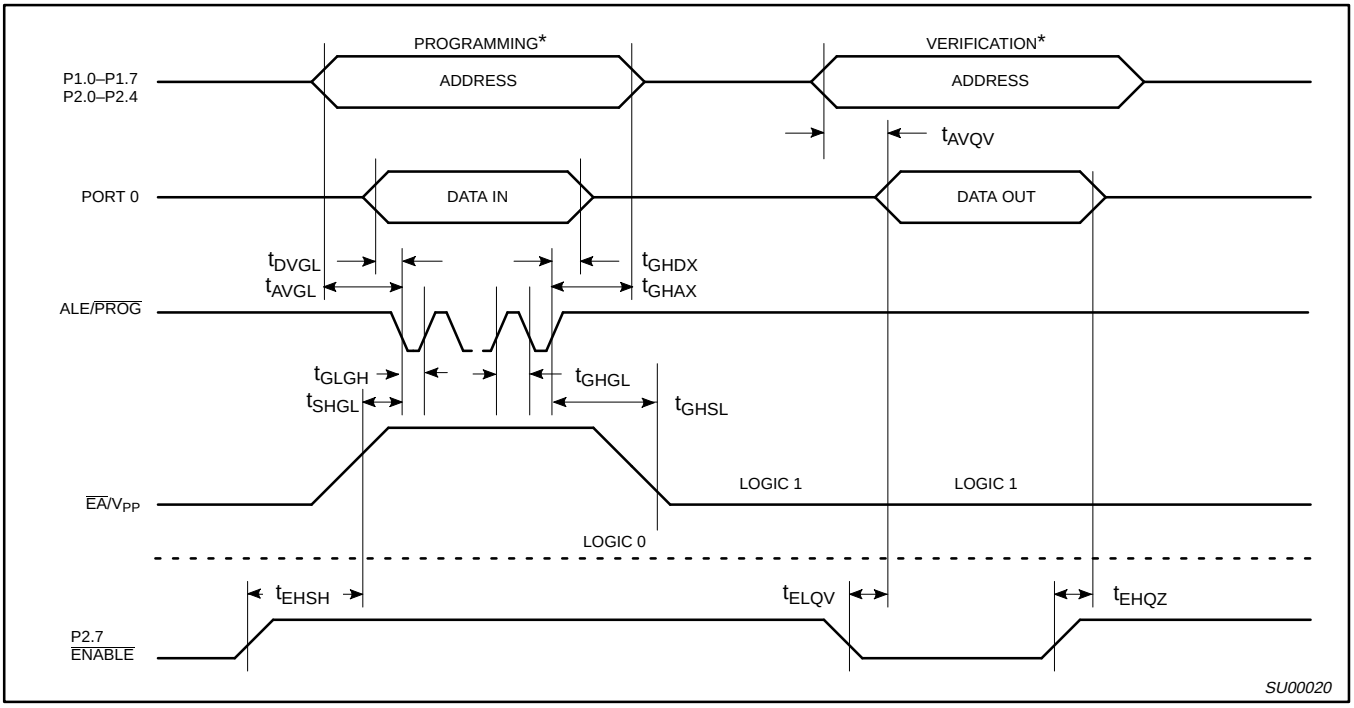


Figure 15. Program Verification

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

T_{amb} = 21°C to +27°C, V_{CC} = 5V±10%, V_{SS} = 0V (See Figure 16)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{PP}	Programming supply voltage	12.5	13.0	V
I_{PP}	Programming supply current		50	mA
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz
t_{AVGL}	Address setup to $\overline{PROG}$ low	$48t_{CLCL}$		
t_{GHAX}	Address hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data setup to $\overline{PROG}$ low	$48t_{CLCL}$		
t_{GHDX}	Data hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) high to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} setup to $\overline{PROG}$ low	10		µs
t_{GHSL}	V_{PP} hold after $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ width	90	110	µs
t_{AVQV}	Address to data valid		$48t_{CLCL}$	
t_{ELQZ}	$\overline{ENABLE}$ low to data valid		$48t_{CLCL}$	
t_{EHQZ}	Data float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHGL}	$\overline{PROG}$ high to $\overline{PROG}$ low	10		µs



NOTE:

* FOR PROGRAMMING VERIFICATION SEE FIGURE 13.
FOR VERIFICATION CONDITIONS SEE FIGURE 15.

Figure 16. EPROM Programming and Verification