TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS057

CD4073B, CD4081B, CD4082B Types

## CMOS AND Gates

High-Voltage Types (20-Volt Rating)

CD4073B Triple 3-Input AND Gate
CD4081B Quad 2-Input AND Gate
CD4082B Dual 4-Input AND Gate

■ CD4073B, CD4081B and CD-4082B AND gates provide the system designer with direct implementation of the AND function and supplement the existing family of CMOS gates.

The CD4073B, CD4081B and CD4082B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Features:

■ Medium-Speed Operation — t_{PLH}, t_{PHL} = 60 ns (typ.) at V_{DD} = 10 V
■ 100% tested for quiescent current at 20 V
■ Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
■ Noise margin (full package-temperature range) =

  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V

■ Standardized, symmetrical output characteristics
■ 5-V, 10-V, and 15-V parametric ratings
■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

CD4081B
FUNCTIONAL DIAGRAM

CD4082B
FUNCTIONAL DIAGRAM

CD4073B
FUNCTIONAL DIAGRAM
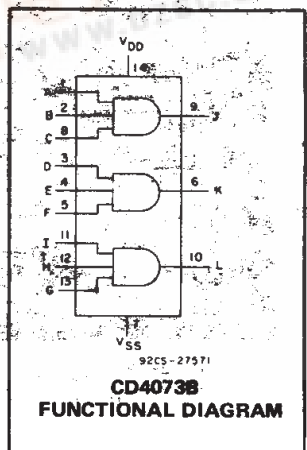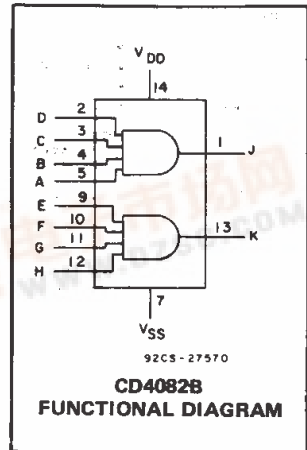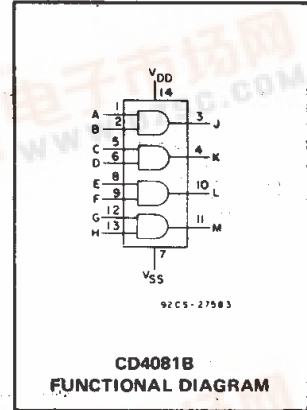
MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  Voltages referenced to V_{SS} Terminal .... −0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT .... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
  For T_A = −55°C to +100°C 500mW
  For T_A = +100°C to +125°C .... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) .... −55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... −65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
 At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, Input t_r,t_f=20 ns, and C_L=50 pF, R_L=200 kΩ

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS		UNITS
	V_{DD} Volts	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}	5	125	250	ns
	10	60	120	
	15	45	90	
Transition Time, t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance, C_{IN}	Any Input	−	5	7.5	pF
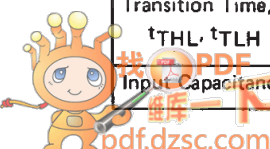
CD4073B, CD4081B, CD4082B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	—	0,5	5	0.25	0.25	7.5	7.5	—	0.01	0.25	μA
	—	0,10	10	0.5	0.5	15	15	—	0.01	0.5	
	—	0,15	15	1	1	30	30	—	0.01	1	
	—	0,20	20	5	5	150	150	—	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	—	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	—	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	—	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	—	
Output Voltage: Low-Level, V_{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	—	0,5	5	4.95				4.95	5	—	
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V_{IL} Max.	0.5	—	5	1.5				—	—	1.5	V
	1	—	10	3				—	—	3	
	1.5	—	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	—	$±10^{-5}$	±0.1	μA

Fig. 3 — Typical voltage transfer characteristics.
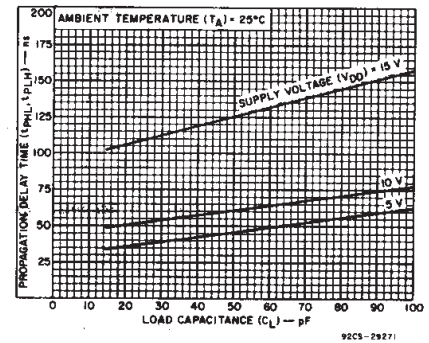
Fig. 4 — Typical propagation delay time as a function of load capacitance.

Fig. 1 — Schematic diagram for CD4081B (1 of 4 identical gates).

*ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

Fig. 2 — Logic diagram for CD4081B (1 of 4 identical gates).

Fig. 5 — Typical output low (sink) current characteristics.

Fig. 6 — Minimum output low (sink) current characteristics.

Fig. 7 — Schematic diagram for CD4082B (1 of 2 identical gates).

*ALL INPUTS ARE PROTECTED BY
CMOS PROTECTION NETWORK

Fig. 9 — Logic diagram for CD4082B (1 of 2 identical gates).

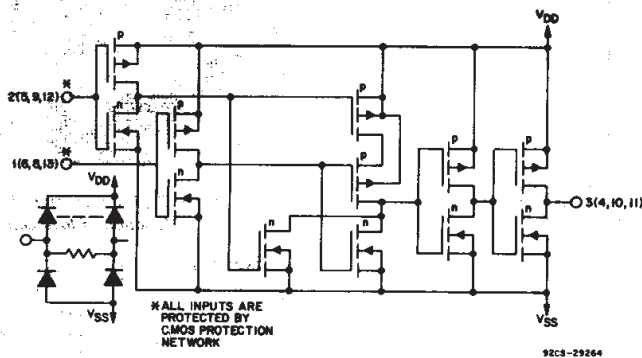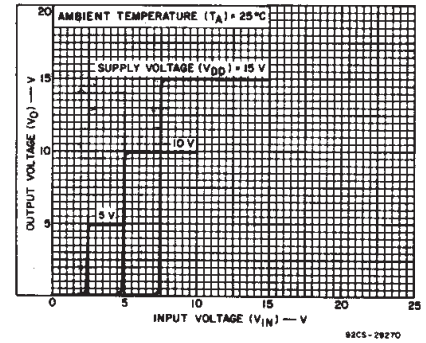
*ALL INPUTS ARE PROTECTED BY
CMOS PROTECTION NETWORK

Fig. 11 — Schematic diagram for CD4073B (1 of 3 identical gates).

Fig. 13 — Logic diagram for CD4073B (1 of 3 identical gates).
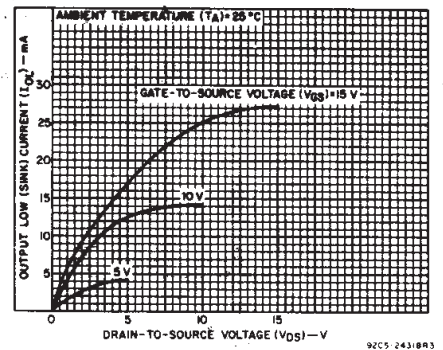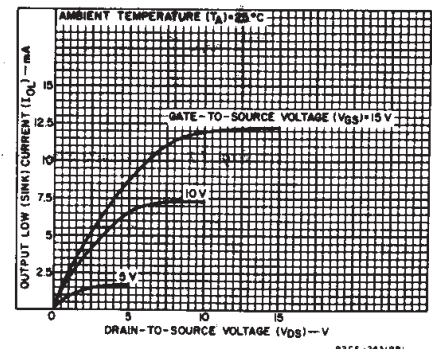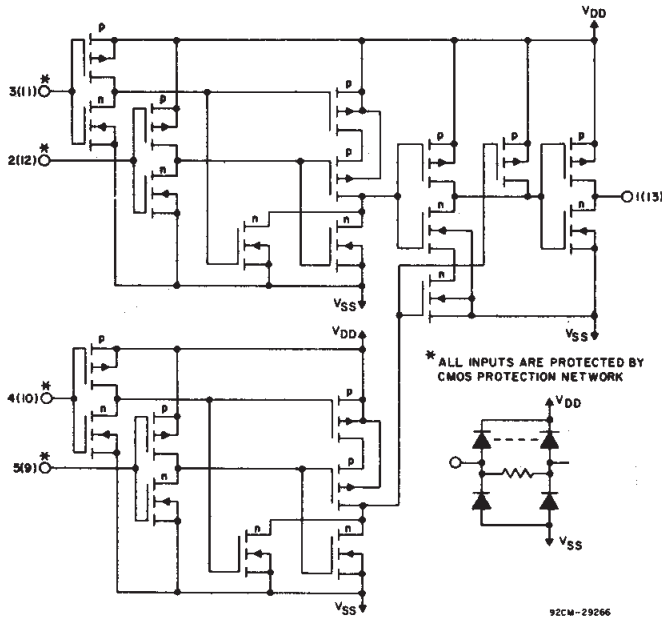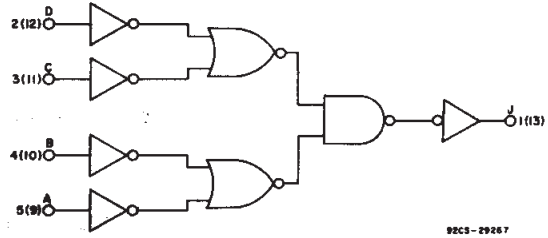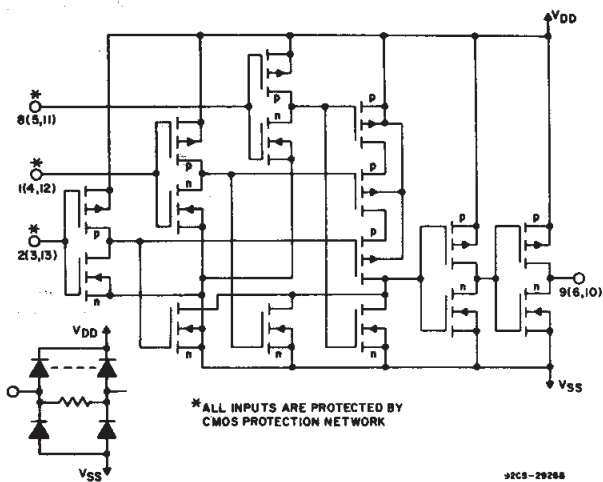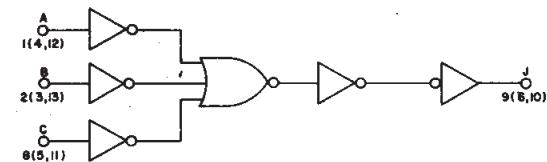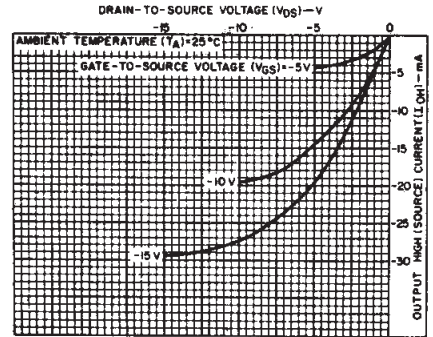

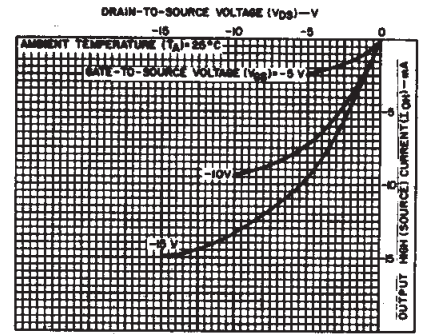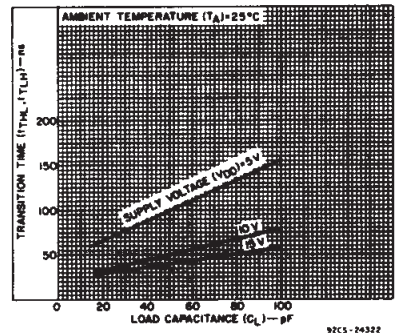Fig. 8 — Typical output high (source)
current characteristics.

Fig. 10 — Minimum output high (source)
current characteristics.

Fig. 12 — Typical transition time as a
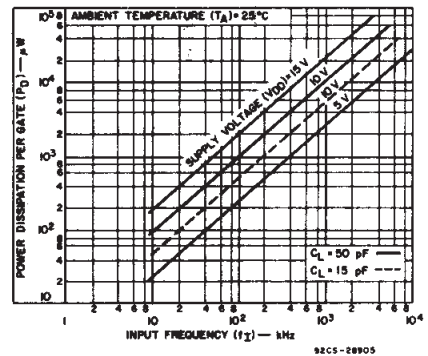function of load capacitance

Fig. 14 — Typical dynamic power dissi-
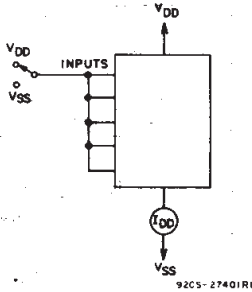pation per gate as a function
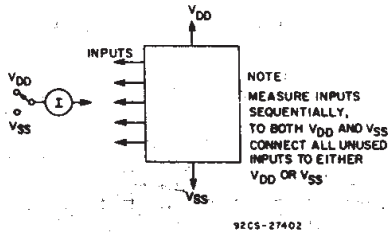of frequency.

Fig. 15 — Quiescent device current test circuit.

NOTE:
MEASURE INPUTS
SEQUENTIALLY,
TO BOTH V_{DD} AND V_{SS}.
CONNECT ALL UNUSED
INPUTS TO EITHER
V_{DD} OR V_{SS}.

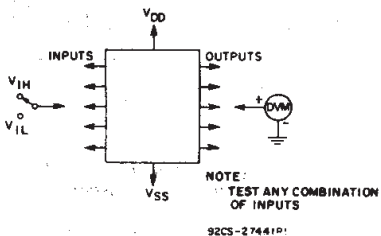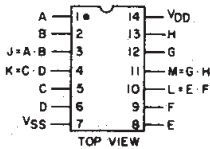Fig. 16 — Input current test circuit.

NOTE:
TEST ANY COMBINATION
OF INPUTS

Fig. 17 — Input-voltage test circuit.

TERMINAL ASSIGNMENTS
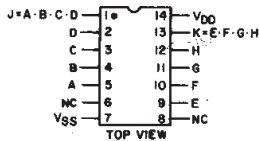
CD4081B
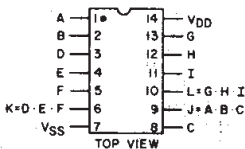

NC = NO CONNECTION
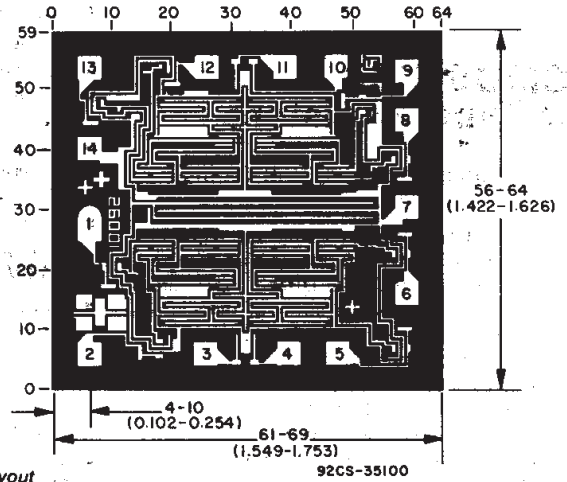
CD4082B

CD4073B

Chip dimensions and pad layout
for CD4081B.
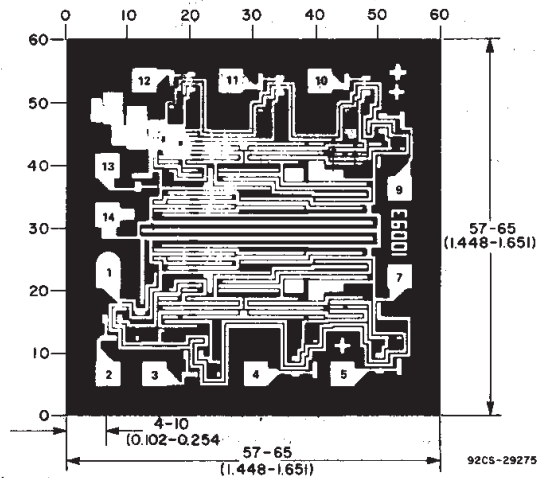
Chip dimensions and pad layout
for CD4082B.
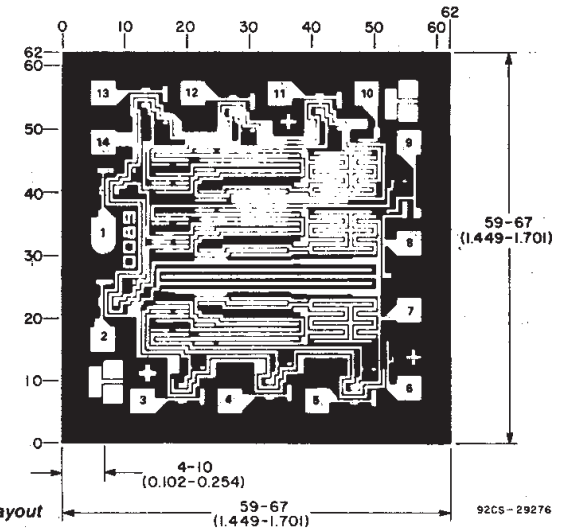
Dimensions in parentheses are in
millimeters and are derived from
the basic inch dimensions as in-
dicated. Grid graduations are in
mils (10^{-3} inch).

Chip dimensions and pad layout
for CD4073B.

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