# M8257
# PROGRAMMABLE DMA CONTROLLER

*Military*

- **Military Temperature Range: −55°C to +125°C ($T_{CASE}$)**
- **4-Channel DMA Controller**
- **Priority DMA Request Logic**
- **Channel Inhibit Logic**
- **Terminal Count and Modulo 128 Outputs**
- **Single TTL Clock**
- **Single +5V Supply**
- **Auto Load Mode**

The Intel M8257 is a 4-channel direct memory access (DMA) controller. It is specifically designed to simplify the transfer of data at high speeds for the Intel microcomputer systems. Its primary function is to generate, upon a peripheral request, a sequential memory address which will allow the peripheral to read or write data directly to or from memory. Acquisition of the system bus is accomplished via the CPU's hold function. The M8257 has priority logic that resolves the peripherals requests and issues a composite hold request to the CPU. It maintains the DMA cycle count for each channel and outputs a control signal to notify the peripheral that the programmed number of DMA cycles is complete. Other output control signals simplify sectored data transfers. The M8257 represents a significant savings in component count for DMA-based microcomputer systems and greatly simplifies the transfer of data at high speed between peripherals and memories.

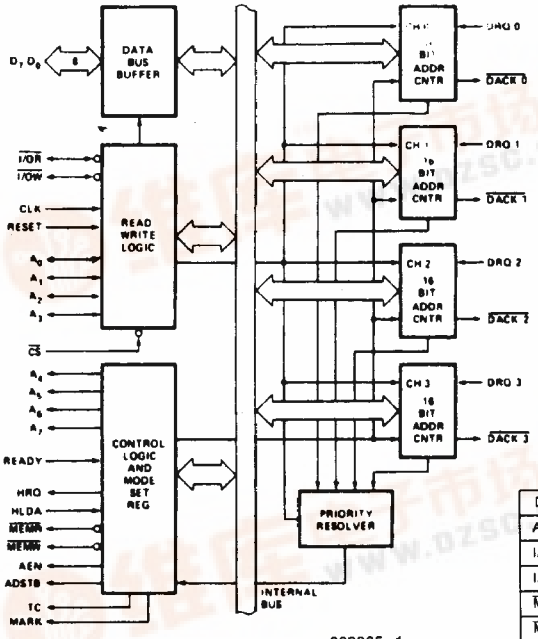


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**Figure 1. Block Diagram**


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| | |
|---|---|
| $D_7$–$D_0$ | Data Bus |
| $A_7$–$A_0$ | Address Bus |
| I/$\overline{OR}$ | I/O Read |
| I/$\overline{OW}$ | I/O Write |
| $\overline{MEMR}$ | Memory Read |
| $\overline{MEMW}$ | Memory Write |
| CLK | Clock Input |
| RESET | Reset Input |
| READY | Ready |
| HRQ | Hold Request (To M8080A) |
| HLDA | Hold Acknowledge (From M8080A) |

| | |
|---|---|
| AEN | Address Enable |
| ADSTB | Address Strobe |
| TC | Terminal Count |
| MARK | Modulo 128 Mark |
| $DRQ_3$–$DRQ_0$ | DMA Request Input |
| $\overline{DACK_3}$–$\overline{DACK_0}$ | DMA Acknowledge Out |
| $\overline{CS}$ | Chip Select |
| $V_{CC}$ | +5 Volts |
| GND | Ground |

**Figure 2. Pin Configuration**

## ABSOLUTE MAXIMUM RATINGS*

Case Temperature
Under Bias(1) ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... −0.5 to +7V
Power Dissipation ..... 1.0W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

## OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_C$ | Case Temperature (Instant On) | −55 | +125 | °C |
| $V_{CC}$ | Digital Supply Voltage | 4.50 | 5.50 | V |

## D.C. CHARACTERISTICS (Over Specified Operating Conditions)

| Symbol | Parameter | Min | Max | Unit | Comments |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | −0.5 | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | 2.2 | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output Low Voltage | | 0.45 | V | $I_{OL}$ = 1.6 mA |
| $V_{OH}$ | Output High Voltage | 2.4 | $V_{CC}$ | V | $I_{OH}$ = −150 μA for AB, DB and AEN<br>$I_{OH}$ = −80 μA for Others |
| $V_{HH}$ | HRQ Output High Voltage | 3.3 | $V_{CC}$ | V | $I_{OH}$ = −80 μA |
| $I_{CC}$ | $V_{CC}$ Current Drain | | 150 | mA | |
| $I_{IL}$ | Input Leakage | | ±10 | μA | $V_{SS} \le V_{IN} \le V_{CC}$ |
| $I_{OFL}$ | Output Leakage During Float | | ±10 | μA | $V_{SS}$ + 0.45 $\le V_{OUT} \le V_{CC}$ |

## CAPACITANCE $T_C$ = 25°C, $V_{CC}$ = GND = 0V

| Symbol | Parameter | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 10 | pF | fc = 1 MHz |
| $C_{I/O}$ | I/O Capacitance | | | 20 | pF | Unmeasured Pins Returned to GND |

## A.C. CHARACTERISTICS—DMA (MASTER) MODE

(Over Specified Operating Conditions)

### TIMING REQUIREMENTS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_{CY}$ | Cycle Time (Period) | 0.320 | 4 | μs |
| $T_\theta$ | Clock Active (High) | 120 | 0.8 $T_{CY}$ | ns |
| $T_{QS}$ | DRQ ↑ Setup to θ ↓ (S1, S4) | 120 | | ns |
| $T_{QH}$ | DRQ ↓ Hold from HLDA ↑ (4) | 0 | | ns |
| $T_{HS}$ | HLDA ↑ or ↓ Setup to θ ↓ (S1, S4) | 100 | | ns |
| $T_{RS}$ | READY Setup Time to θ ↑ (S3, Sw) | 30 | | ns |
| $T_{RH}$ | READY Hold Time from θ ↑ (S3, Sw) | 30 | | ns |

## A.C. CHARACTERISTICS—DMA (MASTER) MODE

(Over Specified Operating Conditions)

### TIMING RESPONSES

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_{DQ}$ | HRQ ↑ or ↓ Delay from θ ↑ (SI, S4) (Measured at 2.0V)(1) | | 180 | ns |
| $T_{DQ1}$ | HRQ ↑ or ↓ Delay from θ ↑ (SI, S4) (Measured at 3.3V)(3) | | 270 | ns |
| $T_{AEL}$ | AEN ↑ Delay from θ ↓ (S1)(1) | | 300 | ns |
| $T_{AET}$ | AEN ↓ Delay from θ ↑ (SI)(1) | | 200 | ns |
| $T_{AEA}$ | Adr(AB)(Active) Delay from AEN ↑ (S1)(4) | 20 | | ns |
| $T_{FAAB}$ | Adr(AB)(Active) Delay from θ ↑ (S1)(2) | | 270 | ns |
| $T_{AFAB}$ | Adr(AB)(Float) Delay from θ ↑ (SI)(2) | | 200 | ns |
| $T_{ASM}$ | Adr(AB)(Stable) Delay from θ ↑ (S1)(2) | | 250 | ns |
| $T_{AH}$ | Adr(AB)(Stable) Hold from θ ↑ (S1)(2) | $T_{ASM} - 50$ | | ns |
| $T_{AHR}$ | Adr(AB)(Valid) Hold from $\overline{Rd}$ ↑ (S1, SI)(4) | 60 | | ns |
| $T_{AHW}$ | Adr(AB)(Valid) Hold from $\overline{Wr}$ ↑ (S1, SI)(4) | 300 | | ns |
| $T_{FADB}$ | Adr(DB)(Active) Delay from θ ↑ (S1)(2) | | 300 | ns |
| $T_{AFDB}$ | Adr(DB)(Float) Delay from θ ↑ (S2)(2) | $T_{STT} + 20$ | 250 | ns |
| $T_{ASS}$ | Adr(DB) Setup to AdrStb ↓ (S1–S2)(4) | 100 | | ns |
| $T_{AHS}$ | Adr(DB)(Valid) Hold from AdrStb ↓ (S2)(4) | 50 | | ns |
| $T_{STL}$ | AdrStb ↑ Delay from θ ↑ (S1)(1) | | 200 | ns |
| $T_{STT}$ | AdrStb ↓ Delay from θ ↑ (S2)(1) | | 160 | ns |
| $T_{SW}$ | AdrStb Width (S1–S2)(4) | $T_{CY} - 100$ | | ns |
| $T_{ASC}$ | $\overline{Rd}$ ↓ or $\overline{Wr}$(Ext) ↓ Delay from AdrStb ↓ (S2)(4) | 70 | | ns |
| $T_{DBC}$ | $\overline{Rd}$ ↓ or $\overline{Wr}$(Ext) ↓ Delay from Adr(DB) (Float)(S2)(4) | 20 | | ns |
| $T_{AK}$ | DACK ↑ or ↓ Delay from θ ↓ (S2, S1) and TC/Mark ↑ Delay from θ ↑ (S3) and TC/Mark ↓ Delay from θ ↑ (S4)(1)(5) | | 270 | ns |
| $T_{DCL}$ | $\overline{Rd}$ ↓ or $\overline{Wr}$(Ext) ↓ Delay from θ ↑ (S2) and $\overline{Wr}$ ↓ Delay from θ ↑ (S3)(2)(6) | | 250 | ns |
| $T_{DCT}$ | $\overline{Rd}$ ↑ Delay fromθ ↓ (S1, SI) and $\overline{Wr}$ ↑ Delay from θ ↑ (S4)(2)(7) | | 200 | ns |
| $T_{FAC}$ | $\overline{Rd}$ or $\overline{Wr}$(Active) from θ ↑ (S1)(2) | | 300 | ns |
| $T_{AFC}$ | $\overline{Rd}$ or $\overline{Wr}$(Float) from θ ↑ (SI)(2) | | 170 | ns |
| $T_{RWM}$ | $\overline{Rd}$ Width (S2–S1 or SI)(4) | $2T_{CY} + T_{\theta} - 50$ | | ns |
| $T_{WWM}$ | $\overline{Wr}$ Width (S3–S4)(4) | $T_{CY} - 50$ | | ns |
| $T_{WWME}$ | $\overline{Wr}$(Ext) Width (S2–S4)(4) | $2T_{CY} - 50$ | | ns |

**NOTES:**
1. Load = 1 TTL.
2. Load = 1 TTL + 50 pF.
3. Load = 1 TTL + ($R_L$ = 3.3K), $V_{OH}$ = 3.3V.
4. Tracking Parameter.
5. $\Delta T_{AK} < 50$ ns.
6. $\Delta T_{DCL} < 50$ ns.
7. $\Delta T_{DCT} < 50$ ns.

## A.C. CHARACTERISTICS—PERIPHERAL (SLAVE) MODE
(Over Specified Operating Conditions)

### M8080A BUS PARAMETERS

#### READ CYCLE

| Symbol | Parameter | Min | Max | Unit | Comments |
|---|---|---|---|---|---|
| $T_{AR}$ | Adr or $\overline{CS}\downarrow$ Setup to $\overline{RD}\downarrow$ | 0 | | ns | |
| $T_{RA}$ | Adr or $\overline{CS}\uparrow$ Hold from $\overline{RD}\uparrow$ | 0 | | ns | |
| $T_{RD}$ | Data Access from $\overline{RD}\downarrow$ | 0 | 300 | ns | (Note 2) |
| $T_{DF}$ | DB $\rightarrow$ Float Delay from $\overline{RD}\uparrow$ | 20 | 150 | ns | |
| $T_{RR}$ | $\overline{RD}$ Width | 250 | | ns | |

#### WRITE CYCLE

| Symbol | Parameter | Min | Max | Unit | Comments |
|---|---|---|---|---|---|
| $T_{AW}$ | Adr Setup to $\overline{WR}\downarrow$ | 20 | | ns | |
| $T_{WA}$ | Adr Hold from $\overline{WR}\uparrow$ | 35 | | ns | |
| $T_{DW}$ | Data Setup to $\overline{WR}\uparrow$ | 200 | | ns | |
| $T_{WD}$ | Data Hold from $\overline{WR}\uparrow$ | 10 | | ns | |
| $T_{WW}$ | $\overline{WR}$ Width | 175 | | ns | |

#### OTHER TIMING

| Symbol | Parameter | Min | Max | Unit | Comments |
|---|---|---|---|---|---|
| $T_{RSTW}$ | Reset Pulse Width | 300 | | ns | |
| $T_{RSTD}$ | Power Supply $\uparrow$ ($V_{CC}$) Setup to Reset $\downarrow$ | 500 | | $\mu$s | |
| $T_r$ | Signal Rise Time | | 20 | ns | |
| $T_f$ | Signal Fall Time | | 20 | ns | |
| $T_{RSTS}$ | Reset to First $\overline{I/OWR}$ | 2 | | $t_{CY}$ | |

**NOTES:**
1. All timing measurements are made at the following reference voltages unless specified otherwise:
Input "1" at 2.0V, "0" at 0.8V.
Output "1" at 2.0V, "0" at 0.8V.
2. M8257: $C_L$ = 100 pF.

### TRACKING PARAMETERS

Signals labeled as Tracking Parameters (footnotes 4–7 under A.C. Specifications) are signals that follow similar paths through the silicon die. The propagation speed of these signals varies in the manufacturing process but the relationship between all these parameters is constant. The variation is less than or equal to 50 ns.

Suppose the following timing equation is being evaluated,

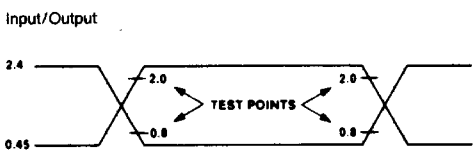
$$T_{A(MIN)} + T_{B(MAX)} \leq 150 \text{ ns}$$

and only minimum specifications exist for $T_A$ and $T_B$. If $T_{A(MIN)}$ is used, and if $T_A$ and $T_B$ are tracking parameters, $T_{B(MAX)}$ can be taken as $T_{B(MIN)}$ + 50 ns.

$$T_{A(MIN)} + (T_{B(MIN)}^{*} + 50 \text{ ns}) \leq 150 \text{ ns}$$

*If $T_A$ and $T_B$ are tracking parameters.

### A.C. TESTING INPUT, OUTPUT WAVEFORM

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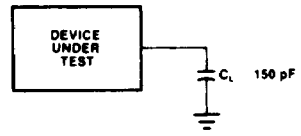
A.C. Testing: Inputs are Driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing Measurements are Made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

### A.C. TESTING LOAD CIRCUIT

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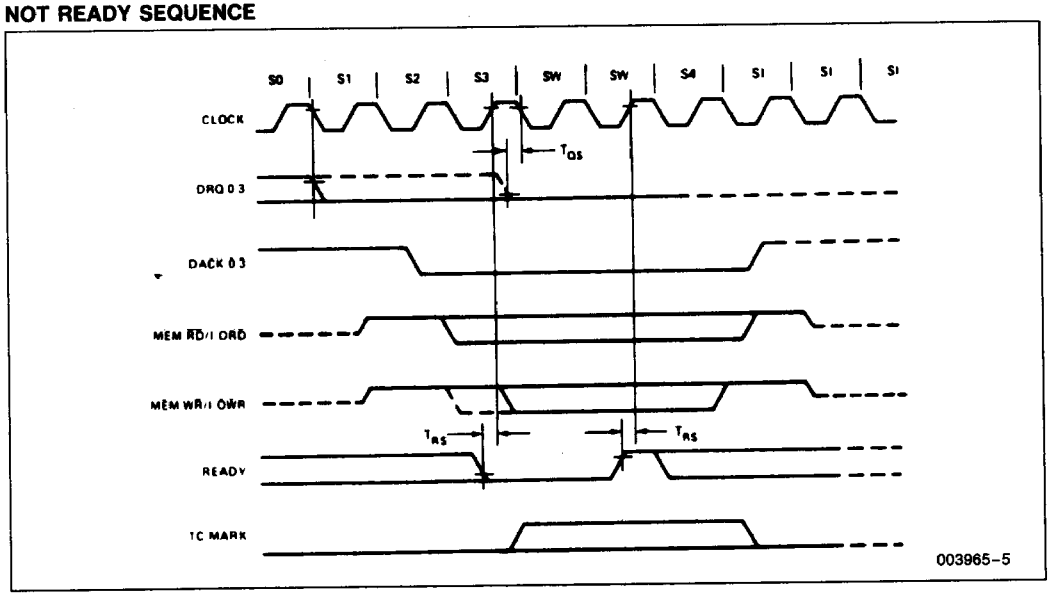
$C_L$ = 150 pF
$C_L$ Includes Jig Capacitance

## WAVEFORMS

### NOT READY SEQUENCE

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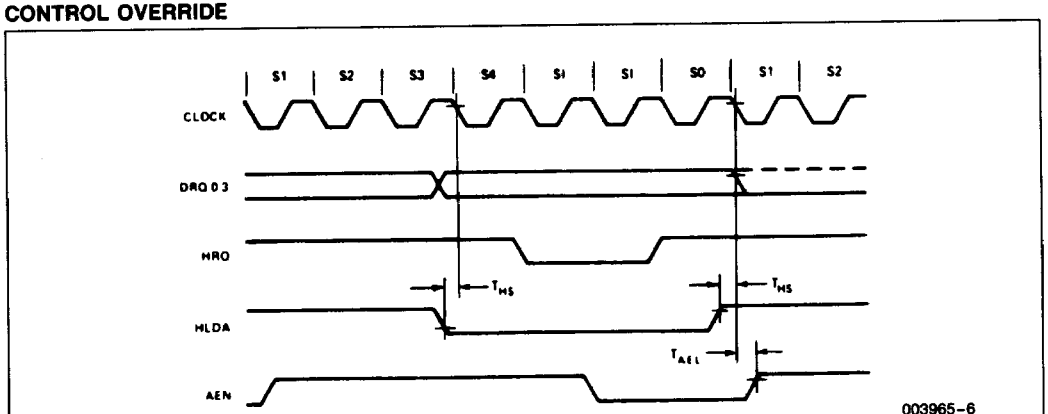
### CONTROL OVERRIDE

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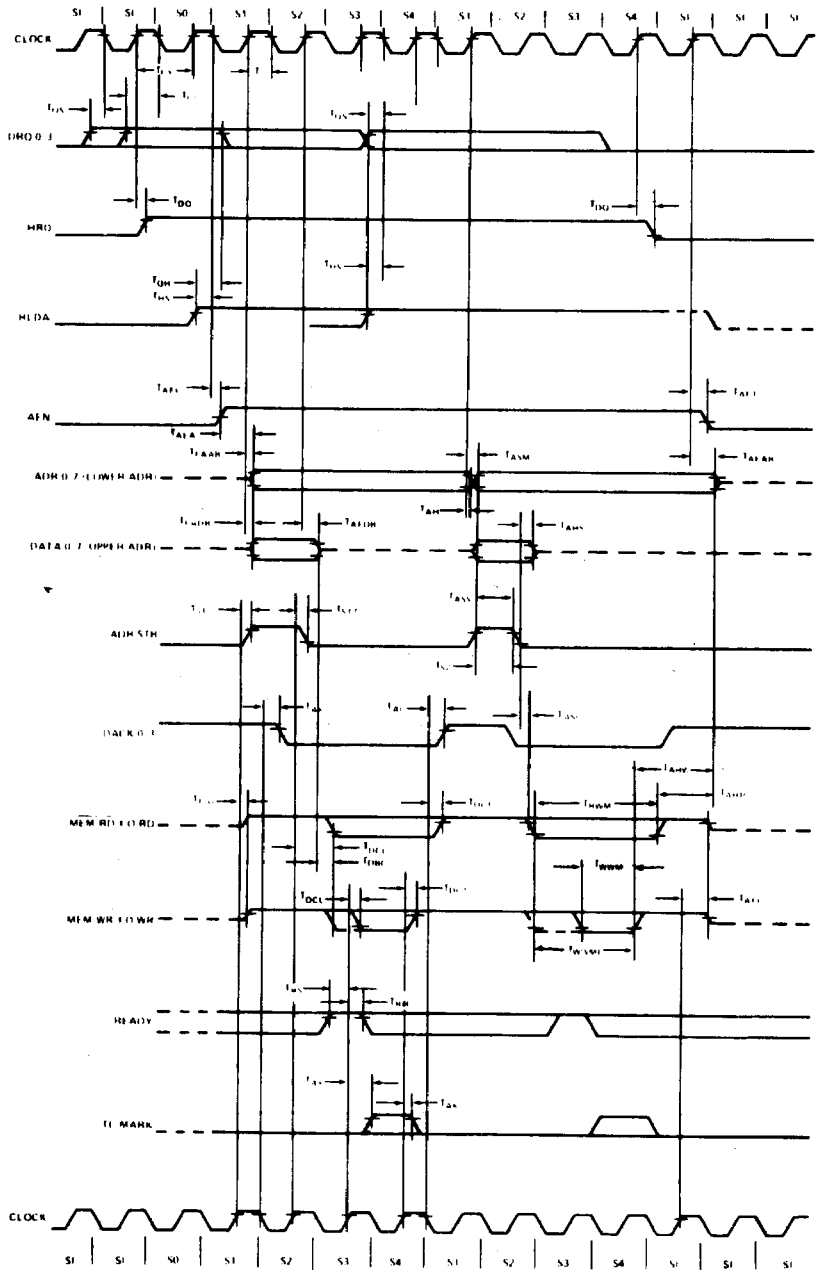
## WAVEFORMS—DMA MODE

### CONSECUTIVE CYCLES AND BURST MODE SEQUENCE

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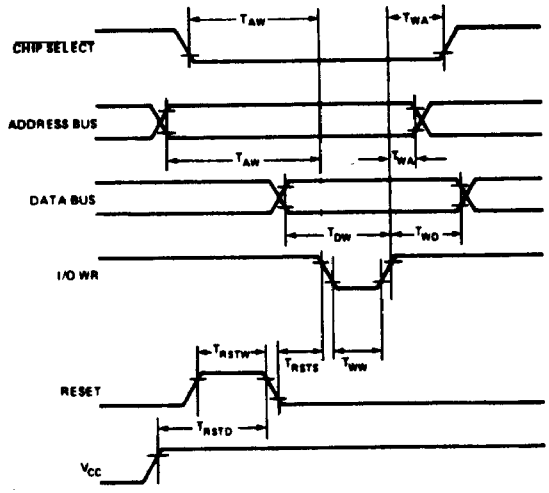
**NOTE:**
The clock waveform is duplicated for clarity. The M8257 requires only one clock input.

## WAVEFORMS—PERIPHERAL MODE

### WRITE

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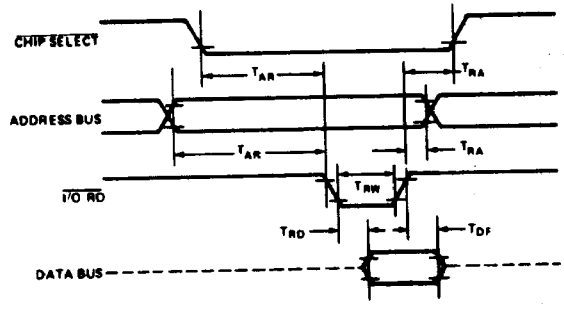
### READ

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