ADVANCE INFORMATION

82731
VIDEO INTERFACE CONTROLLER

- Parallel to Serial Data Conversion
- On-Chip Clock Generator
- High Video Dot Rates
  80 MHz—82731-2
  50 MHz—82731
- Character up to 16 Dots Wide
- Proportional Character Spacing
- On-Chip Character Attribute Processing
- Control Functions to Provide Screen Reverse Video, Video Clock, Synchronization and Tab Function
- Single 5V Power Supply
- 40 Pin DIP
- All Inputs and Outputs TTL Compatible Except Video Output which is ECL

The 82731 is a general purpose video interface which generates a serial video signal output from parallel character and attribute information coming from the character generator and the 82730 Text Coprocessor. With a character generator and minimal hardware, the 82731 will comprise a complete video interface system for the 82730 Text Coprocessor and the CRT monitor.

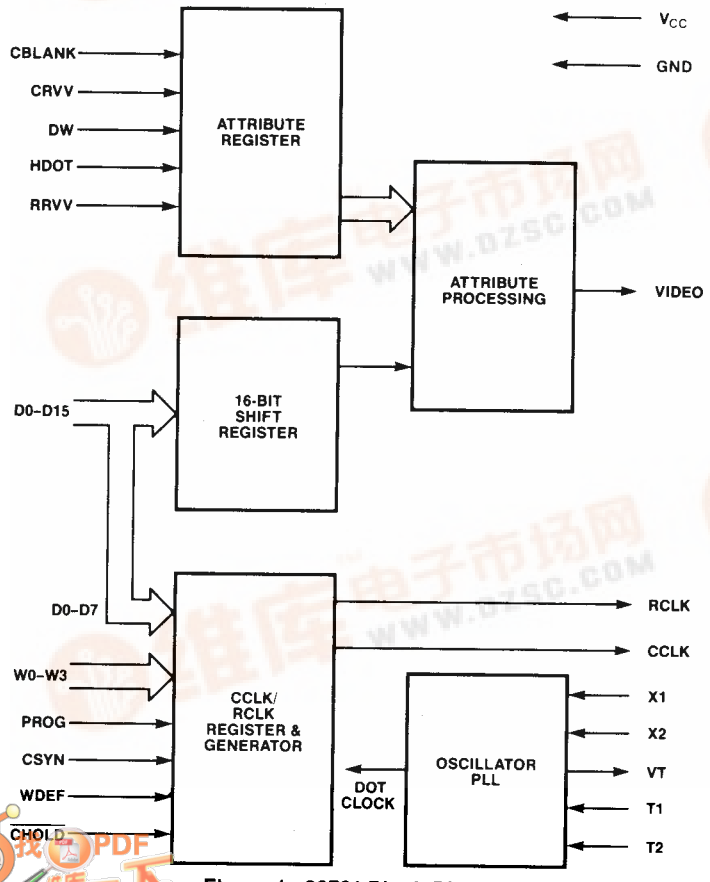


Figure 1. 82731 Block Diagram

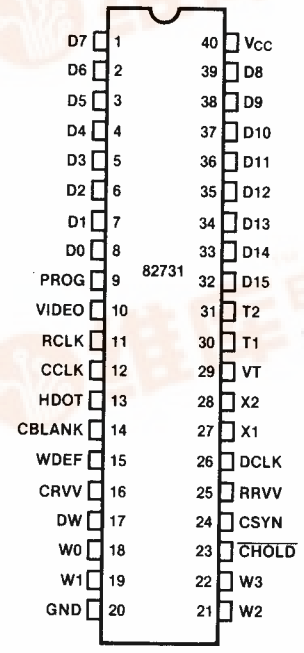


Figure 2. 82731 Pin Configuration

Table 1. 82731 Pin Description

Symbol	Pin Number	Type	Name and Function
D0-D15	8-1, 39-32	I	Character data parallel inputs.
PROG	9	I	Program control input; used to program default width values of CCLK and RCLK; these are latched into the 82731 via D0-D7 at the rising edge of CCLK (PROG is active high).
VIDEO	10	O	Video output; provides the dot information clocked by the internal dot clock.
RCLK	11	O	Reference clock output; used to generate timings for the screen columns for data formatting and video signals. The period of RCLK is programmable from 6 to 21 times the period of the internal dot clock.
CCLK	12	O	Character clock output; used to clock character and attribute information out of the CRT controller. The period of CCLK is programmable from 3 to 18 times the period of the internal dot clock.
HDOT	13	I	Half dot shift input; the video signal at the video output will be delayed by half dot clock for character rounding (active high).
CBLANK	14	I	Character blank attribute input; the video output is blanked (active high).
WDEF	15	I	Width defeat attribute input; the CCLK period is set to a preprogrammed default value (active high).
CRVV	16	I	Character reverse video attribute input; inverts the character data from D0-D15 (active high).
DW	17	I	Double width attribute input; the internal dot clock frequency and the CCLK frequency are divided by two (active high). The RCLK frequency remains unchanged.
W0-W3	18, 19, 21, 22	I	Clock width inputs; they are used for programming the CCLK clock width on a character by character basis.
$\overline{\text{CHOLD}}$	23	I	CCLK inhibit input; this signal inhibits CCLK generation and is used for TAB function (active low).
CSYN	24	I	CCLK synchronization input; CCLK will be synchronized to RCLK and the video output signal is defined by RRVV (active high).
RRVV	25	I	Field reverse video input; the video signal at the video output will be inverted (active high).
DCLK	26	O	Dot clock output; ECL-level signal; must be connected to a 3.3k resistor to ground if used.
X1-X2	27, 28	I	Inputs for fundamental mode crystal; its frequency must be 1/8 of the required dot clock frequency.
VT	29	O	Tuning voltage for PLL-VCO; this output is used to tune the LC-circuit and thus control the oscillator frequency of the internal dot clock.
T1-T2	30, 31	I	LC-circuit inputs for PLL-VCO. T1 can be used to provide the 82731 with an external TTL-level clock at twice the dot clock frequency.
VCC	40	-	+5V power supply
6ND	20	-	Ground (0V)

FUNCTIONAL DESCRIPTION

The Video Interface Controller, 82731, in a typical CRT system shown in Figure 3, interfaces the Text Coprocessor to the CRT video terminal. It receives the parallel data along with the attribute and control information from the Text Coprocessor, processes it into a serial video signal which can be fed to a video CRT terminal. It also generates the basic dot clock (DCLK), character clock (CCLK) and the reference clock (RCLK) signals required by the Text Coprocessor.

CRT terminals requiring very high resolution, extremely stable and absolutely flicker-free picture place special demands on the dot rate generator. In such applications dot rates up to 80 MHz are necessary. This allows 12.5 ns per dot (pixel) for converting data, attribute and control information into serial form for the video terminal.

The functionality of the 82731 is largely determined by the complexity and the demands of the CRT controller it supports. Figure 1 shows the block diagram of the Video Interface Controller. The dot clock is generated by voltage controlled LC circuit connected at T1 and T2. Another clock is generated which is crystal controlled and has frequency 1/8 of the dot clock. This is used to stabilize the dot clock using an on-chip phase locked loop (PLL). This two-oscillator concept enables the use of low cost, fundamental mode crystals even for generating frequencies up to 80 MHz.

The 16 bit shift register receives parallel inputs from pins D0-D15. This allows a maximum character width of 16 dots. The minimum width is 3 dots. The character width is programmable through pins W0-W3 for proportional character spacing. This also determines the character clock (CCLK) frequency. Programming of the default character width and the reference clock (RCLK) is done through inputs D0-D7 and PROG. Signal WDEF can be used to switch between the default character width and the one specified dynamically through the lines W0-W3. When using variable character width, for example, in generating tables on the screen, it is essential that every entry in a column starts at the same dot distance (and not the character distance) from the start of line. The 82731 supports this requirement by providing a tab function using CSYN and $\overline{\text{CHOLD}}$ signals to synchronize with the reference clock (RCLK).

It is possible to shift any scan line of any character by half a dot using the HDOT signal. This feature, known as character rounding, further enhances the quality of high resolution character displays. Other features, like character blinking, reverse video etc., which improve the readability of text on screen are directly supported by the 82731 using signals CRVV and RRVV from the Text Coprocessor, processing them and affecting the final video signal to show the characters with the desired attributes.

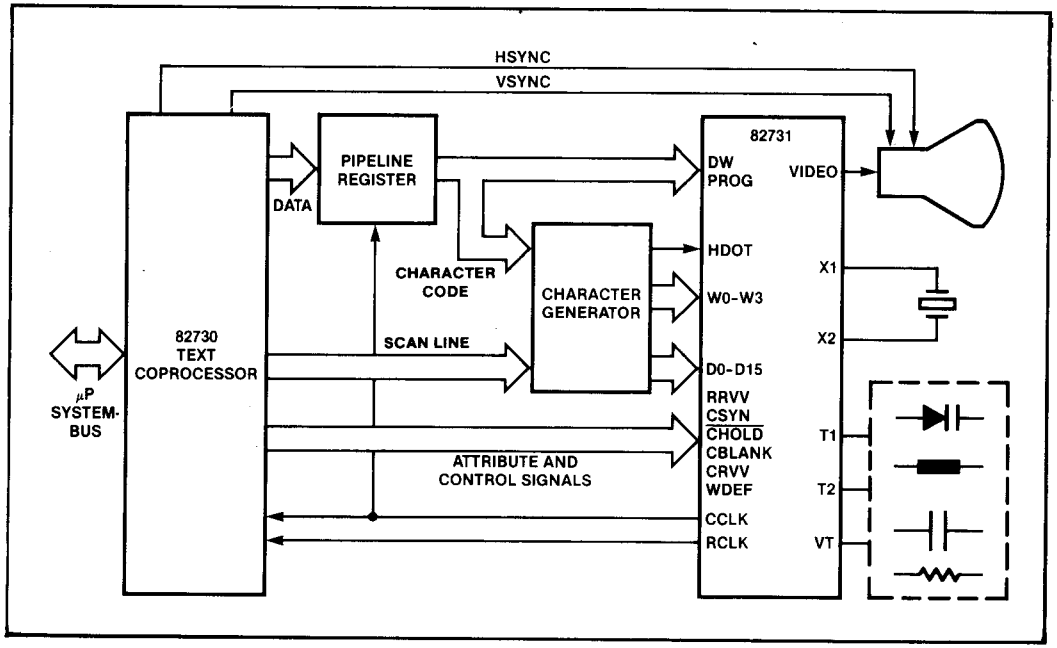


Figure 3. CRT System Block Diagram

Clock Generation

The most fundamental clock required to run the CRT display is the dot clock which provides the reference for the dot data to be shifted serially to the CRT. In addition, it is the basis for the character clock (CCLK) and the reference clock (RCLK) required by the 82730.

Dot Clock

The dot clock is derived from an on-chip oscillator which runs at twice the normal dot clock (DCLK) frequency. A voltage-controlled LC circuit is connected to the T1, T2 pins, to create a voltage-controlled oscillator (VCO). The 82731 compares the phase of this oscillator with another on-chip oscillator controlled by a crystal attached to the X1, X2 pins. This oscillator runs at 1/8 the normal DCLK frequency to allow using inexpensive low-frequency crystals. The on-chip PLL circuit produces an error voltage via the VT pin which locks the VCO to the 16th harmonic of the crystal frequency (see Figure 4a).

Alternatively the 82731 can be supplied with an external TTL-level clock at twice the normal DCLK frequency via the T1 pin, as shown in Figure 4b.

When the Double Width (DW) input is active, the DCLK frequency is divided to 1/2 its normal value. This affects the DCLK, CCLK, and VIDEO outputs, but not RCLK.

Designing the Oscillator Circuit

The whole external oscillator circuit consists of three parts:
—the crystal circuit,
—the voltage controlled LC-circuit, and
—the loop filter for the PLL.

Figure 5a shows the general crystal circuit. The crystal must be a fundamental mode series resonant type with a resonant frequency of 1/8 of the desired dot clock frequency. The capacitor C_X is necessary if a fine adjustment of the dot clock rate must be

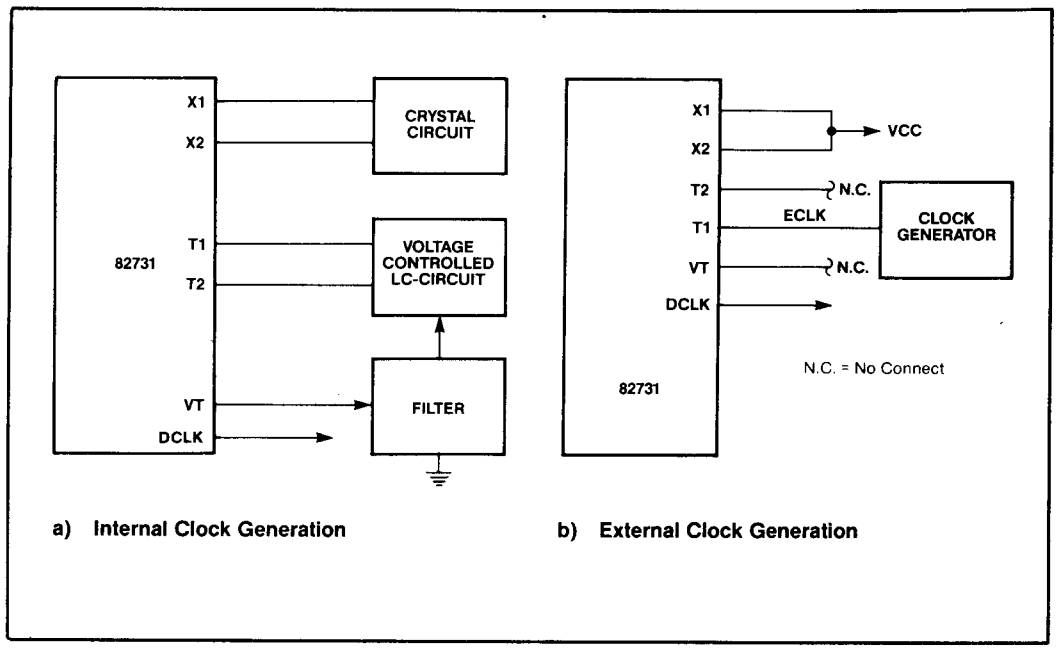
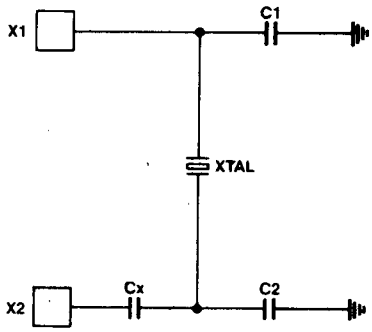


Figure 4. Clock Generation

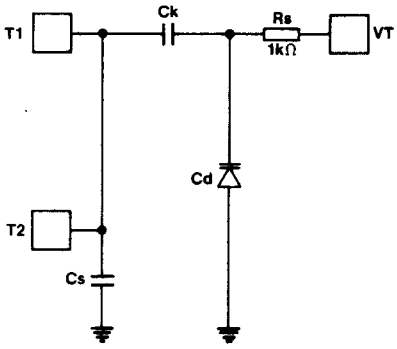


a) Crystal Circuit

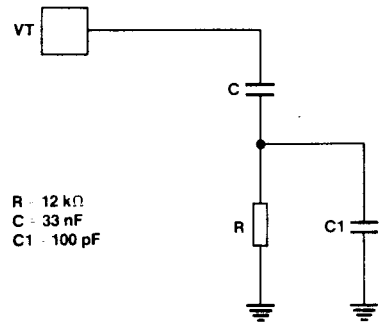
Cx (pF)	FDCLK (MHz)
2.2	64.053
6.8	64.016
15	63.987
33	63.966

(nominal crystal frequency 8 MHz)

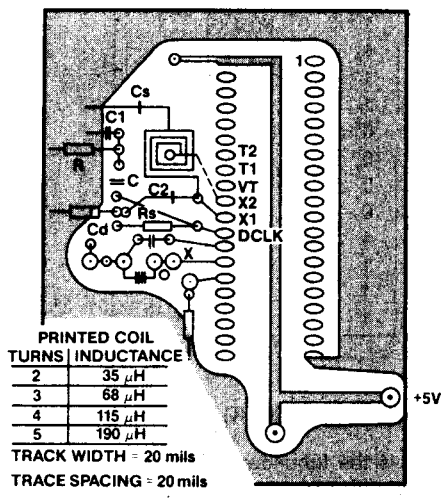
b) Example of the influence of Cx on the dot clock frequency



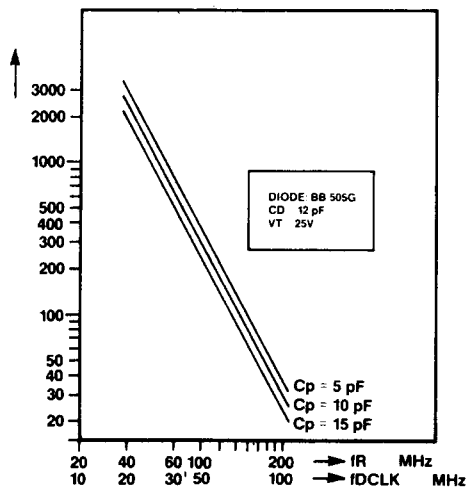
c) VCO circuit



d) PLL - loop filter



e) Example layout for printed circuit



f) L/f-diagram

Figure 5. Designing the Oscillator Circuit

made. Figure 5b shows an example how the dot clock frequency can vary with different values of Cx. The capacitors C1 and C2 may be necessary to suppress overtone oscillations if the crystal frequency is below 6 MHz. The exact values depend on the crystal used and must be determined empirically. The recommended ranges are 0 to 10 pF for C1 and 0 to 100 pF for C2.

The voltage controlled LC-circuit is shown in Figure 5c. The effective resonant circuit consists of the inductance L, the capacitance Cd of the varactor diode and the parasitic capacitance Cp. Its resonant frequency is

$$fR = \frac{1}{2\pi\sqrt{L \cdot (Cd + Cp)}}$$

where fR must be 2 × fDCLK. The value of Cp depends on many factors (e.g. layout, single/multilayer board . . .), thus it changes from application to application. However a value of 5 to 15 pF seems to be a good approximation.

The value of DC (varactor diode) should be determined at a control voltage of 2.5 V to get the lock-in-range as wide as possible. The variation of VT ranges from 1 V to VCC-1 which results in a minimum frequency shift of about 6-8% in relation to the center frequency at 2.5 V.

The value of the inductance L must be determined in such a way that the resulting center frequency lies as near as possible to the needed frequency fR = 2 × fDCLK to guarantee a stable dot clock under all operation conditions. Figure 5f shows a diagram that will help to find the needed inductance L. It is based on the use of a varactor diode (Siemens BB 505G) that has a capacitance of 12 pF at a control voltage of 2.5 V. The use of other diodes will of course lead to other diagrams.

At dot clock frequencies higher than 50 MHz the needed inductance becomes lower than 100 μH. In these cases it is better to integrate the inductance into the board layout. Figure 5e shows a possible layout for the external oscillator circuit and approximate (measured) values of the inductance of the printed coil (trace width and trace spacing 20 mils).

The loop filter converts the current pulses at the VT pin into the control voltage VT for the VCO. it is an essential part of the PLL and affects the lock-in-range and stability of the PLL. A second order filter that was found to work well under all operation conditions and over the full frequency range is shown in Figure 5d.

Reference Clock (RCLK)

RCLK is the reference clock output used to generate video timing and to define screen columns for data formatting and tabulor locations. In addition, it is used to clock the field attribute signals into the 82731. The period of RCLK is programmable from 6 to 21 times the period of the dot clock, i.e. the RCLK hightime is 3 dot clock periods and the RCLK lowtime is programmable from 3 to 18 dot clock periods. It is programmed via D4-D7 at the rising edge of CCLK, when PROG is active (see Table 1 and Figure 6).

The RCLK clock width should be programmed only once after a system reset.

Table 1. Programming RCLK

D7	D6	D5	D4	PROG	RCLK Period (dot clocks)
0	0	0	0	1	16
0	0	0	1	1	17
0	0	1	0	1	18
0	0	1	1	1	19
0	1	0	0	1	20
0	1	0	1	1	21
0	1	1	0	1	6
0	1	1	1	1	7
1	0	0	0	1	8
1	0	0	1	1	9
1	0	1	0	1	10
1	0	1	1	1	11
1	1	0	0	1	12
1	1	0	1	1	13
1	1	1	0	1	14
1	1	1	1	1	15

Character Clock (CCLK)

CCLK is the fundamental character clock output used to clock character and attribute information from the 87730.

It is a rising edge triggered clock and inside the active character field its period is programmable from 3 to 18 times the period of the dot clock, i.e. the

CLK hightime is 2 dot clock periods and the CCLK w time is programmable from 1 to 16 dot clock eriods.

/hen CSYN is active (normally outside the active naracter field) CCLK is forced to match RCLK. In iis case the CCLK high time is 3 dot clock periods istead of 2.

n order to support proportional spacing, the period f CCLK can be reprogrammed at the beginning of ach CCLK cycle (i.e. at the beginning of each haracter) if PROG is inactive.

Programming the character width is done via the clock width inputs W0-W3 according to Table 2. The W0-W3 input data is clocked into the 82731 at the rising edge of CCLK and defines the width of the currently displayed character (see Figure 7).

If the width defeat attribute (WDEF) is active, the period of CCLK will be set to the programmed default value ignoring the clock width inputs W0-W3. This value is programmable from 3 to 18 times the period of the dot clock via the D0-D3 inputs, when the PROG input is active (see Figure 6).

The default CCLK width should be programmed only once after a system reset.

The CCLK clock period will be doubled if the double width attribute (DW) is asserted at the rising edge of CCLK.

NOTE

If width of CCLK is programmed to 17 or 18, zeros are shifted out from the internal shift register after the 16 data bits and displayed according to the attribute signals.

Clock Initialization Sequence (PROG)

After power on the width of RCLK is a random value between 6 and 21 and the width of CCLK is a random value between 3 and 18.

The 82731 should be initialized in the following way:

- Activate the CSYN signal. CCLK is forced to match RCLK, which has a minimum clock width of 6 dot clock periods.
- Apply the clock width informations to D0-D3 and D4-D7 according to tables.
- Activate the PROG signal. The default width of CCLK and the width of RCLK are programmed at the next rising edge of CCLK (see Figure 6).
- Remove the PROG signal.

CSYN can be removed at the beginning of the next active data field.

Table 2. Programming CCLK

PROG = 1	D3	D2	D1	D0	CCLK Period (dot clocks)
PROG = 0	W3	W2	W1	W0	
	0	0	0	0	16
	0	0	0	1	17
	0	0	1	0	18
	0	0	1	1	3
	0	1	0	0	4
	0	1	0	1	5
	0	1	1	0	6
	0	1	1	1	7
	1	0	0	0	8
	1	0	0	1	9
	1	0	1	0	10
	1	0	1	1	11
	1	1	0	0	12
	1	1	0	1	13
	1	1	1	0	14
	1	1	1	1	15

Note:
PROG = 1: Programming the CCLK default clock width during the initialization phase via D0-D3 at the rising edge of CCLK.
PROG = 0: Programming the clock width of the current CCLK cycle via W0-W3 at the rising edge of CCLK.

Character Data Signals

The character data signals are normally provided by the character ROM and clocked into the 82731 at the rising edge of CCLK.

The character data signals consist of:

- the character data lines (D0-D15),
- the character width information (W0-W3), and
- the half dot shift signal (HDOT).

Dot Data (D0-D15)

The dot data signals will be clocked into the 82731 via the D0-D15 inputs at the rising edge of CCLK. The actual character width is defined by the W0-W3 inputs or the default width information previously programmed. The dot data will be displayed dependent on the control signals and on the corresponding attribute information. The data bits are serially shifted out at the video output starting with D0.

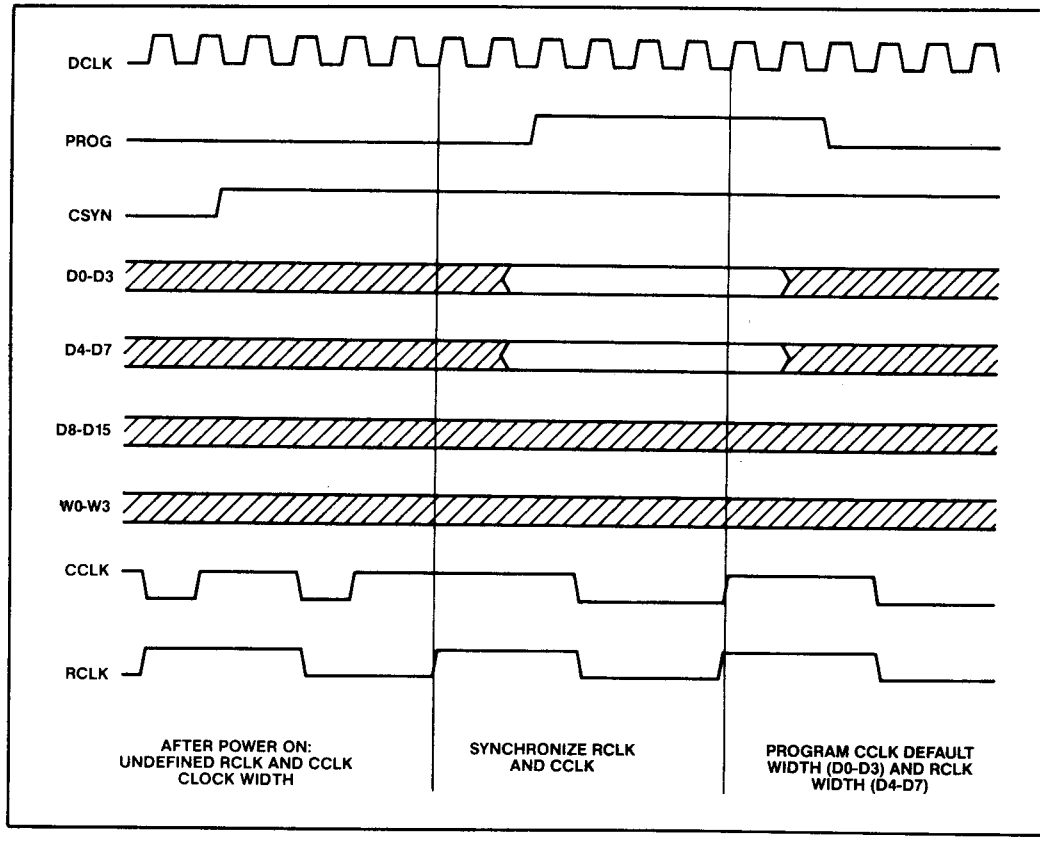


Figure 6. Clock Initialization

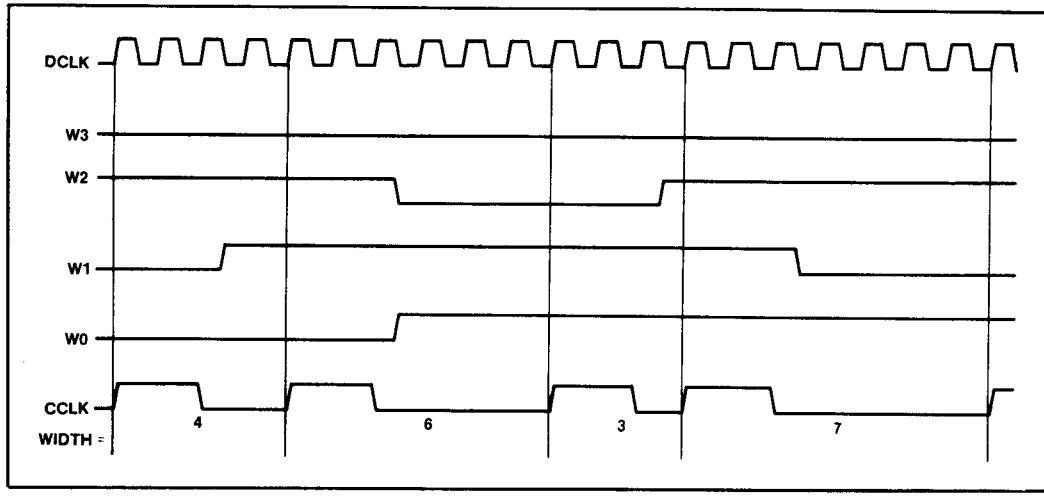


Figure 7. Action of Clock Width Inputs W0-W3 on CCLK

If CCLK width is greater than 16, zeros are shifted out for the rest of the dot clocks and displayed according to the attribute signals.

Character Width (W0-W3)

The W0-W3 inputs are clocked into the 82731 at the rising edge of CCLK and determine the width of the currently displayed character.

Half Dot Shift (HDOT)

The half dot shift signal is clocked into the 82731 at the rising edge of CCLK. When the half dot shift signal is active (high), the output of the video data will be delayed by half a dot time. The first dot of the character dot line is transmitted for one and a half dot clock period while the last dot of this character dot line is displayed for half a dot clock period. The remaining character dots are transmitted for one dot clock period and thus are shifted by half a dot.

The HDOT signal is not a character attribute signal, because it can change from scan line to scan line of a character. Thus it is reasonable to generate it from the character ROM, together with the dot data and the width information.

Character Attribute Signals

These signals are clocked into the 82731 at the rising edge of CCLK. Thus they are valid for the next character only.

The character attribute signals consist of:

- character blanking CBLANK,
- character reverse video CRVV,
- double width DW, and
- width defeat WDEF.

Outside the active character field (which is defined by the CSYN signal) all character attribute signals are ignored.

Character Blanking (CBLANK)

If CBLANK is active (high), the blank attribute will produce the effect of blanking the display of the character. When the CBLANK attribute is active, the corresponding dot data information D0-D15 will be as if all zeros were forced at the inputs. The video output can be inverted to all ones by simultaneously activating the CRVV attribute. Independent of these character oriented operations the video output signal is also affected by the RRVV field attribute signal.

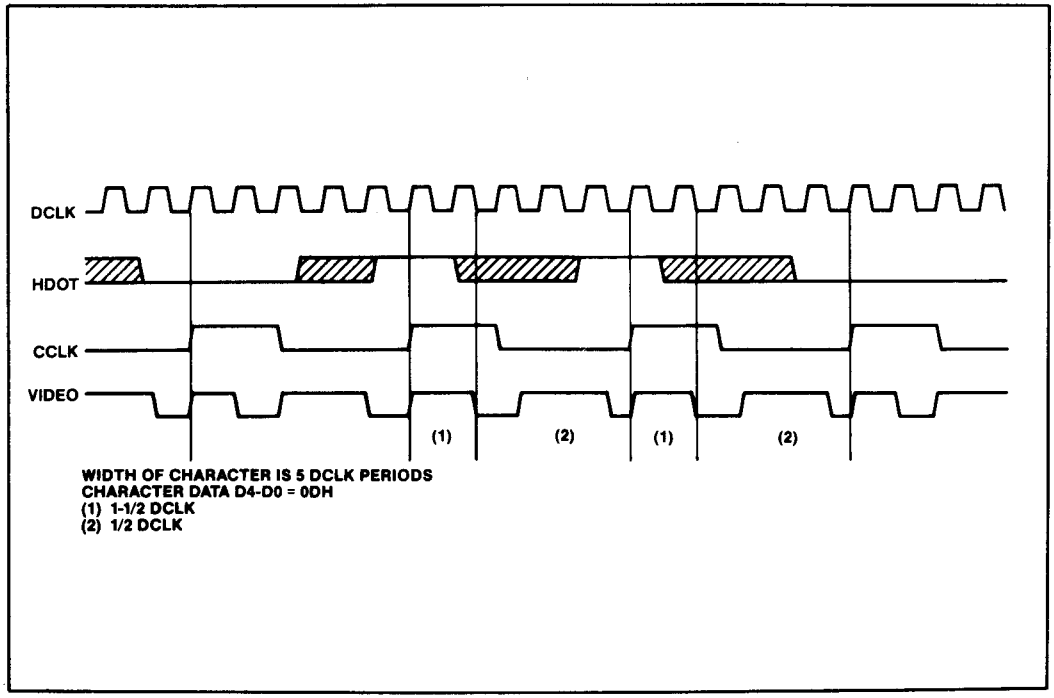


Figure 8. Function of HDOT on VIDEO

Character Reverse Video (CRVV)

CRVV is an active high signal. In the character field, the CRVV attribute will produce the effect of reversing the polarity of the display during the transmission of the current character. CRVV is also effective together with the CBLANK attribute (see CBLANK description) and the RRVV signal. Outside the character field, the CRVV attribute is ignored.

Although the CBLANK signal is normally a character attribute, it may change from dot line to dot line of a character. Thus one or more underlines or cursors can be generated by the CRT controller activating CBLANK and CRVV.

Double Width (DW)

The dot clock frequency and the CCLK frequency will be halved when the double width attribute is active (high), producing characters that are twice as wide. The period of RCLK is not changed (see Figure 9).

Width Defeat (WDEF)

The WDEF attribute signal is clocked into the SAB 82731 at the rising edge of CCLK. When the width defeat attribute is active (high), the width of CCLK will be set to a default width value previously programmed (see figure 10).

Field Attribute Signals

The field attribute signals are clocked into the 82731 with the rising edge of RCLK. Thus the attributes are valid for a specific part of the screen independent of how many characters are displayed within this part.

The 82731 supports two field attributes:

- field reverse video RRVV, and
- clock synchronization CSYN.

Row Reverse Video (RRVV)

RRVV control signal is clocked into the 82731 at the rising edge of RCLK. It immediately affects the display by the polarity of the video eoutput in both the character field and the border of the display. It is an active high signal.

Clock Synchronization (CSYN)

CSYN is a field attribute signal, because it defines the active character field in addition to its function of synchronizing CCLK and RCLK.

CSYN must be inactive (low) during the display of characters. At the first rising edge of RCLK after CSYN is deactivated (low), character data is latched into the 82731, beginning the display of the active character field (see Figure 11). At the next rising edge of RCLK after CSYN is activated (i.e. at the end of the character field), the video output is forced to zero or, if the RRVV control signal is active, to a high level. The currently transmitted character will be truncated at this location. At the same time, CCLK will be forced to match RCLK starting with the next rising edge of RCLK (see Figure 11). While CSYN is active all character attribute and data signals are ignored and only the field reverse video signal (RRVV) affects the video output.

Before the deactivation of CSYN, the data and attribute pipeline has to be filled by the CRT controller with the information of the first character.

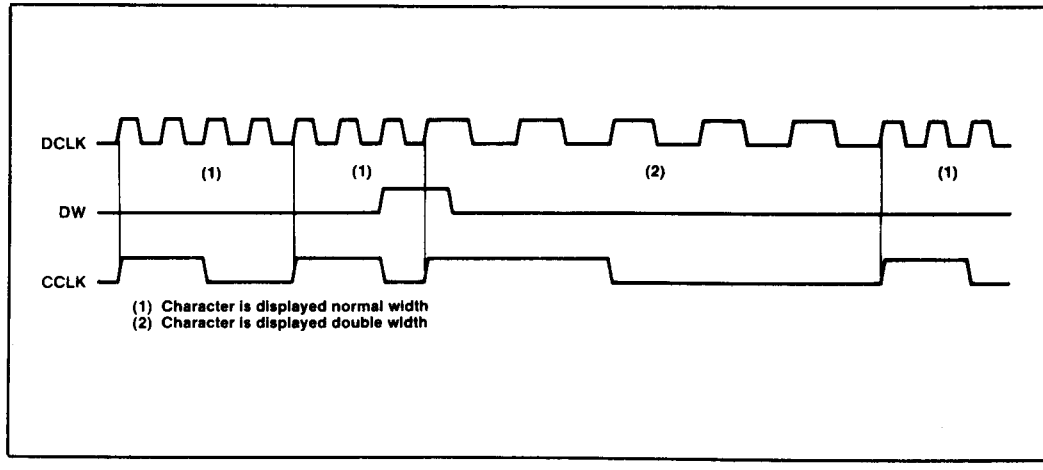


Figure 9. Function of DW on DCLK and CCLK

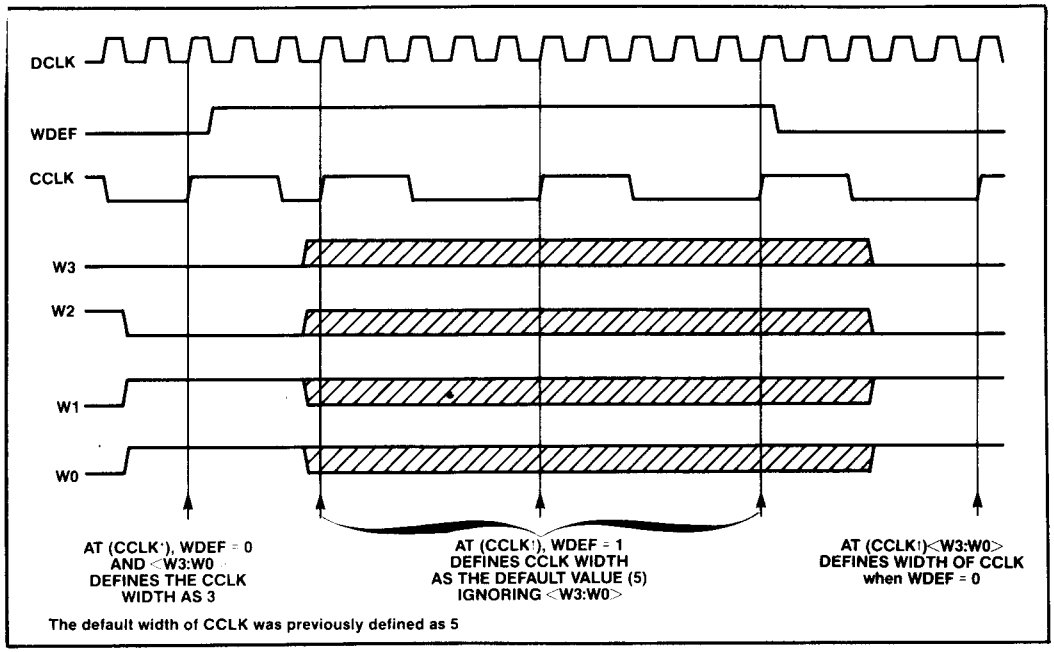


Figure 10. Function of WDEF

Tabulator Function

The 82731 supports tabulator functions by providing the CHOLD (character clock inhibit) input.

CCLK Inhibit ($\overline{\text{CHOLD}}$)

When the $\overline{\text{CHOLD}}$ signal is activated (low) it inhibits CCLK and thus freezes the information pipeline between CRT-controller and 82731 until the next tabulator location is reached. $\overline{\text{CHOLD}}$ Has to be activated simultaneously with the display of the TAB-character. If the TAB-character doesn't consist of all zeros, it must be blanked by activating CBLANK.

The width of the TAB-character can be determined by W0-W3 or by activating WDEF.

The $\overline{\text{CHOLD}}$ signal is provided by the 82730 and it is assumed to be triggered with the rising edge of CCLK (Figure 12). With the same edge of CCLK, the TAB-character will be latched into the 82731. Thus the TAB-character will be displayed completely and the CCLK will be inhibited until reaching the specified tabulator location, which is defined by $\overline{\text{CHOLD}}$ inactive (high) at the rising edge of RCLK.

In the timing diagrams it is assumed that $\overline{\text{CHOLD}}$ is deactivated by the falling edge of RCLK. Figure 12 shows the normal case where the display of the TAB-character is finished before deactivation of $\overline{\text{CHOLD}}$. The gap between the TAB- and the following character is normally blanked. In this scheme the TAB-character will be handled by the 82731 like each other character (attributes operate normally).

In case of $\overline{\text{CHOLD}}$ active width less than the TAB-character width the TAB-character will be also displayed completely. However, we have to distinguish three different cases:

1) TAB-character is terminated before reaching TAB-location. The next character will be displayed as described before. In the gap the video output is normally blanked.
2) TAB-character is finished exactly at the TAB-location. The next character will be displayed immediately without delay.
3) TAB-character is not terminated when reaching the TAB-location (see Figure 13). The following character will be displayed subsequently after the display of the TAB-character (i.e. the start of the following character is not at the TAB-location).

If the $\overline{\text{CHOLD}}$ signal is not deactivated the video output will be continuously blanked. In the gap between the end of the TAB-character and the TAB-location all character attribute signals will have no effect on the video output signal. If the RRVV control signal is active the video output signal is inverted.

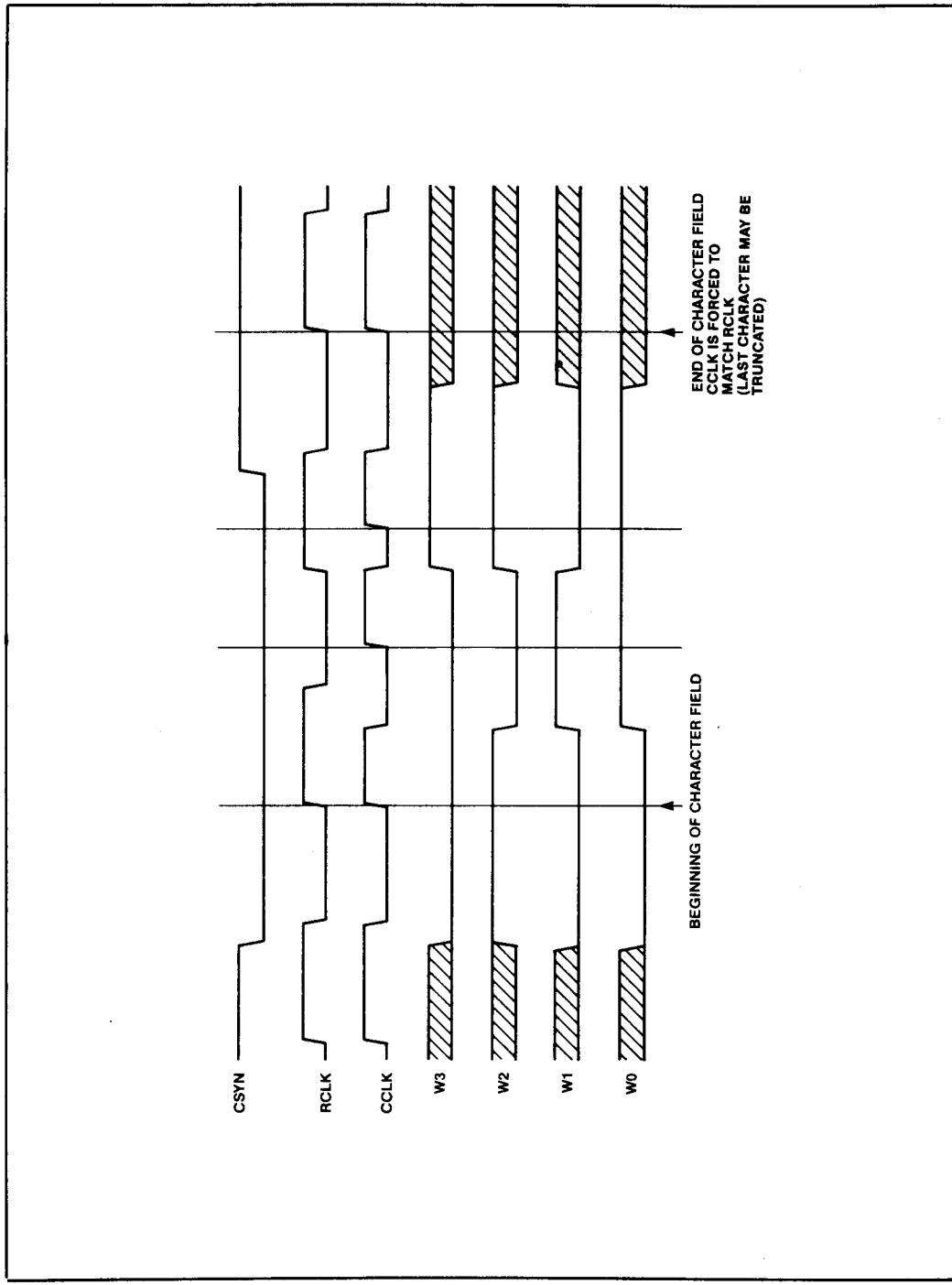
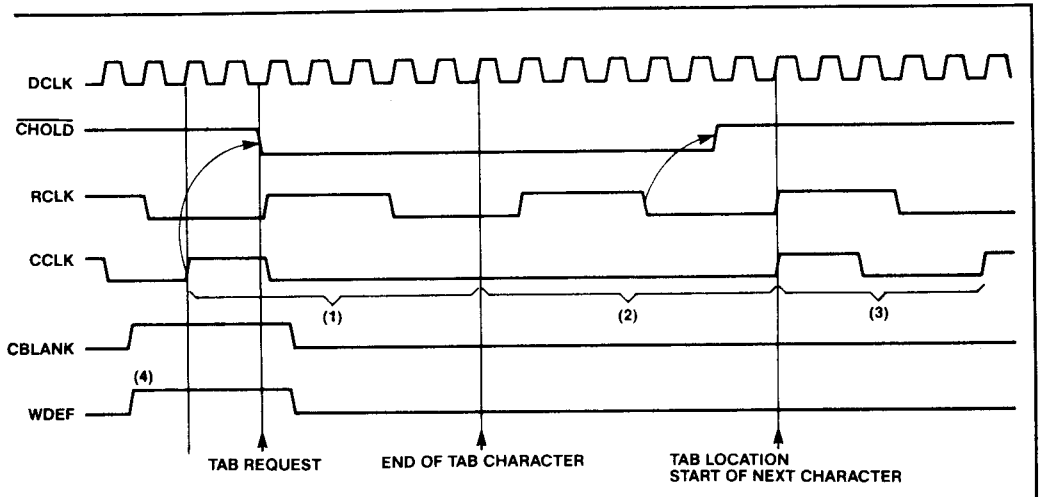
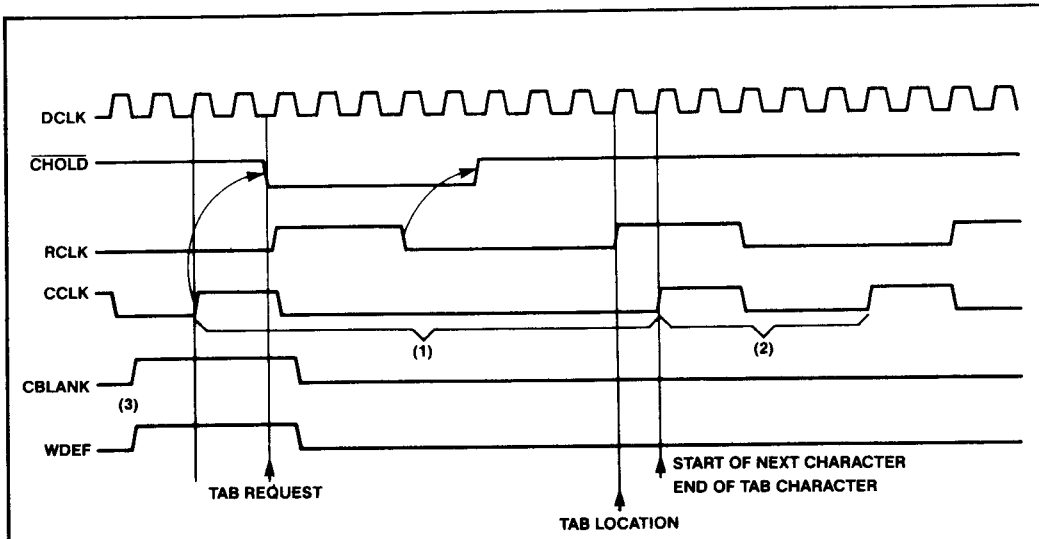


Figure 11. Function of CSYN



(1) TAB character is displayed completely - video output is blanked
(2) Video output is blanked
(3) Next character
(4) Default width: 7, TAB character width defined by WDEF

Figure 12. Function of CHOLD (Normal Case)



NOTE:
(1) TAB character is displayed completely - video output is blanked
(2) Next character is displayed (not on TAB location)
(4) Default width = 11.

Figure 13. Function of CHOLD with CHOLD Width Less than Character Width (Case 3)

Video Output

The video output provides an ECL-oriented signal (see Figure 14) and is matched to drive a 50 Ohm coax cable (see Figure 15). In case of external attribute processing the external logic can be EC or STTL-compatible.

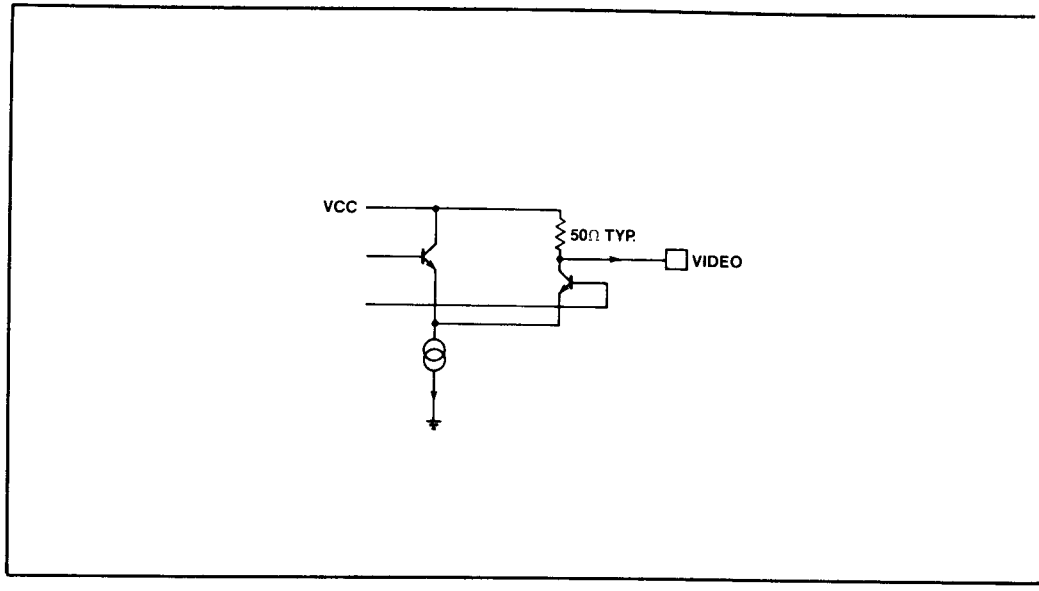


Figure 14. Video Output Stage

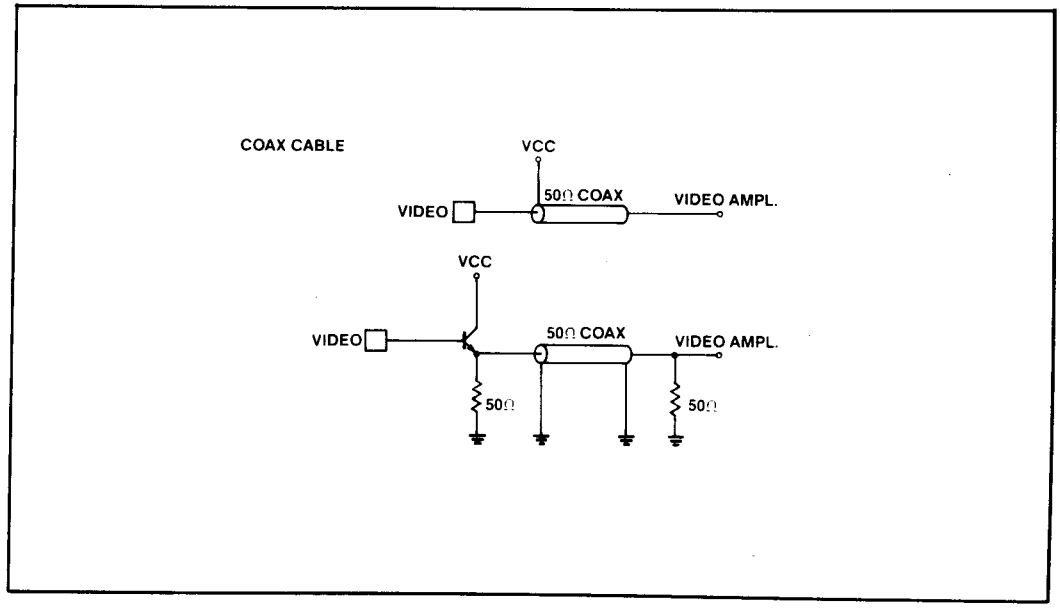


Figure 15. A Video Output Load

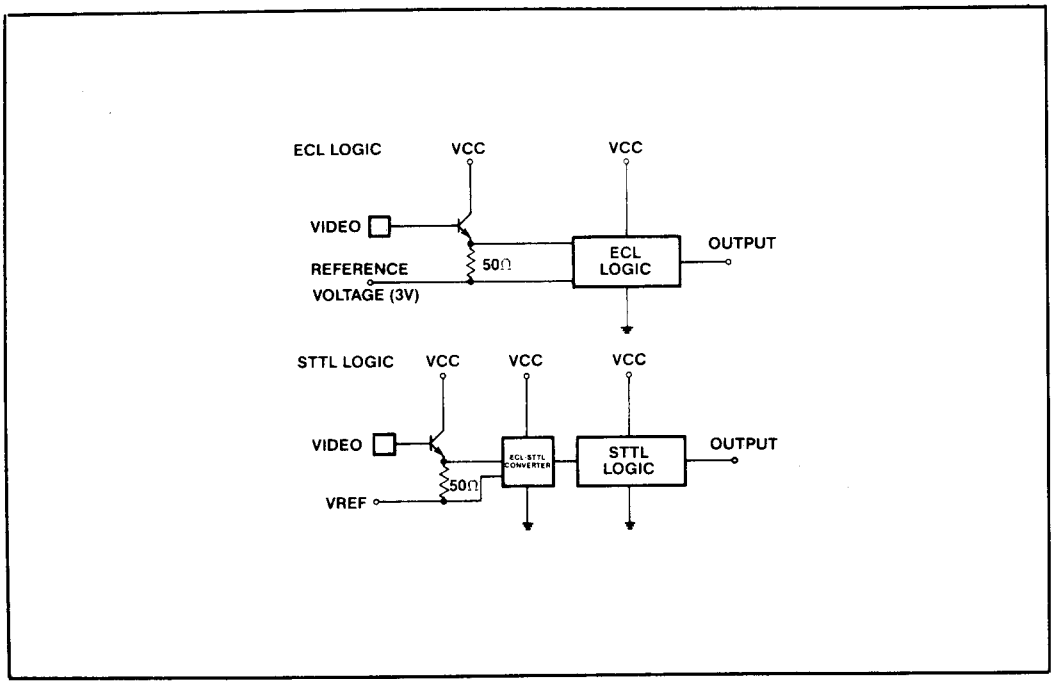


Figure 15.B Proposed Converter for Video Output to TTL Level Output

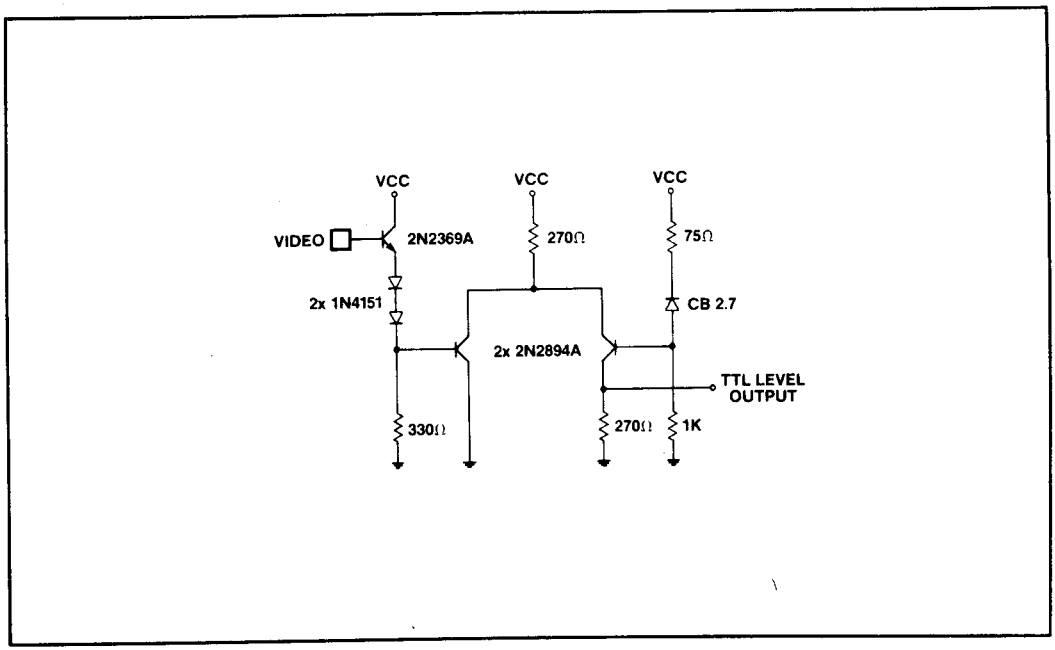


Figure 16. TTL-Level-Output Test Load

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +125°C
All Output and Supply Voltages ..... −0.5V to +6V
All Input Voltages ..... −0.6V to +5.5V
Power Dissipation ..... 1.75 Watt

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_A = 0°C$ to $70°C$)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_C	Input Clamp Voltage		−1	V	$I_C = -5$ mA
I_F	Forward Input Current		−0.7	mA	$V_F = 0.5V$
I_R	Reverse Input Current		50	μA	$V_R = V_{CC}$
V_{OL}	Output Low Voltage				
	CCLK		0.5	V	$I_{OL} = 8$ mA
	RCLK		0.5	V	$I_{OL} = 4$ mA
	VIDEO	$V_{CC} - 1.2V$	$V_{CC} - 0.6V$	—	$I_{OL} = 0$
V_{OH}	Output High Voltage				
	CCLK, RCLK	2.4		V	$I_{OH} = -400$ μA
	VIDEO	$V_{CC} - 0.2V$	V_{CC}	—	$I_{OH} = 0$
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0		V	
I_{CC}	Power Supply Current		300	mA	
Z_O	Output Impedance VIDEO	40	70	Ω	
C_{IN}	Input Capacitance		15	pF	$f_C = 1$ MHz

A.C. CHARACTERISTICS

T_A = 0 to 70° C; V_{CC} = 5V ± 10%. All timings measured at 1.5V unless otherwise noted.

Symbol	Parameter	Limit Values				Unit	Test Conditions
		82731		82731-2			
		Min.	Max.	Min.	Max.		
T_{DHDH}	DCLK cycle period	20	125	12.5	125	ns	-
T_{CHCH}	CCLK cycle period	3	18	3	18	T_{DHDH}	Fig. 17
T_{CLCH}	CCLK low time	T_{DHDH} − 10	16 T_{DHDH}	T_{DHDH} − 10	16 T_{DHDH}	ns	
T_{CHCL}	CCLK high time	2 T_{DHDH} − 5	-	2 T_{DHDH} − 5	-		
T_{RHRH}	RCLK cycle period	6	21	6	21	T_{DHDH}	
T_{RLRH}	RCLK low time	3 T_{DHDH} − 10	18 T_{DHDH}	3 T_{DHDH} − 10	18 T_{DHDH}	ns	
T_{RHRL}	RCLK high time	3 T_{DHDH} − 5	-	3 T_{DHDH} − 5	-		
T_{DRCH}	Data and attribute input set up time	25		20			-
T_{CHDX}	Data and attribute input hold time	0		0			
T_{HLTE}	$\overline{CHOLD}$ active before end of TAB-character	25		20			
T_{HLHH}	$\overline{CHOLD}$ pulse width						
T_{HHRH}	$\overline{CHOLD}$ inactive set up before rising edge of RCLK						
T_{HLRH}	$\overline{CHOLD}$ inactive hold time after rising edge of RCLK	0		0			
T_{CHVV}	Video output valid after rising edge of CCLK	-	10	-	6	ns	Video output measured at V_{CC} − 0.4V
T_{OLOH}	TTL-output rise time				10		Fig. 17
T_{OHOL}	TTL-output fall time						
T_{VLVH}	Video output rise time		5		3		Fig. 18
T_{VHVL}	Video output fall time						

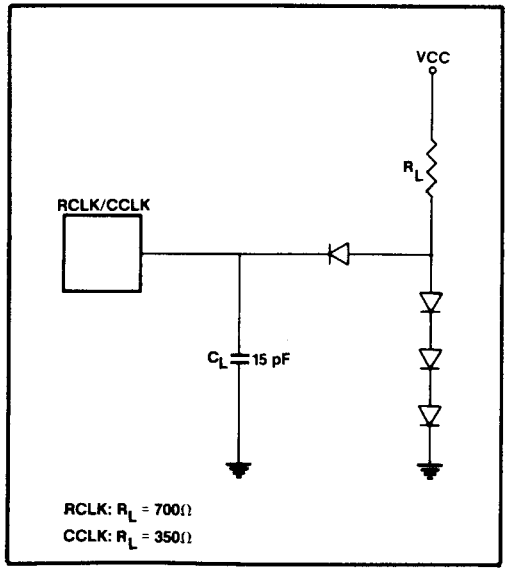


Figure 17. TTL-Level-Output Test Load

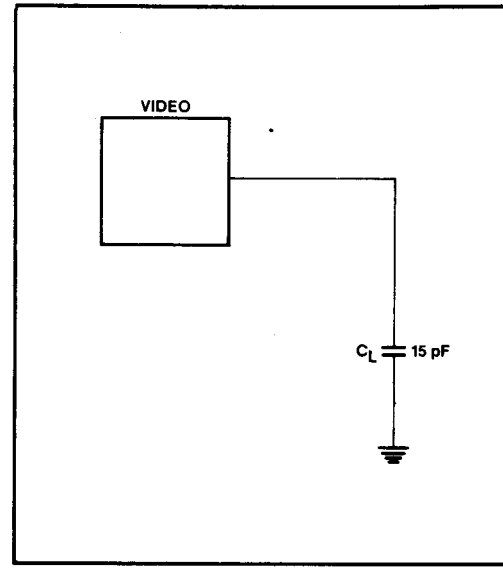


Figure 18. ECL-Level-Output Test

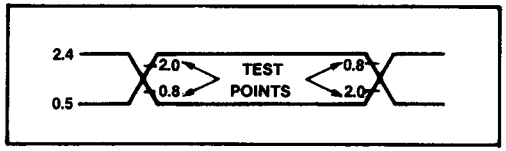


Figure 19. TTL-Level-Output Load Circuit

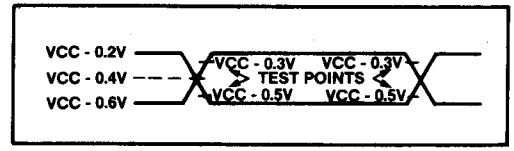


Figure 20. ECL-Level-Output Load Circuit

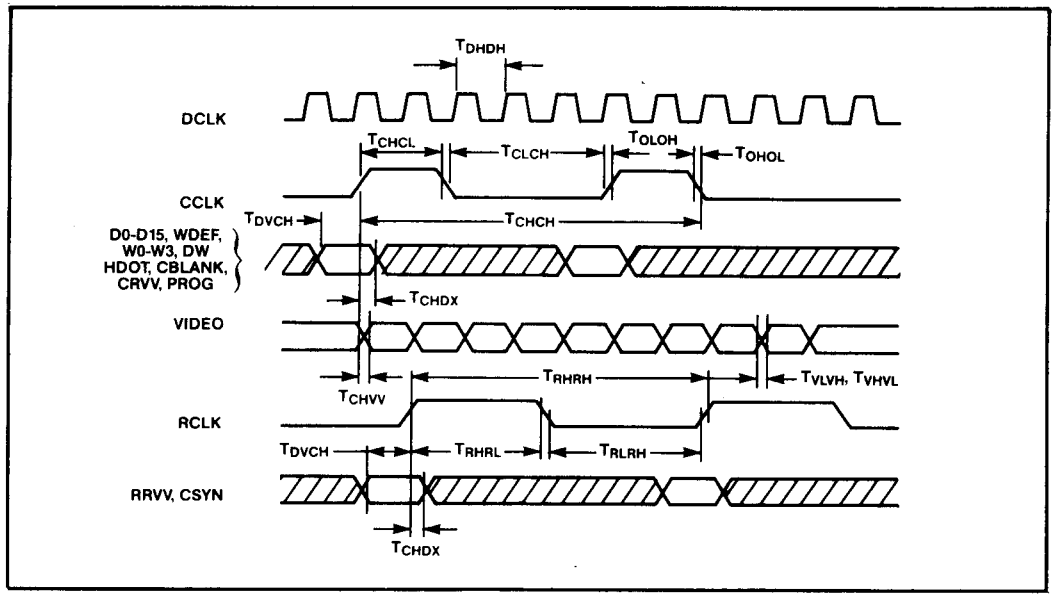


Figure 21. Basic Timing

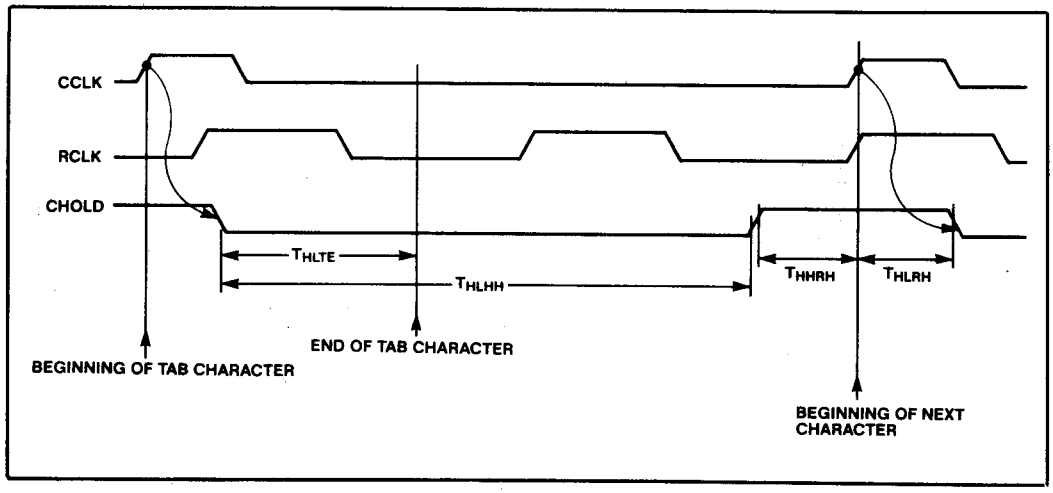


Figure 22. Timing on CHOLD

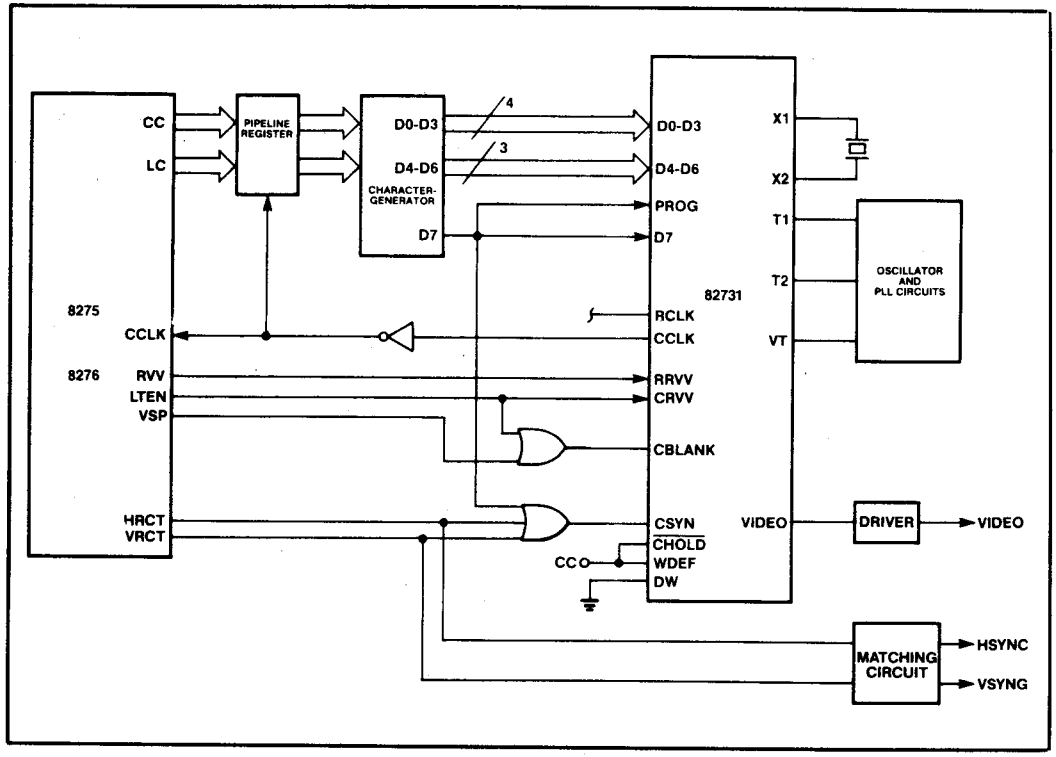


Figure 23. Example Interface to 8275