CHIPS PRELIMINARY

82C550A
STARLAN SERIAL INTERFACE

- 100% Compatible with the IEEE 802.3 STARLAN Specifications
- Supports 1 Mbps Bus Implementations
- Fully Compatible with the Intel™ 82586 LAN Coprocessor serial interface
- 1 Mbps Operation
- Manchester Encoding and Decoding and Receive Clock Recovery
- On-chip Collision Detector
- Noise Filter for Receive and Collision Inputs
- Generates Carrier Sense signal to indicate network activity
- Option of TTL or RS422/RS485 level driver/receiver at the cable interface
- External Slew-Rate-Cable-Control signal provided for differential outputs
- Tolerates up to ±90ns jitter on receive data
- Diagnostic Loopback for fault detection and isolation
- 30 ms Watchdog Timer
- Low Power CMOS implementation

The 82C550A STARLAN Serial Interface is a single chip Manchester Encoder/Decoder with an on-chip transceiver, designed to perform the serial interface functions for the IEEE 802.3 STARLAN networks. The 82C550A performs Manchester encoding on the transmit data and decodes the Manchester encoded receive data into NRZ format. The chip detects any Manchester Bit Code Violation on the receive data, and generates collision signal. It also generates collision under various other conditions described later. The chip can transmit and receive TTL level signals. In the extended mode, an RS422/RS485 transceiver option is also provided on the chip. This transceiver can be used as an alternate to the TTL levels on the transmit output and receive input. The chip is designed to interface directly with the Intel 82586 LAN Coprocessor. It can also be used with other data link controllers available for Local Area Networks.

The 82C550A is implemented using CMOS process technology, and is packaged in a 20-pin Plastic DIP.

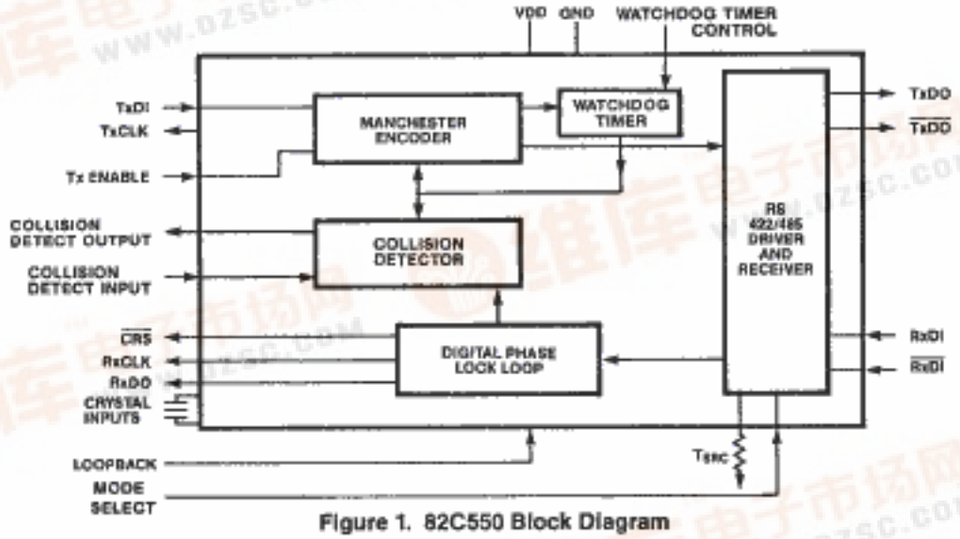
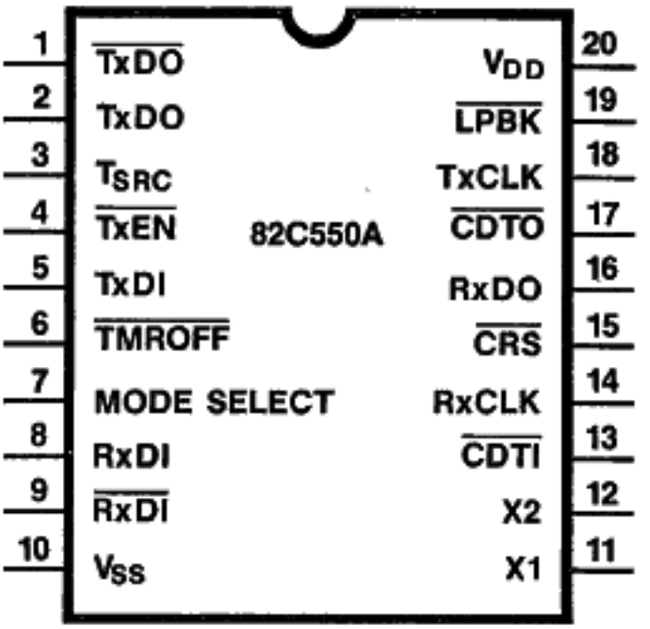


Figure 1. 82C550 Block Diagram

Printed in USA 5M 1/87 Rev 1

PIN DIAGRAM


1 TxDO
2 TxDO
3 TSRC
4 TxEN
5 TxDI
6 TMROFF
7 MODE SELECT
8 RxDI
9 RxDI
10 VSS
82C550A
20 VDD
19 LPBK
18 TxCLK
17 CDTO
16 RxDO
15 CRS
14 RxCLK
13 CDTI
12 X2
11 X1

82C550A Pin Description

Pin No.	Pin Type	Symbol	Description
1,2	O	$\overline{\text{TxDO}}$, TxDO	Transmit Data Output. In normal mode a TTL level signal is output on TxDO pin and $\overline{\text{TxDO}}$ is the tri-state control signal for the off-chip driver. In Expanded Mode, TxDO in conjunction with the $\overline{\text{TxDO}}$ output provides the differential output from the on-chip transceiver.
3	I	Tsrc	Slew Rate Control Input. An external resistor on this input determines the rise and fall rates on the TxDO and $\overline{\text{TxDO}}$ output pair in the Expanded Mode.
4	I	$\overline{\text{TxEN}}$	Transmit Enable is an active low input signal. It is used to signal the 82C550 to start encoding the data on TxDI input and transmit it on the TxDO and $\overline{\text{TxDO}}$ pair.
5	I	TxDI	Transmit Data Input is the NRZ data input from the controller. The data on this input is encoded and transmitted as Manchester encoded data on the TxDO and $\overline{\text{TxDO}}$ pair.
6	I	$\overline{\text{TMROFF}}$	Timer Off is an active low input. It is used to disable the "Watchdog" Timer on the chip. This capability is useful in running diagnostic tests on the system, where the user may want to send frames longer than 30 ms in time duration.
7	I	Mode Select	Mode Select input is used to select the transceiver option on the chip. When high, the Normal Mode is selected and TTL level data is output on the TxDO pin. When low, Expanded Mode with the on-chip transceiver is selected. In the Expanded Mode, the differential data is output on the TxDO and $\overline{\text{TxDO}}$ pair.
8,9	I	RxDI $\overline{\text{RxDI}}$	Receive Input data are the input pins for the Manchester encoded data. In the Normal Mode, RxDI is the encoded receive data signal used by the DPLL to recover the data and clock. $\overline{\text{RxDI}}$ is the output from the Offset receiver which is used for carrier Sense detection. In the Expanded Mode, the differential data is input on RxDI and $\overline{\text{RxDI}}$ input pair. Like the Normal Mode, the data is decoded into NRZ format and output on the RxDO pin.
10	I	V_{SS}	Power Supply Ground.

82C550A Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
11, 12	I/O	X1, X2	Crystal Oscillator input. A fundamental frequency parallel resonant crystal should be connected to this pair. Alternatively, a TTL signal may be connected to the X1 input. The clock frequency should be 16 MHz.
13	I	$\overline{CDTI}$	Collision Detect Input is used for detecting externally detected collisions. This input is useful in Bus implementations, where an external Collision Detect circuit generates a Collision signal based upon energy level on the wire. When not used, this input should be tied high.
14	O	RxCLK	Receive Clock is the clock output recovered from the received data on the RxDI input. During the beginning of a frame reception, the RxCLK output is held low for 8-bit period. During this period the Digital Phase Lock Loop on the chip is in the process of acquiring a lock onto the receive data. During idle condition, the RxCLK output is a free running clock, operating at 1/16th the crystal frequency.
15	O	$\overline{CRS}$	Carrier Sense is an active low output. It is activated at the beginning of a frame reception and is deactivated at the end of a frame reception.
16	O	RxDO	Receive Data Output is the decoded receive data output. The Manchester encoded data received on the RxDI input is decoded into NRZ and output on the RxDO output. At the beginning of a frame reception, the RxDO is held high for a period of 8-bits. During this time the Digital Phase Lock Loop is acquiring a lock on to the received data. This output is held high during the idle state.
17	O	$\overline{CDTO}$	Collision Detector Output is an active low output signal. When active, it indicates that two or more stations are active at the same time. This signal is also activated under several other conditions, which are described later in this data book.
18	O	TxCLK	Transmit Clock Output is the transmit clock for the controller. It operates at 1/16th the crystal frequency on the X1, X2 inputs.
19	O	$\overline{LPBK}$	Loopback is an active low input. When active it will put the device into a local loopback mode. In normal operation $\overline{LPBK}$ should be pulled high.
20	I	V_{DD}	Power Supply.

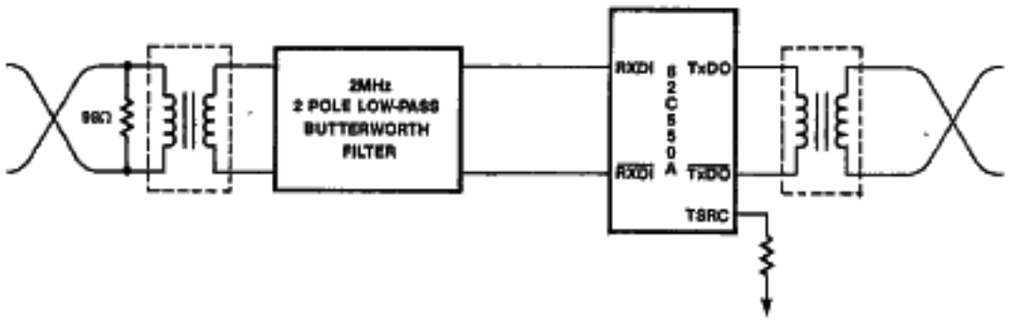


Figure 2. Typical Expanded Mode Configuration

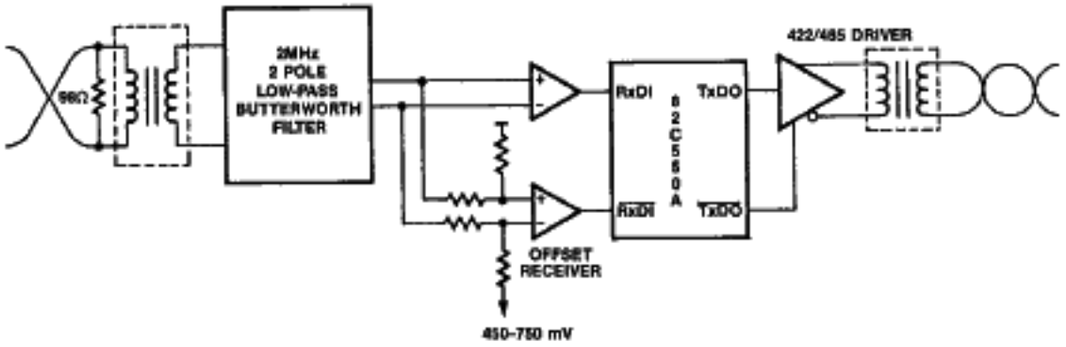


Figure 3. Typical Normal Mode Configuration

Functional Description

The 82C550A Manchester Encoder/Decoder chip is designed to be used with 1 Mbps IEEE 802.3 compatible STARLAN networks. The device performs Manchester encoding on the transmit data, and decodes the Manchester encoded receive data into NRZ format. A complete Collision Detection is also performed on the receive data by detecting the STARLAN specific collision pattern, and activating the Collision Detection $\overline{CDTO}$ output.

The 82C550A features an on-chip transceiver. The transceiver is compatible with the RS422/RS485 and the STARLAN specifications. The signals on the communication channel are also available in TTL levels. The user can select either of the two signal levels through the Mode Select pin.

The 82C550A provides the transmit clock for the data link controller. It uses a Digital Phase Locked Loop to generate a receive clock which is synchronized to the receive NRZ data. On-chip Loopback capability allows the user to loopback the transmit data to the receive data, thus allowing a quick isolation and diagnosis of a network fault.

The 82C550A is designed to interface directly with the Intel LAN coprocessor 82586. It can also be used with other popular data link controllers.

Modes of Operation

The 82C550A is designed to be used either with or without the transceiver on the channel interface. The two modes are selected by the polarity of the Mode Select input.

Mode Select	Mode
1	Normal Mode with TTL input/output levels.
0	Expanded Mode with the on-chip transceiver.

In the Expanded Mode, an external resistor is used to selectively control the slew rate of the output waveform on the transmit output pair.

The 82C550A consists of various logical sections. Following is a description of these sections:

Transmit

The transmit section includes the oscillator and the Manchester encoder. The oscillator can be driven either by an external level clock source or by a parallel resonant fundamental mode crystal. The clock frequency in both cases is fixed at 16 MHz. From this 16 MHz clock generator, a 1 MHz clock is generated as the basic frequency for the transmit clock. The encoder circuit takes in the transmit data from the controller and converts it into Manchester-format for serial transmission. The duration of a bit cell is 1 μs for 1 Mbps system. The first half of each bit cell contains the complementary data and the second half contains the true data. Therefore, there is always a transition at the center of the bit cell and may or may not have a transition at the cell boundary.

In the Normal Mode, during idle period, the TxDO is forced into a high state. The transmission starts two bits after the $\overline{TxEN}$ is asserted. *This feature will prevent the first two bits generated by the 82586 from being transmitted.* The transmission terminates when $\overline{TxEN}$ goes inactive. The last high going transition may be at the bit cell center if the last bit is a "1", or it may be at the bit cell boundary if the last transmitted bit is a "0". A tri-state control output is provided on the chip to enable and disable the external line driver connected to the transmit data output, TxDO. The tri-state control signal is the $\overline{TxDO}$ output. This output becomes active 2.2-2.8 bit times after the last low to high transition on the transmit data output.

In the Expanded Mode with the transceiver included, the transmit output pair TxDO and $\overline{TxDO}$ are tri-stated at the end of transmission within 2.2-2.8 bit times after the last low to high transition on the transmitted data output. Also, the rate of the rise and fall times in the TxDO and $\overline{TxDO}$ outputs are controlled by the Tsrc Transmit Slew Rate Control input, Tsrc. Table 1 shows the resistor values and

the corresponding rise/fall times which can be selected.

Resistor at Tsrc in Ohms	Rise/Fall Time
0	15 ns
2.5 K	25 ns
5 K	40 ns
7.5 K	55 ns
10 K	70 ns
15 K	100 ns
20 K	140 ns

Table 1

Watchdog Timer

The chip features a 30 ms watchdog timer to prevent transmissions which are longer than 30 ms in duration. The watchdog timer can be enabled or disabled using the $\overline{\text{TMROFF}}$ pin. When enabled, the watchdog timer starts counting at the beginning of a frame transmission. If a transmission terminates before the timer expires (30 ms), the timer resets itself and gets started at the beginning of the next transmission. In case the transmission continues for longer than 30 ms, than the transmission is aborted and the Collision Detect output $\overline{\text{CDTO}}$ is asserted. The $\overline{\text{CDTO}}$ will be kept asserted until the transmission enable $\overline{\text{TXEN}}$ remains asserted. $\overline{\text{CDTO}}$ will become inactive after the $\overline{\text{TXEN}}$ becomes inactive. The Watchdog timer when enabled, is active both in normal transmission and Loopback modes.

Receive

The primary function of the receive section of the 82C550A is to receive the data from the serial link and separate the data from the clock. This function is achieved by using the digital phase locked loop (DPLL) technique. Under normal reception, the frame starts with the input RxDI going negative. The Carrier Sense becomes active on detecting a transition on the RxDI input. Once the carrier sense $\overline{\text{CRS}}$ becomes active, the DPLL starts the acquisition process. The DPLL uses the first 8 bits to acquire lock . Once the loop is locked, the circuit generates a window around the bit center for data sampling. Due to the nature of the Manchester format, the data sampled *before* the bit center will be different from the data sampled *after* the bit center. The sampling scheme is used to detect any missing transition at the bit center. A missing transition in the bit center is reported as a Collision condition.

The Carrier Sense output $\overline{\text{CRS}}$ indicates to the controller that there have been transitions on the cable. To prevent any false indication, 82C550A provides a noise rejection filter for carrier sense detection. A minimum of two low going transitions (within a period of 3 microseconds) on the receive data input will turn on the Carrier Sense output. Once the Carrier Sense is turned on, it will remain active until no more activity is detected on the receive data input. In the transmit mode, once the Carrier Sense is turned on, it will remain active until the $\overline{\text{TXEN}}$ signal becomes in-active and there are no more transitions on the receive data input. This scheme will eliminate the possibility of signal cancellation in *Multi-Point Extension* applications. At the end of the frame reception, the $\overline{\text{CRS}}$ is de-asserted and will remain inactive (high) for a minimum period of 21 bit periods between two consecutive back-to-back frame receptions. This is also defined as the *blinding period* and is used to mask out the under shoot caused by transformer at the end of transmission.

Squelch Circuit

The receive data input features a squelch circuit to prevent cable noise and cross-talk from turning on the $\overline{\text{CRS}}$ inadvertantly. The squelch is enforced in the Expanded Mode only, with the on-chip transceiver. A squelch circuit of 450 mV to 750 mV offset voltage is provided at the receive input. In the Normal Mode, an external squelch circuit should be used. Also, in both Extended and Normal modes, in addition to the squelch circuit, it is also recommended that a 2 MHz 2-pole low pass filter butterworth filter is implemented externally.

Collision Detector

The 82C550A detects and generates a Collision output, $\overline{CDTO}$ under several conditions. The conditions under which a Collision Signal is activated are as follows:

i Manchester Code Violation:

The receive data has a missing transition in the center of the bit, which construes a Manchester Code Violation.

ii Starlan Specific Collision Pattern is Detected:

Whenever a Starlan specific Collision Pattern, CP, is received at the receive data inputs, the Collision Detect Output, $\overline{CDTO}$ is asserted.

iii AT & T Release 1 Collision Presence:

Some earlier versions of Starlan products from AT & T generated a 2/3 MHz signal to indicate a Collision Condition. The 82C550A will detect this pattern and assert the $\overline{CDTO}$ output.

iv Carrier Drop during Transmission:

If Carrier signals becomes active during transmission, and then becomes inactive, a Collision signal is generated; $\overline{CDTO}$ will be asserted.

v External Collision:
If the external collision input, $\overline{CDTI}$ becomes active for at least 24 ns during $\overline{CRS}$ active period, $\overline{CDTO}$ will be asserted.

vi Watchdog Timer:

If Watchdog timer times out before the transmission is completed, the Collision output, $\overline{CDTO}$ will be asserted. $\overline{CDTO}$ will remain active until $\overline{TXEN}$ Transmit Enable becomes inactive.

vii Absence of Echo:

If no Carrier signal is detected within 280 bit times after the transmission is started ($\overline{TXEN}$ Transmit Enable becomes active), $\overline{CDTO}$ will be activated.

viii Pulse Width Too Short or Too Long:

If Pulse Width of the Incoming Receive data is shorter than 3/16 bit period, or longer than 21/16 bit period, Collision Detect $\overline{CDTO}$ output will be generated.

ix Heartbeat Signal:

In loopback mode at the end of transmission, the Collision Detect signal $\overline{CDTO}$ will be asserted for a period of 5-13 bit times.

Loopback Mode

The 82C550A features a loopback capability on the chip. When the Loopback pin $\overline{LPBK}$ is activated, the transmit data is routed back into the receive section. During loopback, the output buffer on the transmit section and the input buffer on the receive section are disabled. The Manchester encoded data from the transmit section is routed to the decoder of the receive section. This scheme is designed to help in isolating and identifying any system level problems. In the loopback mode, a simulated collision detect signal (Heartbeat Signal) is generated at the end of the attempted transmission frame. The Collision Detect signal can be used by some data link controllers, like the Intel 82586, to verify that the Collision Detect circuit of the 82C550A is working correctly.

82C550A Absolute Maximum Ratings

Parameter	Sym	Min.	Max.	Units
Supply Voltage	V_{DD}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	°C
Storage Temperature	T_{stg}	-40	125	°C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C550A Operating Conditions

Parameter	Sym	Min.	Max.	Units
Supply Voltage	V_{DD}	4.75	5.25	V
Ambient Temperature	T_A	0	70	°C

82C550A DC Characteristics

Sym	Parameter	Min.	Max.	Units
I_{IL}	Input leakage current $0 < V_{IN} < V_{DD}$		10	μA
I_{CC}	Supply Current		80	mA
V_{IL}	Input low voltage	-0.3	0.8	V
V_{IH1}	Input high voltage (except X1 input)	2.0	V_{DD}	V
V_{IH2}	X1 input high voltage	3.5	V_{DD}	V
V_{OL1}	Output low voltage (except TxCLK) @ I_{OL} = 2.1 mA		0.4	V
V_{OL2}	TxCLK output low voltage @ I_{OL} = 4.2 mA		0.4	V
V_{OH1}	Output high voltage @ I_{OH} = -400±μA	2.4		V
V_{OH2}	Output high voltage @ I_{OH} = -400±μA (Note 1)	3.9		V
V_{DIFO}	Differential output voltage in the Expanded Mode on the TxDO and $\overline{\text{TxDO}}$ input pair. Cable impedance = 80 -115 Ohms	2.1	3.5	V
V_{CMS}	Expanded Mode Common Mode Swing Voltage at RxDI and $\overline{\text{RxDI}}$ input pair		±2	V
V_{DIF}	Expanded Mode Differential Voltage at RxDI and $\overline{\text{RxDI}}$ input pair	1.1		V
V_{SQ}	Differential Input Squelch Voltage	0.45	0.75	V
V_{BKSV}	TxDO, $\overline{\text{TxDO}}$ Back Swing Voltage at 20-bit time after idle		0.4	V
C_{IN}	Input Capacitance @ fc = 1 MHz		15	pF
C_{OUT}	Output Capacitance @ fc = 1 MHz		15	pF
Z_{DIFI}	Differential Impedance on RxDI, $\overline{\text{RxDI}}$ pair in Expanded Mode	25	50	K-Ohms

NOTE: 1. RxCLK, TxCLK and RxDO outputs only.

82C550A AC Characteristics
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	Min.	Typ.	Max.	Units
Transmit timing in Normal mode					
t1	Input clock cycle time	62.49375	62.5	62.50625	ns
t2	Input clock rise time			10	ns
t3	Input clock fall time			10	ns
t4	Input clock high time	20			ns
t5	Input clock low time	20			ns
t6	TxCLK cycle time		16×t1		ns
t7	TxCLK rise time			10	ns
t8	TxCLK fall time			10	ns
t9	TxCLK high time	8×t1-30		8×t1+30	ns
t10	TxCLK low time	8×t1-30		8×t1+30	ns
t11	$\overline{\text{TxEN}}$ Setup time	50			ns
t12	$\overline{\text{TxEN}}$ Hold time	0			ns
t13	TxDI Setup time	50			ns
t14	TxDO Hold time	0			ns
t15	TxDO bit cell duration	16×t1-5	16×t1	16×t1+5	ns
t16	TxDO bit cell center to bit cell boundary	8×t1-5	8×t1	8xt1+5	ns
t17	TxDO transition fall time (normal mode)			10	ns
t18	TxDO transition rise time (normal mode)			10	ns
t19	Normal Mode tri-state control delay from the first TxDO transition	0		10	ns
t20	Normal Mode tri-state control delay from the last low to high transition on TxDO	2.2		2.8	µs
t20A	Expanded Mode TxDO stay high before becoming tri-stated	2.2		2.8	µs
Receive timing					
t21	RxCLK cycle time	16×t1-85		16×t1+85	ns
t22	RxCLK rise time			5	ns
t23	RxCLK fall time			5	ns
t24	RxCLK high time	6×t1-20		10×t1+20	ns
t25	RxCLK low time	6×t1-20		10×t1+20	ns
t26	Time RxCLK held low at the beginning of a received frame	5×t21	6×t21	7×t21	ns

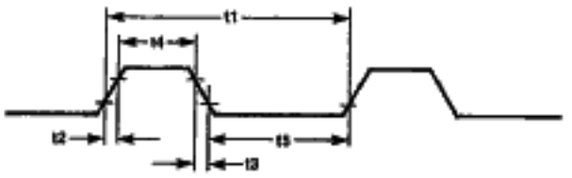
82C550A AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	Min.	Typ.	Max.	Units
Receive timing (Continued)					
t27	RxDI rise time			20	ns
t28	RxDI fall time			20	ns
t29	Maximum jitter at the input data			±90	ns
t30	$\overline{CRS}$ activated from the first valid RxDI transition			3×t21	ns
t31	RxDO rise time			10	ns
t32	RxDO fall time			10	ns
t33	RxDO delay time	−10		30	ns
t34	Time from last transition of RxDI to de-assertion of $\overline{CRS}$	1.5×t21		3×t21	ns
t35	$\overline{CRS}$ Assertion or De-assertion time delay	10		40	ns
t36	RxDI, $\overline{RxDI}$ return to zero from last positive going transition	1.7			µs
Loopback Timing					
t37	$\overline{LPBK}$ active set-up time before the actual frame starts	100			ns
t38	$\overline{CDTO}$ active from $\overline{TxEN}$ inactive	3×t21		11×t21	ns
t39	Duration of $\overline{CDTO}$ active	5×t21		13×t21	ns
t40	$\overline{CRS}$ disable time after inactive (both loopback and normal modes)	21×t21	22×t21	23×t21	ns

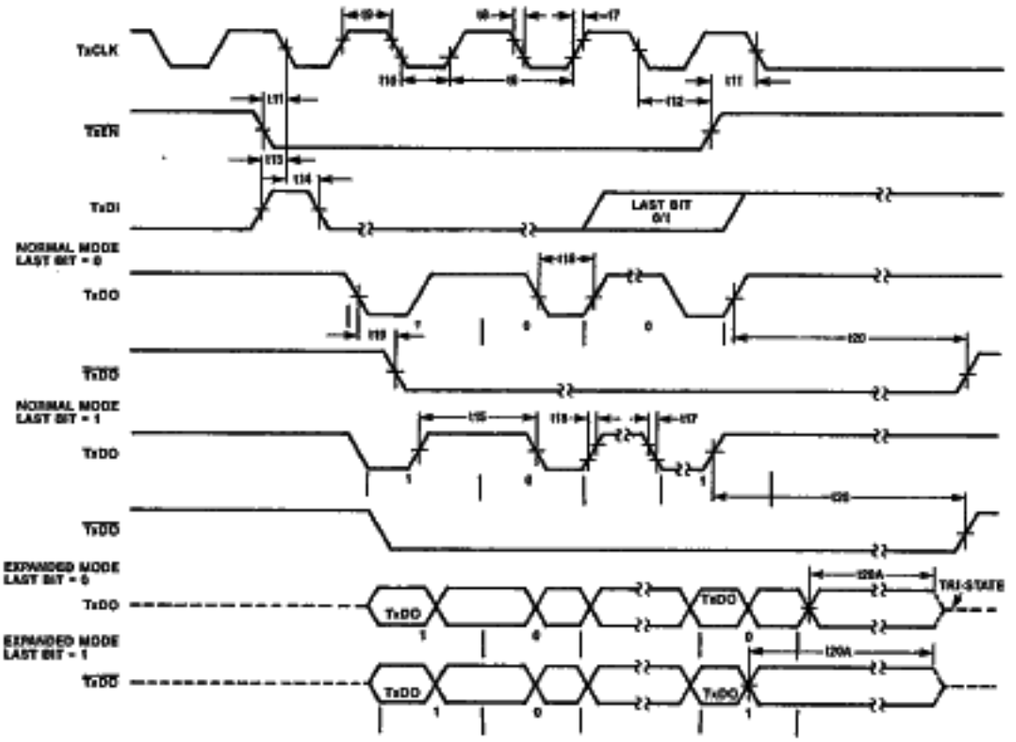
NOTES:

1. AC measurements are done at: TTL output: High level = 2.0 V Low level= 0.8 V
   Input swing is at least 0.4 V to 2.4 V with 3–10 ns rise and fall times.
   The rise and fall times are measured between 0.6V and 3.0V.
   For RCLK, X1, TxCLK and RxDO:
   High time is measured at 3.0V
   Low time is measured at 0.6V
2. AC load for all outputs is 30 pf to ground.
3. If X1 input is driven with an external clock source, the TTL waveform should meet the timing specifications t1, t2, t3, t4, and t5.

CLOCK

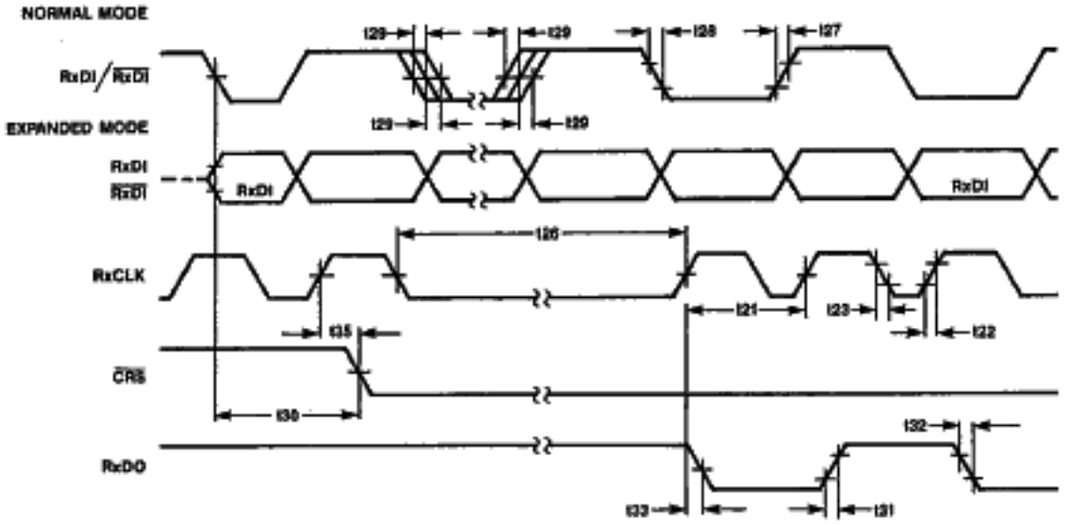


TRANSMIT TIMING

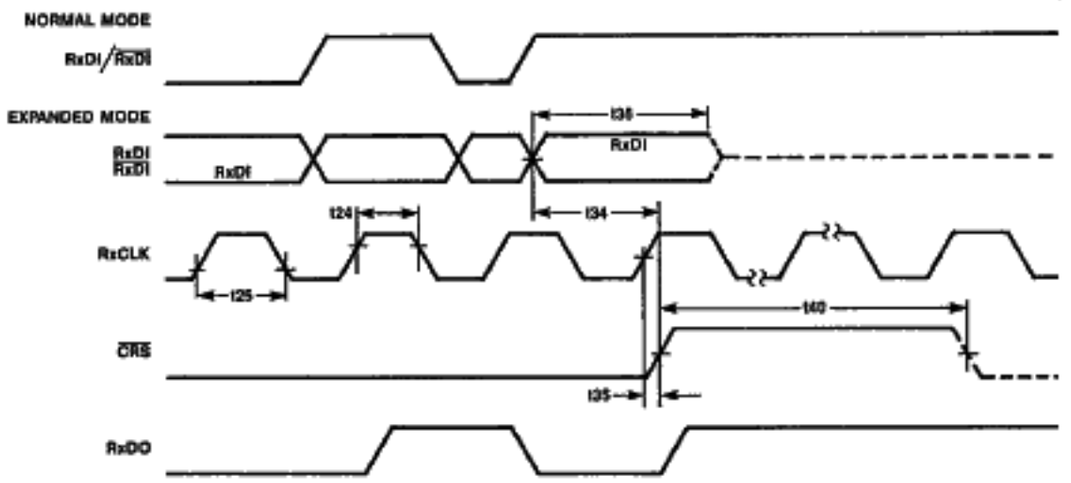


CHIPS

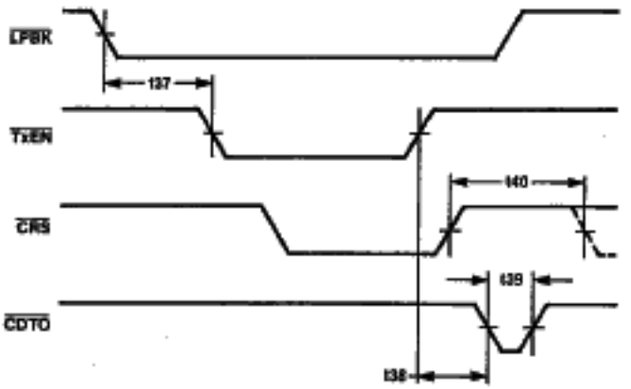
RECEIVE TIMING — START OF FRAME



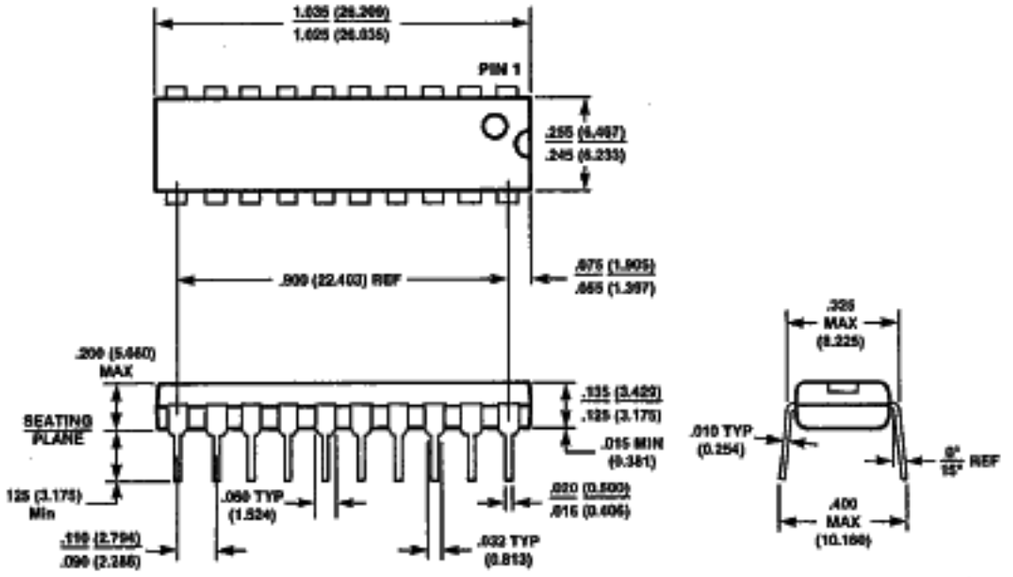
RECEIVE TIMING — END OF FRAME



LOOPBACK TIMING



20-PIN PDIP MECHANICAL SPECIFICATIONS



DIMENSIONS IN INCHES (mm)

Crystal Specification

The crystal required in the X1, X2 inputs should meet the following requirements.

Resonant Frequency
(CL = 20 pF) ..... 16 MHz
Type ..... Fundamental Mode
Circuit ..... Parallel Resonance
Load Capacitance (CL) ..... 20 pF
Shunt Capacitance (CO) ..... 7 pF Max.

Equivalent
Series Resistance (R1) .... 25 Ohm Max.
Motional Capacitance (C1) ... 0.02 pF Max.
Drive Level ..... 2 mW
Accuracy .... at 16 MHz ±0.002% at 25° C
.. at 16 Mhz ±0.005% for 0-70° C

Also, instead of the crystal at the X1, X2 inputs, an alternate TTL input may be connected at X1 input and floating X2.

Ordering Information

Order Number	Package Type	Operating Range
P82C550A	PDIP-20	C (Note 1)

Notes:
1. PDIP-20 Plastic Dual-in-Line 20 pin package
. C = Commercial Range, 0-70°C, ±5% Supply Voltage