intersil

82C84A

March 1997

CMOS Clock Generator Driver

Features

- Generates the System Clock For CMOS or NMOS Microprocessors
- Up to 25MHz Operation
- Uses a Parallel Mode Crystal Circuit or External Frequency Source
- Provides Ready Synchronization
- Generates System Reset Output From Schmitt Trigger Input
- TTL Compatible Inputs/Outputs
- Very Low Power Consumption
- Single 5V Power Supply
- Operating Temperature Ranges
  - C82C84A . . . . . .0^oC to $+70^oC$
  - I82C84A . . . . . -40^oC to $+85^oC$
  - M82C84A . . . . . -55^oC to $+125^oC$

Description

The Intersil 82C84A is a high performance CMOS Clock Generator-driver which is designed to service the requirements of both CMOS and NMOS microprocessors such as the 80C86, 80C88, 8086 and the 8088. The chip contains a crystal controlled oscillator, a divide-by-three counter and complete “Ready” synchronization and reset logic.

Static CMOS circuit design permits operation with an external frequency source from DC to 25MHz. Crystal controlled operation to 25MHz is guaranteed with the use of a parallel, fundamental mode crystal and two small load capacitors.

All inputs (except X1 and $\overline{RES}$) are TTL compatible over temperature and voltage ranges.

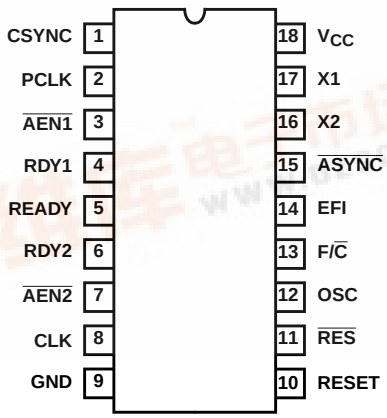
Power consumption is a fraction of that of the equivalent bipolar circuits. This speed-power characteristic of CMOS permits the designer to custom tailor his system design with respect to power and/or speed requirements.

Ordering Information

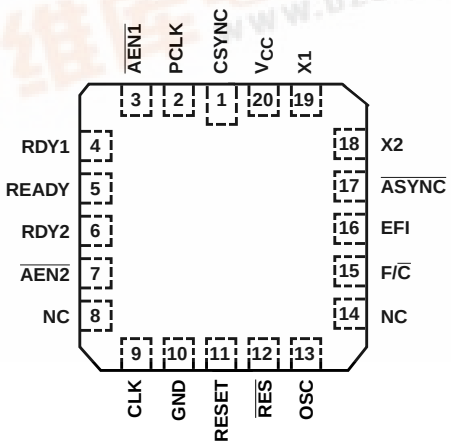
PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
CP82C84A	0^oC to $+70^oC$	18 Ld PDIP	E18.3
IP82C84A	-40^oC to $+85^oC$		E18.3
CS82C84A	0^oC to $+70^oC$	20 Ld PLCC	N20.35
IS82C84A	-40^oC to $+85^oC$		N20.35
CD82C84A	0^oC to $+70^oC$	18 Ld CERDIP	F18.3
ID82C84A	-40^oC to $+85^oC$		F18.3
MD82C84A/B	-55^oC to $+125^oC$		F18.3
8406801VA		SMD#	F18.3
MR82C84A/B	-55^oC to $+125^oC$	20 Pad CLCC	J20.A
84068012A		SMD#	J20.A

Pinouts

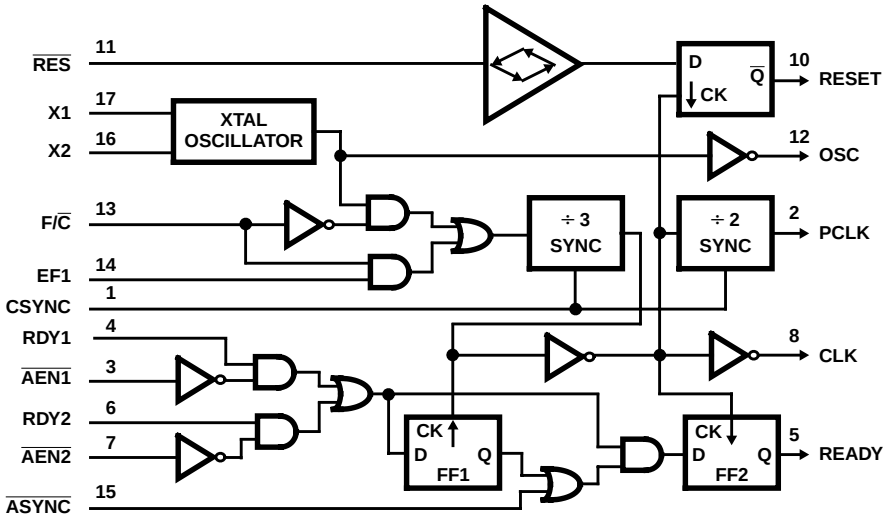
82C84A (PDIP, CERDIP)
TOP VIEW



82C84A (PLCC, CLCC)
TOP VIEW



Functional Diagram



CONTROL PIN	LOGICAL 1	LOGICAL 0
F/$\overline{C}$	External Clock	Crystal Drive
$\overline{RES}$	Normal	Reset
RDY1, RDY2	Bus Ready	Bus Not Ready
$\overline{AEN1}$, $\overline{AEN2}$	Address Disabled	Address Enable
$\overline{ASYNC}$	1 Stage Ready Synchronization	2 Stage Ready Synchronization

Pin Description

SYMBOL	NUMBER	TYPE	DESCRIPTION
$\overline{AEN1}$, $\overline{AEN2}$	3, 7	I	ADDRESS ENABLE: $\overline{AEN}$ is an active LOW signal. $\overline{AEN}$ serves to qualify its respective Bus Ready Signal (RDY1 or RDY2). $\overline{AEN}$1 validates RDY1 while $\overline{AEN2}$ validates RDY2. Two $\overline{AEN}$ signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non-Multi-Master configurations, the $\overline{AEN}$ signal inputs are tied true (LOW).
RDY1, RDY2	4, 6	I	BUS READY (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available RDY1 is qualified by $\overline{AEN1}$ while RDY2 is qualified by $\overline{AEN2}$.
$\overline{ASYNC}$	15	I	READY SYNCHRONIZATION SELECT: $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is low, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open or HIGH, a single stage of READY synchronization is provided.
READY	5	O	READY: READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
X1, X2	17, 16	I O	CRYSTAL IN: X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency, (Note 1).
F/$\overline{C}$	13	I	FREQUENCY/CRYSTAL SELECT: F/$\overline{C}$ is a strapping option. When strapped LOW. F/$\overline{C}$ permits the processor's clock to be generated by the crystal. When F/$\overline{C}$ is strapped HIGH, CLK is generated for the EFI input, (Note 1).
EFI	14	I	EXTERNAL FREQUENCY IN: When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.
CLK	8	O	PROCESSOR CLOCK: CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus. CLK has an output frequency which is 1/3 of the crystal or EFI input frequency and a 1/3 duty cycle.
PCLK	2	O	PERIPHERAL CLOCK: PCLK is a peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle.
OSC	12	O	OSCILLATOR OUTPUT: OSC is the output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
$\overline{RES}$	11	I	RESET IN: $\overline{RES}$ is an active LOW signal which is used to generate RESET. The 82C84A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.
RESET	10	O	RESET: RESET is an active HIGH signal which is used to reset the 80C86 family processors. Its timing characteristics are determined by $\overline{RES}$.
CSYNC	1	I	CLOCK SYNCHRONIZATION: CSYNC is an active HIGH signal which allows multiple 82C84As to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hardwired to ground.
GND	9		Ground
V_{CC}	18		V_{CC}: The +5V power supply pin. A 0.1µF capacitor between V_{CC} and GND is recommended for decoupling.

NOTE:

1. If the crystal inputs are not used X1 must be tied to V_{CC} or GND and X2 should be left open.

Functional Description

Oscillator

The oscillator circuit of the 82C84A is designed primarily for use with an external parallel resonant, fundamental mode crystal from which the basic operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input crystal connections. For the most stable operation of the oscillator (OSC) output circuit, two capacitors (C1 = C2) as shown in the waveform figures are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

TABLE 1. CRYSTAL SPECIFICATIONS

PARAMETER	TYPICAL CRYSTAL SPEC
Frequency	2.4 - 25MHz, Fundamental, “AT” cut
Type of Operation	Parallel
Unwanted Modes	6dB (Minimum)
Load Capacitance	18 - 32pF

Capacitors C1, C2 are chosen such that their combined capacitance

$$CT = \frac{C1 \times C2}{C1 + C2} \text{ (Including stray capacitance)}$$

matches the load capacitance as specified by the crystal manufacturer. This ensures operation within the frequency tolerance specified by the crystal manufacturer.

Clock Generator

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another 82C84A clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the 82C84A. This is accomplished with two flip-flops. (See Figure 1). The counter output is a 33% duty cycle clock at one-third the input frequency.

NOTE: The F/$\overline{C}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the ÷ 3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

Clock Outputs

The CLK output is a 33% duty cycle clock driver designed to drive the 80C86, 80C88 processors directly. PCLK is a peripheral clock signal whose output frequency is 1/2 that of CLK. PCLK has a 50% duty cycle.

Reset Logic

The reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the 82C84A.

READY Synchronization

Two READY input (RDY1, RDY2) are provided to accommodate two system busses. Each input has a qualifier ($\overline{AEN1}$ and $\overline{AEN2}$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{AEN}$ pin should be tied LOW.

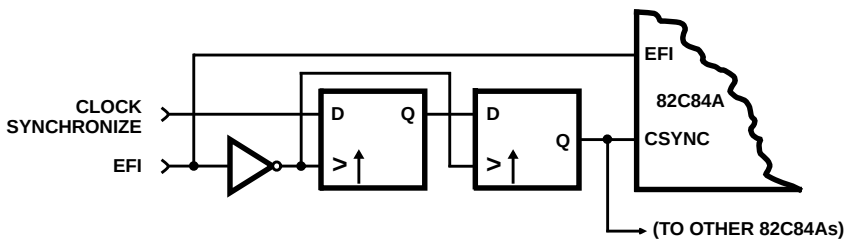
Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{ASYNC}$ input defines two modes of READY synchronization operation.

When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop one of the rising edge of CLK (requiring a setup time tR1VCH) and the synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go active (HIGH). Negative-going asynchronous READY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which the READY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, TR1VCL, on each bus cycle.

When $\overline{ASYNC}$ is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time.

$\overline{ASYNC}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.



NOTE: If EFI input is used, then crystal input X1 must be tied to V_{CC} or GND and X2 should be left open. If the crystal inputs are used, then EFI should be tied to V_{CC} or GND.

FIGURE 1. CSYNC SYNCHRONIZATION

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
C82C84A . . . . . 0^oC to $+70^oC$
I82C84A . . . . . -40^oC to $+85^oC$
M82C84A . . . . . -55^oC to $+125^oC$

Thermal Information

Thermal Resistance	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	80	20
CLCC Package	95	28
PDIP Package	85	N/A
PLCC Package	85	N/A

Storage Temperature Range . . . . . -65^oC to $+150^oC$
Max Junction Temperature . . . . . $+175^oC$
Lead Temperature (Soldering 10s) . . . . . $+300^oC$
(PLCC - Lead Tips Only)

Die Characteristics

Gate Count . . . . . 50 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = +5.0V ±10%,
T_A = 0^oC to $+70^oC$ (C82C84A),
T_A = -40^oC to $+85^oC$ (I82C84A),
T_A = -55^oC to $+125^oC$ (M82C84A)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0 2.2	-	V V	C82C84A, I82C84 M82C84A, Notes 1, 2
V_{IL}	Logical Zero Input Voltage	-	0.8	V	Notes 1, 2, 3
V_{IHR}	Reset Input High Voltage	V_{CC} -0.8	-	V	
V_{ILR}	Reset Input Low Voltage	-	0.5	V	
VT+ - VT-	Reset Input Hysteresis	0.2 V_{CC}	-	-	
V_{OH}	Logical One Output Current	V_{CC} -0.4	-	V	I_{OH} = -4.0mA for CLK Output I_{OH} = -2.5mA for All Others
V_{OL}	Logical Zero Output Voltage	-	0.4	V	I_{OL} = +4.0mA for CLK Output I_{OL} = +2.5mA for All Others
II	Input Leakage Current	-1.0	1.0	µA	V_{IN} = V_{CC} or GND except $\overline{ASYNC}$, X1: (Note 4)
I_{CCOP}	Operating Power Supply Current	-	40	mA	Crystal Frequency = 25MHz Outputs Open, Note 5

NOTES:

1. F/$\overline{C}$ is a strap option and should be held either ≤ 0.8V or ≥ 2.2V. Does not apply to X1 or X2 pins.
2. Due to test equipment limitations related to noise, the actual tested value may differ from that specified, but the specified limit is guaranteed.
3. $\overline{CSYNC}$ pin is tested with V_{IL} ≤ 0.8V.
4. $\overline{ASYNC}$ pin includes an internal 17.5kΩ nominal pull-up resistor. For $\overline{ASYNC}$ input at GND, $\overline{ASYNC}$ input leakage current = 300µA nominal, X1 - crystal feedback input.
5. f = 25MHz may be tested using the extrapolated value based on measurements taken at f = 2MHz and f = 10MHz.

Capacitance

T_A = $+25^oC$

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	10	pF	FREQ = 1MHz, all measurements are referenced to device GND
C_{OUT}	Output Capacitance	15	pF	

AC Electrical Specifications

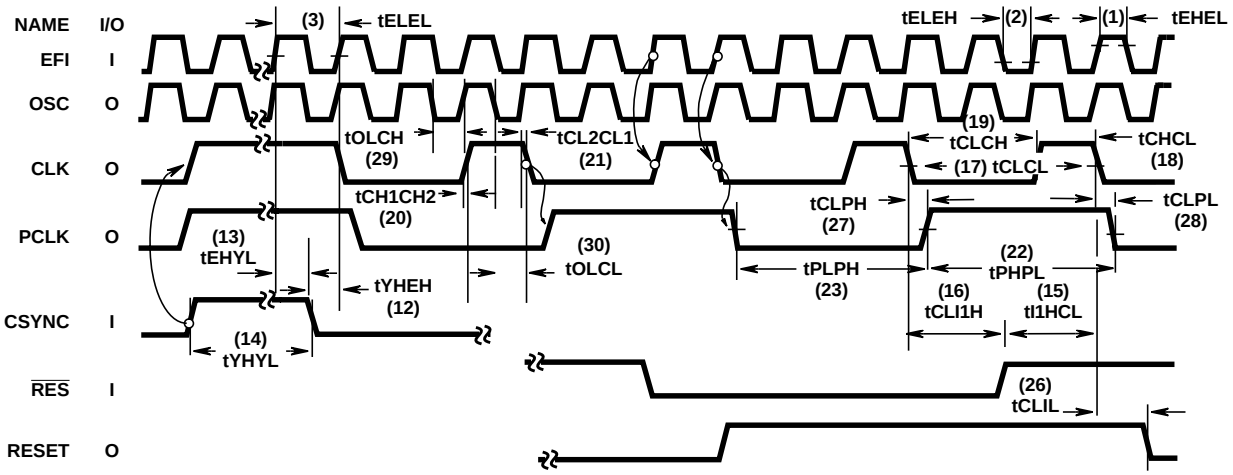
V_{CC} = +5V± 10%,
T_A = 0°C to +70°C (C82C84A),
T_A = -40°C to +85°C (I82C84A),
T_A = -55°C to +125°C (M82C84A)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	(NOTE 1) TEST CONDITIONS
TIMING REQUIREMENTS					
(1) TEHEL	External Frequency HIGH Time	13	-	ns	90%-90% V_{IN}
(2) TELEH	External Frequency LOW Time	13	-	ns	10%-10% V_{IN}
(3) TELEL	EFI Period	36	-	ns	
	XTAL Frequency	2.4	25	MHz	Note 2
(4) TR2VCL	RDY1, RDY2 Active Setup to CLK	35	-	ns	ASYNC = HIGH
(5) TR1VCH	RDY1, RDY2 Active Setup to CLK	35	-	ns	ASYNC = LOW
(6) TR1VCL	RDY1, RDY2 Inactive Setup to CLK	35	-	ns	
(7) TCLR1X	RDY1, RDY2 Hold to CLK	0	-	ns	
(8) TAYVCL	$\overline{ASYNC}$ Setup to CLK	50	-	ns	
(9) TCLAYX	$\overline{ASYNC}$ Hold to CLK	0	-	ns	
(10) TA1VR1V	$\overline{AEN1}$, $\overline{AEN2}$ Setup to RDY1, RDY2	15	-	ns	
(11) TCLA1X	$\overline{AEN1}$, $\overline{AEN2}$ Hold to CLK	0	-	ns	
(12) TYHEH	CSYNC Setup to EFI	20	-	ns	
(13) TEHYL	CSYNC Hold to EFI	20	-	ns	
(14) TYHYL	CSYNC Width	2 TELEL	-	ns	
(15) TI1HCL	$\overline{RES}$ Setup to CLK	65	-	ns	Note 3
(16) TCLI1H	$\overline{RES}$ Hold to CLK	20	-	ns	Note 3
TIMING RESPONSES					
(17) TCLCL	CLK Cycle Period	125	-	ns	Note 6
(18) TCHCL	CLK HIGH Time	(1/3 TCLCL) +2.0	-	ns	Note 6
(19) TCLCH	CLK LOW Time	(2/3 TCLCL) -15.0	-	ns	Note 6
(20) TCH1CH2 (21) TCL2CL1	CLK Rise or Fall Time	-	10	ns	1.0V to 3.0V
(22) TPHPL	PCLK HIGH Time	TCLCL-20	-	ns	Note 6
(23) TPLPH	PCLK LOW Time	TCLCL-20	-	ns	Note 6
(24) TRYLCL	Ready Inactive to CLK (See Note 4)	-8	-	ns	Note 4
(25) TRYHCH	Ready Active to CLK (See Note 3)	(2/3 TCLCL) -15.0	-	ns	Note 5
(26) TCLIL	CLK to Reset Delay	-	40	ns	
(27) TCLPH	CLK to PCLK HIGH Delay	-	22	ns	
(28) TCLPL	CLK to PCLK LOW Delay	-	22	ns	
(29) TOLCH	OSC to CLK HIGH Delay	-5	22	ns	
(30) TOLCL	OSC to CLK LOW Delay	2	35	ns	

NOTES:

1. Tested as follows: f = 2.4MHz, V_{IH} = 2.6V, V_{IL} = 0.4V, C_L = 50pF, $V_{OH} \geq 1.5V$, $V_{OL} \leq 1.5V$, unless otherwise specified. $\overline{RES}$ and F/$\overline{C}$ must switch between 0.4V and V_{CC} -0.4V. Input rise and fall times driven at 1ns/V. $V_{IL} \leq V_{IL}$ (max) - 0.4V for CSYNC pin. V_{CC} = 4.5V and 5.5V.
2. Tested using EFI or X1 input pin.
3. Setup and hold necessary only to guarantee recognition at next clock.
4. Applies only to T2 states.
5. Applies only to T3 TW states.
6. Tested with EFI input frequency = 4.2MHz.

Timing Waveforms



NOTE: All timing measurements are made at 1.5V, unless otherwise noted.

FIGURE 2. WAVEFORMS FOR CLOCKS AND RESETS SIGNALS

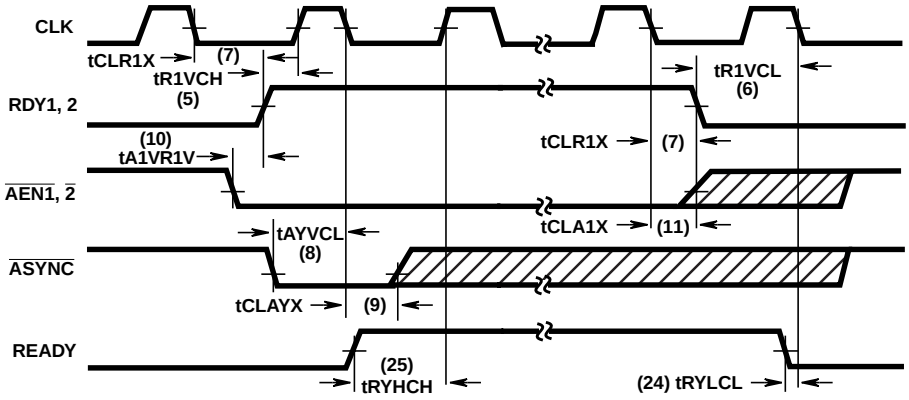


FIGURE 3. WAVEFORMS FOR READY SIGNALS (FOR ASYNCHRONOUS DEVICES)

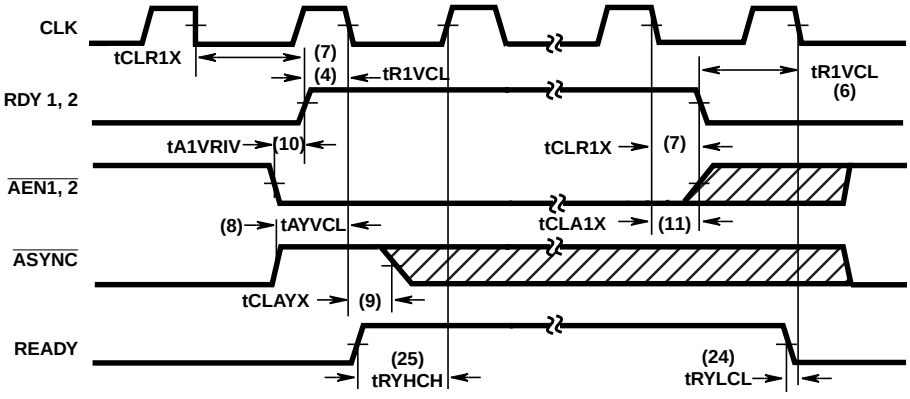
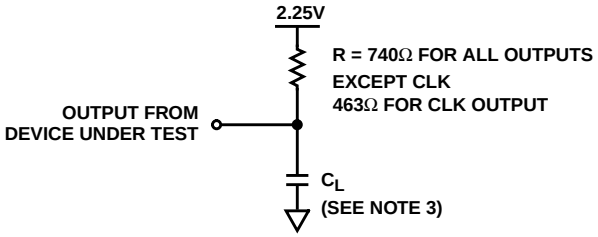


FIGURE 4. WAVEFORMS FOR READY SIGNALS (FOR SYNCHRONOUS DEVICES)

Test Load Circuits



NOTES:

1. C_L =100pF for CLK output.
2. C_L = 50pF for all outputs except CLK.
3. C_L = Includes probe and jig capacitance.

FIGURE 5. TEST LOAD MEASUREMENT CONDITIONS

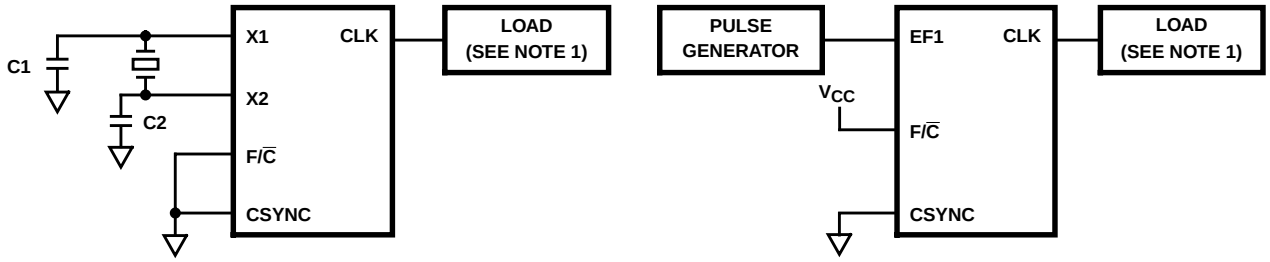


FIGURE 6. TCHCL, TCLCH LOAD CIRCUITS

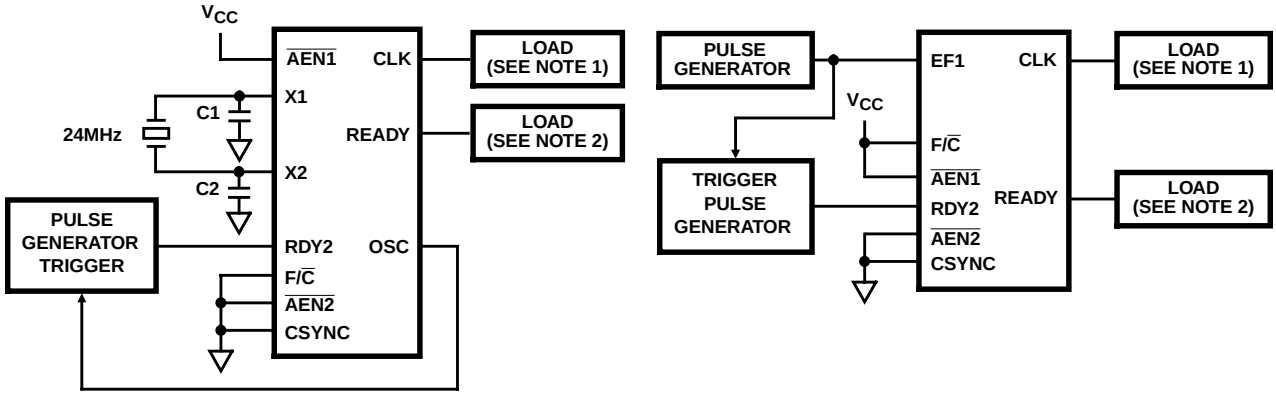
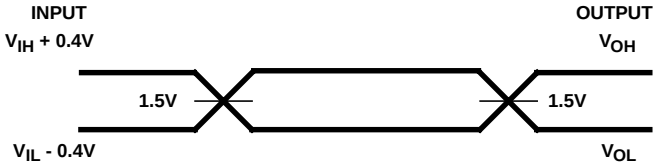


FIGURE 7. TRYLCL, TRYHCH LOAD CIRCUITS

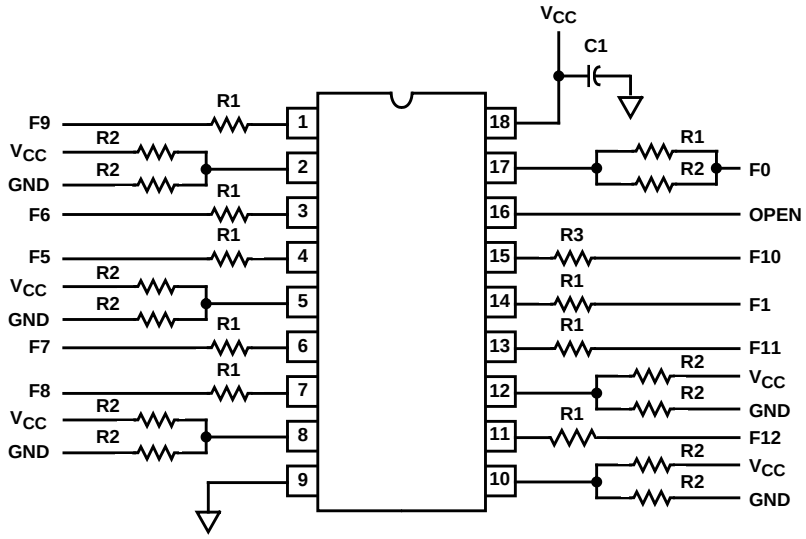
AC Testing Input, Output Waveform



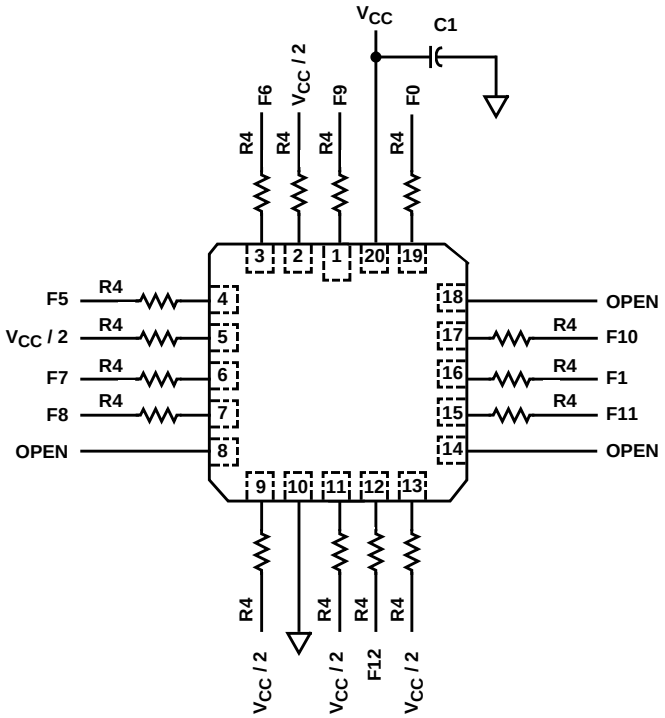
NOTE: Input test signals must switch between V_{IL} (maximum) -0.4V and V_{IH} (minimum) +0.4V. $\overline{RES}$ and F/$\overline{C}$ must switch between 0.4V and V_{CC} -0.4V. Input rise and fall times driven at 1ns/V. $V_{IL} \leq V_{IL}$ (max) -0.4V for CSYNC pin. V_{CC} -4.5V and 5.5V.

Burn-In Circuits

MD82C84A CERDIP



MR82C84A CLCC



NOTES:

V_{CC} = 5.5V ±0.5V, GND = 0V.
V_{IH} = 4.5V ±10%.
V_{IL} = -0.2 to 0.4V.
R1 = 47kΩ, ±5%.
R2 = 10kΩ, ±5%.
R3 = 2.2kΩ, ±5%.
R4 = 1.2kΩ, ±5%.
C1 = 0.01µF (minimum).
F0 = 100kHz ±10%.
F1 = F0/2, F2 = F1/2, . . . F12 = F11/2.

Die Characteristics

DIE DIMENSIONS:
66.1 x 70.5 x 19 ± 1mils

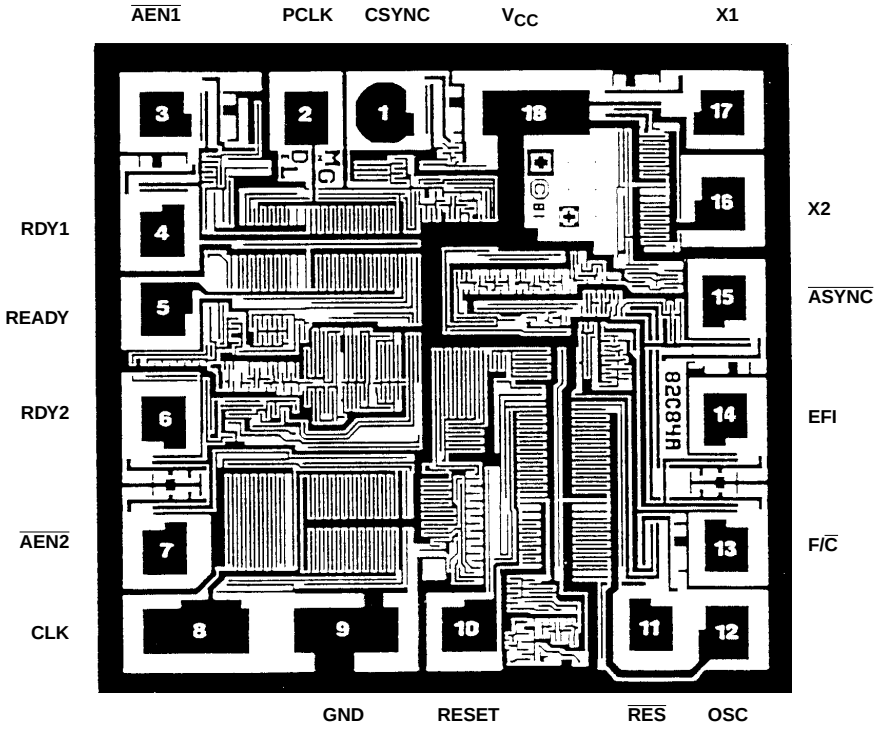
METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
1.42 x 10^5 A/cm^2

Metallization Mask Layout

82C84A



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