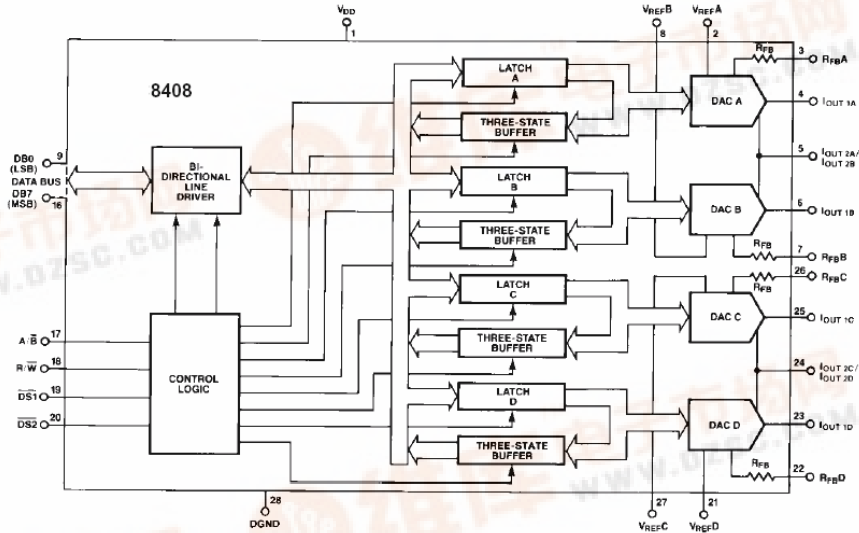
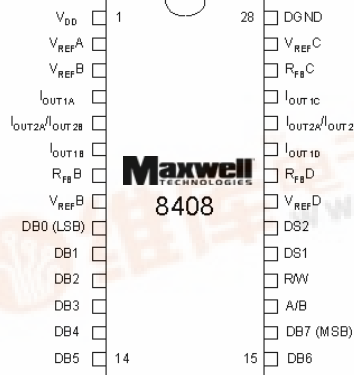




8408 Quad 8-Bit Multiplying CMOS D/A Converter with Memory



Logic Diagram

FEATURES:

- RAD-PAK® patented shielding against natural
- space radiation
- Total dose hardness:
 - equal to 100 krad (Si), depending upon orbit and space mission
- Package:
 - 28 pin RAD-PAK® Flat Pack
- Single Supply Operation (+5V)
- Four 8 Bit DACs in one 28 Pin Package
- D/As Matched to within 1%
- TTL/CMOS Compatible
- Four-Quadrant Multiplication

own reference input, feedback resistor, and onboard data latches that feature read/write capability. The readback function serves as memory for those systems requiring self-diagnostics.

A common 8-bit TTL/CMOS compatible input port is used to load data into any of the four DAC data-latches. Control lines DS1, DS2 and A/B determine which DAC will accept data. Data loading is similar to that of a RAMs write cycle. Data can be read back onto the same bus with control line R/W. The 8408 is a bus compatible with most 8-bit microprocessors, including the 6800, 8080, 8085, and Z80. The 8408 operates on a single +5 volt supply and dissipates less than 20 mW. The 8408 is manufactured using highly stable, thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS process. The improved latch-up resistant design eliminates the need for external protective Schottky diodes.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Class S.

DESCRIPTION:

Maxwell Technologies' 8408 is a monolithic quad 8-bit multiplying digital-to-analog CMOS converter. Each DAC has its



Quad 8-Bit Multiplying CMOS D/A Converter with Memory

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TABLE 1. 8408 PINOUT DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	V_{DD}	Supply Voltage
2	V_{REFA}	REF Voltage (A)
3	R_{FBA}	REF Feedback (A)
4	$I_{OUT 1A}$	Current Output (1A)
5	$I_{OUT 2A}/I_{OUT 2B}$	Current Output (2A/2B)
6	$I_{OUT 1B}$	Current Output (1B)
7	R_{FBB}	REF Feedback (B)
8	V_{REFB}	REF Voltage (B)
9	DB0 (LSB)	Data Bit 0, least significant bit
10 - 15	DB 1 - 6	Data bits 1-6
16	DB 7 (MSB)	Data Bit 7, most significant bit
17	A/\overline{B}	A/\overline{B}
18	R/\overline{W}	Read/Write
19 - 20	DS1 - 2	Data Strobes
21	V_{REFD}	REF Voltage (D)
22	R_{FBD}	REF Feedback (D)
23	$I_{OUT 1D}$	Current Output (1D)
24	$I_{OUT 2C}/I_{OUT 2D}$	Current Output (2C/2D)
25	$I_{OUT 1C}$	Current Output (1C)
26	R_{FBC}	REF Feedback (C)
27	V_{REFC}	REF Voltage (C)
28	DGND	Digital Ground

TABLE 2. 8408 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
V_{DD} to $I_{OUT 2A}$, $I_{OUT 2B}$, $I_{OUT 2C}$, $I_{OUT 2D}$	--	0	7	V
V_{DD} to DGND	--	0	7	V
$I_{OUT 1A}$, $I_{OUT 1B}$, $I_{OUT 1C}$, $I_{OUT 1D}$ to DGND	--	-0.3	$V_{DD} + 0.3$	V
R_{RFA} , R_{RFB} , V_{RFC} , R_{RFD} to I_{OUT}	--	--	± 25	V
$I_{OUT 2A}$, $I_{OUT 2B}$, $I_{OUT 2C}$, $I_{OUT 2D}$ to DGND	--	-0.3	$V_{DD} + 0.3$	V
DB0 through DB7 to DGND	--	-0.3	$V_{DD} + 0.3$	V
Control Logic Input Voltage to DGND	--	-0.3	$V_{DD} + 0.3$	V
V_{REFA} , V_{REFB} , V_{REFC} , V_{REFD} to $I_{OUT 2A}$, $I_{OUT 2B}$, $I_{OUT 2C}$, $I_{OUT 2D}$	--	--	± 25	V

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TABLE 2. 8408 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Power Dissipation	P_D	--	20	mW
Operating Temperature	T_A	-55	125	°C
Storage Temperature Range	T_S	-65	150	°C

TABLE 3. DELTA LIMITS

PARAMETER	VARIATION
I_{DD}	±10% of value specified in Table 4

TABLE 4. 8408 SPECIFICATIONS

($V_{DD} = +5\text{ V}$; $V_{REF} = \pm 10\text{ V}$; $V_{OUTA, B, C, D} = 0\text{ V}$, $T_A = -55\text{ TO } 125\text{ °C}$ UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	TEST CONDITION	SUBGROUPS	MIN	TYP	MAX	UNIT
STATIC ACCURACY							
Resolution	N		1, 2, 3	8	--	--	Bits
Non-linearity ^{1, 2}	INL		1, 2, 3	--	--	±1/2	LSB
Differential Nonlinearity	DNL		1, 2, 3	--	--	±1	LSB
Gain Error	G_{FSE}	(Using Internal R_{FB})	1, 2, 3	--	--	±1	LSB
Gain Tempco ^{3, 4}	TC_{GFS}		1, 2, 3	--	±2	±40	ppm/°C
Power Supply Rejection	PSR	$\Delta V_{DD} = \pm 10\%$	1, 2, 3	--	--	0.001	%FSR/ %
$I_{OUT\ 1A, B, C, D}$ Leakage Current ⁵	I_{LKG}	+25°C	1	--	--	±30	nA
		-55 to 125°C	2, 3	--	--	±200	
REFERENCE INPUT							
Input Voltage Range	--		1, 2, 3	--	--	±20	V
Input Resistance	R_{IN}		1, 2, 3	6	10	14	KΩ
DIGITAL INPUTS							
Digital Input High Voltage	V_{IH}		1, 2, 3	2.4	--	--	V
Digital Input Low Voltage	V_{IL}		1, 2, 3	--	--	0.8	V
Digital Input Current ⁶	I_{IN}	+25°C	1	--	±0.01	±1.0	μA
		-55 to 125°C	2, 3	--	--	±10.0	
Digital Input Capacitance ⁴	C_{IN}		1, 2, 3	--	--	8	pF
DATA BUS OUTPUTS							
Digital Output Low	V_{OL}	16 mA Sink	1, 2, 3	--	--	0.4	V
Digital Output High	V_{OH}	400 μA Source	1, 2, 3	4	--	--	V

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TABLE 4. 8408 SPECIFICATIONS

($V_{DD} = +5\text{ V}$; $V_{REF} = \pm 10\text{ V}$; $V_{OUT\ A, B, C, D} = 0\text{ V}$, $T_A = -55\text{ TO } 125\text{ }^\circ\text{C}$ UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	TEST CONDITION	SUBGROUPS	MIN	TYP	MAX	UNIT
Output Leakage Current	I_{LKG}	+25°C	1	--	±0.005	±1.0	µA
		-55 to 125°C	2, 3	--	±0.075	±10.0	
DAC OUTPUTS ⁴							
Propogation Delay ⁷	t_{PD}		9, 10, 11	--	150	180	ns
Settling Time ^{8, 9}	t_s		9, 10, 11	--	190	250	ns
Output Capacitance	C_{OUT}	DAC latches All "0s"	9, 10, 11	--	--	30	pF
		DAC latches All "1s"	9, 10, 11	--	--	50	
AC Feedthrough	FT	20 V_{P-P} @ F = 100 kHz	9, 10, 11	54	--	--	dB
SWITCHING CHARACTERISTICS ^{4, 10}							
Write to Data Strobe Time	t_{DS1}	+25°C	9	90	--	--	ns
		-55 to 125°C	10, 11	145	--	--	
Data Valid to Strobe Set-up Time	t_{DSU}	+25°C	9	150	--	--	ns
		-55 to 125°C	10, 11	175	--	--	
Data Valid to Strobe Hold Time	t_{DH}		9, 10, 11	10	--	--	ns
DAC Select to Strobe Set-Up Time	t_{AS}		9, 10, 11	0	--	--	ns
DAC Select to Strobe Hold Time	t_{AH}		9, 10, 11	0	--	--	ns
Write Select to Strobe Set-Up Time	t_{WSU}		9, 10, 11	0	--	--	ns
Write Select to Strobe Hold Time	t_{WH}		9, 10, 11	0	--	--	ns
Read to Data Strobe Width	t_{RDS}	+25°C	9	220	--	--	ns
		-55 to 125°C	10, 11	350	--	--	
Data Strobe to Output Valid Time	t_{CO}	+25°C	9	320	--	--	ns
		-55 to 125°C	10, 11	430	--	--	
Output Data Deselect Time	t_{OTD}	+25°C	9	200	--	--	ns
		-55 to 125°C	10, 11	270	--	--	
Read Select to Strobe Set-Up Time	t_{RSU}		9, 10, 11	0	--	--	ns
Read Select to Strobe Hold Time	t_{RH}		9, 10, 11	0	--	--	ns
POWER SUPPLY							
Voltage Range	V_{DD}		1, 2, 31	4.5	--	5.5	V
Supply Current ¹¹	I_{DD}		1, 2, 3	--	--	50	µA
Supply Current ¹²	I_{DD}	+25°C	1	--	--	1.0	mA
		-55 to 125°C	2, 3	--	--	1.5	

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1. This is an end-point linearity specification.
2. Guaranteed to be monotonic over the full operating temperature range.
3. ppm/°C of FSR (FSR = Full Scale Range = $V_{REF} - 1 \text{ LSB}$).
4. Guaranteed by design.
5. All Digital Inputs = 0V; $V_{REF} = +10V$.
6. Logic Inputs are MOS gates. Typical input current at +25°C is less than 10 nA.
7. From Digital Input to 90% of final analog output current.
8. Digital Inputs = 0V to V_{DD} or V_{DD} to 0V.
9. Extrapolated: $t_s (1/2 \text{ LSB}) = t_{PD} + 6.2\tau$ where τ = the measured first constant of the final RC decay.
10. See Timing Diagram
11. All Digital Inputs "0" or V_{DD} .
12. All Digital Inputs V_{IH} or V_{IL}

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FIGURE 1. TIMING DIAGRAM

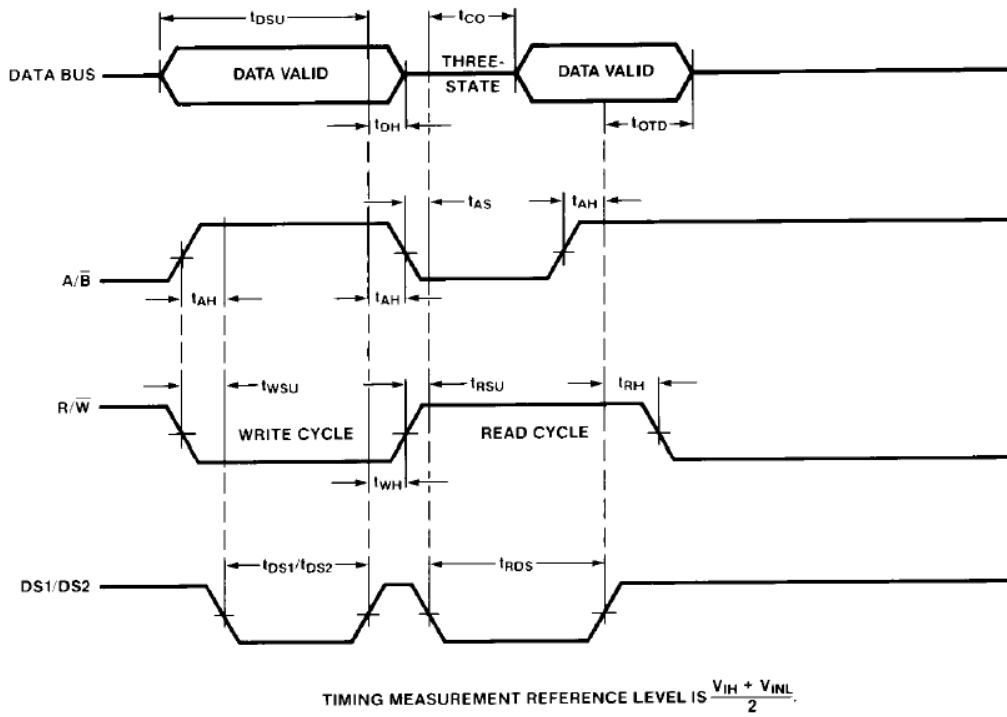
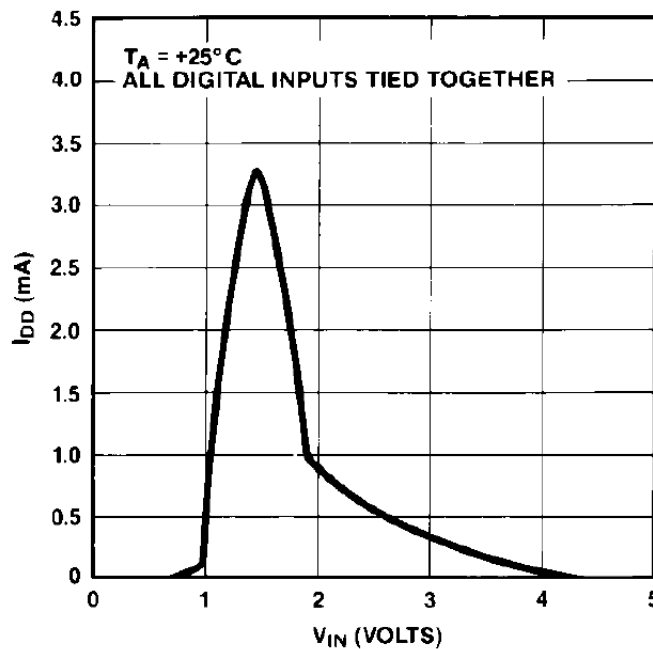


FIGURE 2. SUPPLY CURRENT VS. LOGIC LEVEL



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CIRCUIT INFORMATION

The 8408 combines four identical 8-bit CMOS DACs onto a single monolithic chip. Each DAC has its own reference input, feedback resistor, and on-board data latches. It also features a read/write function that serves as an accessible memory location for digital-input data words. The DAC's three-state readback drivers place the data word back onto the data bus.

D/A CONVERTER SECTION

Each DAC contains a highly stable, silicon-chromium, thin-film, R-2R resistor ladder network and eight pairs of current steering switches. These switches are in series with each ladder resistor and are single-pole, double-throw NMOS transistors; the gates of these transistors are controlled by CMOS inverters. Figure 3 shows a simplified circuit of the R-2R resistor ladder section, and Figure 4 shows an approximate equivalent switch circuit. The current through each resistor leg is switched between IOUT 1 and IOUT 2. This maintains a constant current in each leg, regardless of the digital input logic states.

Each transistor switch has a finite "ON" resistance that can introduce errors to the DAC's specified performance. These resistances must be accounted for by making the voltage drop across each transistor equal to each other. This is done by binarily scaling the transistor's "ON" resistance from the most significant bit (MSB) to the least significant bit (LSB). With 10 volts applied at the reference input, the current through the MSB switch is 0.5 mA, the next bit is 0.25 mA, etc.; this maintains a constant 10 mV drop across each switch and the converter's accuracy is maintained. It also results in a constant resistance appearing at the DAC's reference input terminal; this allows the DAC to be driven by a voltage or current source, ac or dc, of positive or negative polarity.

Shown in Figure 5 is an equivalent output circuit for DAC A. The circuit is shown with all digital inputs high. The leakage current source is the combination of surface and junction leakages to the substrate. The $1/256$ current source represents the constant 1-bit current drain through the ladder terminating resistor. The situation is reversed with all digital inputs low, as shown in Figure 6. The output capacitance is code dependent, and therefore, is modulated between the low and high values.

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FIGURE 3. SIMPLIFIED D/A CIRCUIT OF 8408

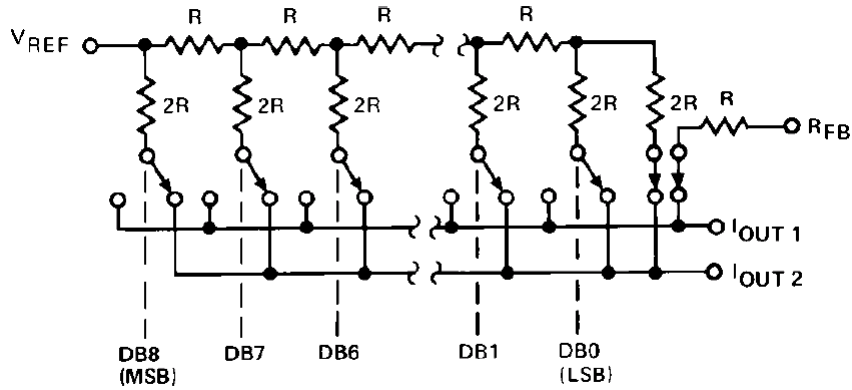


FIGURE 4. N-CHANNEL CURRENT STEERING SWITCH

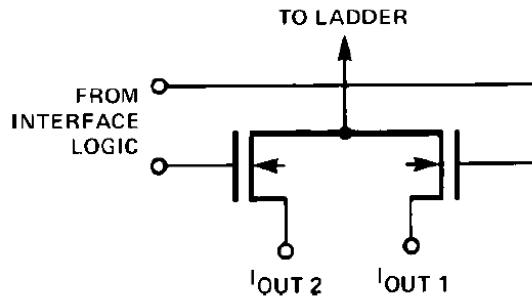
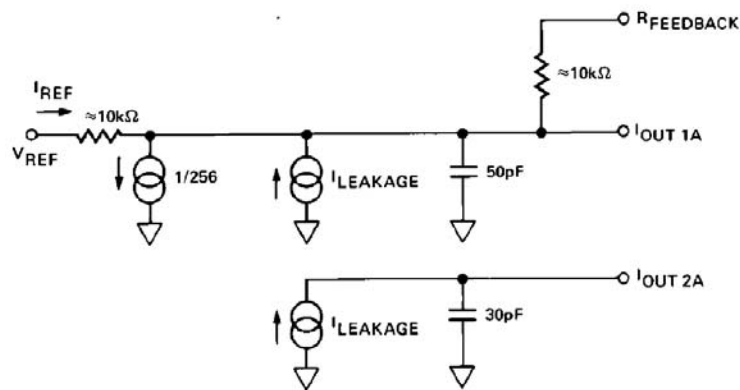


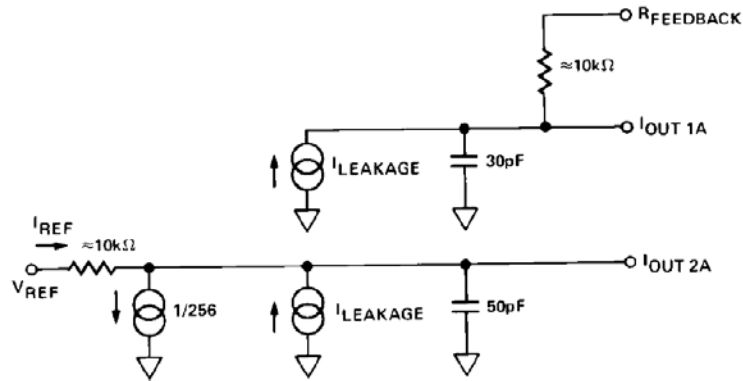
FIGURE 5. EQUIVALENT DAC CIRCUIT (ALL DIGITAL INPUTS HIGH)



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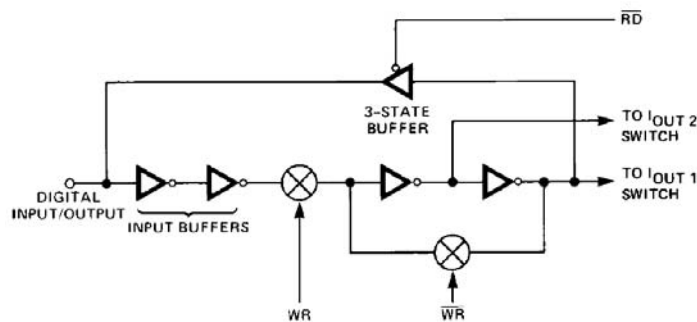
FIGURE 6. EQUIVALENT DAC CIRCUIT (All Digital Inputs LOW)



DIGITAL SECTION

Figure 7 shows the digital input/output structure for one bit. The digital \overline{WR} , \overline{WR} , and \overline{RD} controls shown in the figure are internally generated from the external A/B, R/W, $\overline{DS1}$, and $\overline{DS2}$ signals. The combination of these signals decide which DAC is selected. The digital inputs are CMOS inverters, designed such that TTL input levels (2.4 V and 0.8 V) are converted into CMOS logic levels. When the digital input is in the region of 1.2 V to 1.8 V, the input stages operate in their linear region and draw current from the +5 V supply (see Typical Supply Current vs. Logic Level curve on page 6). It is recommended that the digital input voltages be as close to VDD and DGND as is practical in order to minimize supply currents. This allows maximum savings in power dissipation inherent with CMOS devices. The three-state readback digital output drivers (in the active mode) provide TTL-compatible digital outputs with a fan-out of one TTL load. The three state digital readback leakage-current is typically 5 nA.

FIGURE 7. DIGITAL INPUT/OUTPUT STRUCTURE



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INTERFACE LOGIC SECTION

DAC Operating Modes

- All DACs in HOLD MODE.
- DAC A, B, C, or D individually selected (WRITE MODE).
- DAC A, B, C, or D individually selected (READ MODE).
- DACs A and C simultaneously selected (WRITE MODE).
- DACs B and D simultaneously selected (WRITE MODE).

DAC Selection: Control inputs, $\overline{DS1}$, $\overline{DS2}$, and $A\overline{B}$ select which DAC can accept data from the input port (see Mode Selection Table).

Mode Selection: Control inputs \overline{DS} and $R\overline{W}$ control the operating mode of the selected DAC.

Write Mode: When the control inputs \overline{DS} and $R\overline{W}$ are both low, the selected DAC is in the write mode. The input data latches of the selected DAC are transparent, and its analog output responds to activity on the data inputs DB0–DB7.

Hold Mode: The selected DAC latch retains the data that was present on the bus line just prior to \overline{DS} or $R\overline{W}$ going to a high state. All analog outputs remain at the values corresponding to the data in their respective latches.

Read Mode: When \overline{DS} is low and $R\overline{W}$ is high, the selected DAC is in the read mode, and the data held in the appropriate latch is put back onto the data bus.

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TABLE 4. MODE SELECTION TABLE

DS1	Control Logic			Mode	DAC
	DS2	A/B	R/W		
L	H	H	L	WRITE	A
L	H	L	L	WRITE	B
H	L	H	L	WRITE	C
H	L	L	L	WRITE	D
L	H	H	H	READ	A
L	H	L	H	READ	B
H	L	H	H	READ	C
H	L	L	H	READ	D
L	L	H	L	WRITE	A&C
L	L	L	L	WRITE	B&D
H	H	X	X	HOLD	A/B/C/D
L	L	H	H	HOLD	A/B/C/D
L	L	L	H	HOLD	A/B/C/D

L = Low State, H = High State, X = Irrelevant

BASIC APPLICATIONS

Some basic circuit configurations are shown in Figures 8 and 9. Figure 8 shows the 8408 connected in a unipolar configuration (2-Quadrant Multiplication), and Table 5 shows the Code Table. Resistors R1, R2, R3, and R4 are used to trim full scale output. Full-scale output voltage = $V_{REF} - 1 \text{ LSB} = V_{REF} (1-2^{-8})$ or $V_{REF} \times (255/256)$ with all digital inputs high. Low temperature coefficient (approximately 50 ppm/°C) resistors or trimmers should be selected if used. Full scale can also be adjusted using V_{REF} voltage. This will eliminate resistors R1, R2, R3, and R4. In many applications, R1 through R4 are not required, and the maximum gain error will then be that of the DAC.

Each DAC exhibits a variable output resistance that is code dependent. This produces a code-dependent, differential nonlinearity term at the amplifier's output which can have a maximum value of 0.67 times the amplifier's offset voltage. This differential nonlinearity term adds to the R-2R resistor ladder differential nonlinearity; the output may no longer be monotonic. To maintain monotonicity and minimize gain and linearity errors, it is recommended that the op amp offset voltage be adjusted to less than 10% of 1 LSB (1 LSB = $2^{-8} \times V_{REF}$ or $1/256 \times V_{REF}$), or less than 3.9 mV over the operating temperature range. Zeroscale output voltage (with all digital inputs low) may be adjusted using the op amp offset adjustment. Capacitors C1, C2, C3, and C4 provide phase compensation and help prevent overshoot and ringing when using high speed op amps.

Figure 9 shows the recommended circuit configuration for the bipolar operation (4-quadrant multiplication), and Table 6 shows the Code Table. Trimmer resistors R17, R18, R19, and R20 are used only if gain error adjustments are required and range between 50 Ω and 1000 Ω. Resistors R21, R22, R23, and R24 will range between 50 Ω and 500 Ω. If these resistors are used, it is essential that resistor pairs R9–R13, R10–R14, R11–R15, R12–R16 are matched both in value and tempco. They should be within 0.01%; wire wound or metal foil types are preferred for best temperature coefficient matching. The circuits of Figure 8 and 9 can either be used as a fixed reference D/A converter, or as an attenuator with an ac input voltage.

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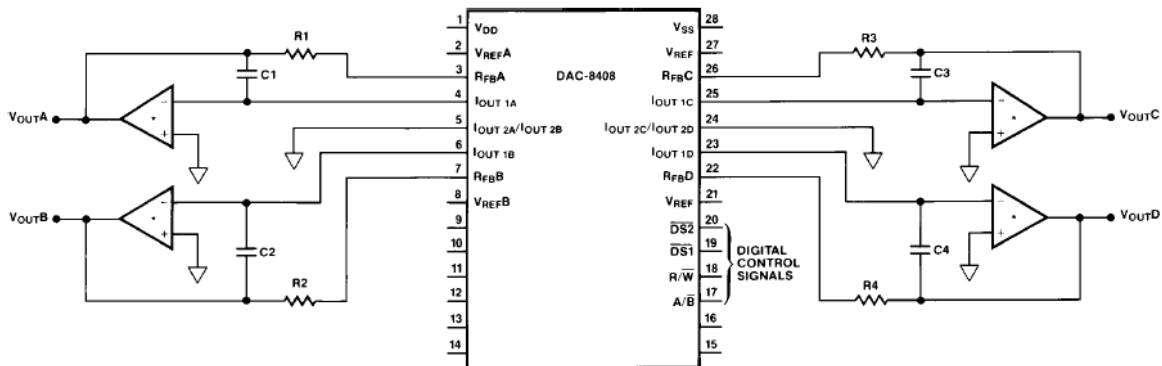
TABLE 5. UNIPOLAR BINARY CODE TABLE (REFER TO FIGURE 8)

DAC Data Input MSB	LSB	Analog Output
1	1 1 1 1 1 1 1 1	$-V_{REF} \left(\frac{255}{256} \right)$
1	0 0 0 0 0 0 0 1	$-V_{REF} \left(\frac{129}{256} \right)$
1	0 0 0 0 0 0 0 0	$-V_{REF} \left(\frac{128}{256} \right) = \frac{-V_{IN}}{2}$
0	1 1 1 1 1 1 1 1	$-V_{REF} \left(\frac{127}{256} \right)$
0	0 0 0 0 0 0 0 1	$-V_{REF} \left(\frac{1}{256} \right)$
0	0 0 0 0 0 0 0 0	$-V_{REF} \left(\frac{0}{256} \right) = 0$

NOTE

$$1 \text{ LSB} = (2^{-8}) (V_{REF}) = \frac{1}{256} (V_{REF})$$

FIGURE 8. QUAD DAC UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)



*ALL AMPLIFIERS ARE OP-27s, 1/4 OP-420s, OR 1/4 OP-421s.

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FIGURE 9. QUAD DAC BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

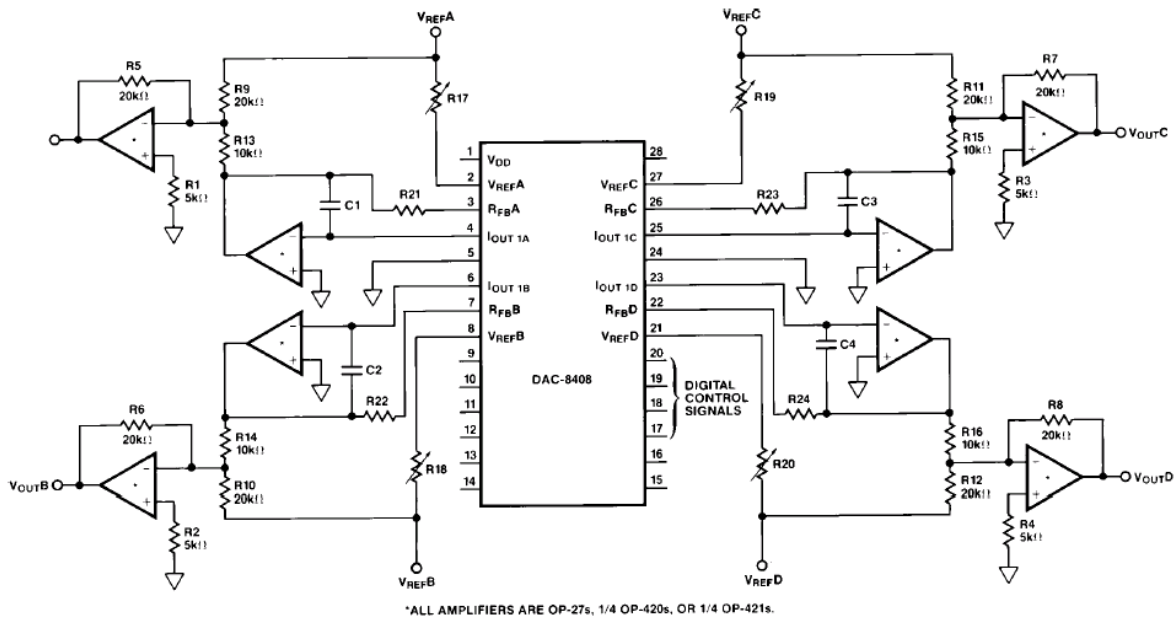


TABLE 6. BIPOLAR (OFFSET BINARY) CODE TABLE (REFER TO FIGURE 9)

DAC Data Input		Analog Output (DAC A OR DAC B)
MSB	LSB	
1	1 1 1 1 1 1 1 1	$+V_{REF} \left(\frac{127}{128} \right)$
1	0 0 0 0 0 0 0 1	$+V_{REF} \left(\frac{1}{128} \right)$
1	0 0 0 0 0 0 0 0	0
0	1 1 1 1 1 1 1 1	$-V_{REF} \left(\frac{1}{128} \right)$
0	0 0 0 0 0 0 0 1	$-V_{REF} \left(\frac{127}{128} \right)$
0	0 0 0 0 0 0 0 0	$-V_{REF} \left(\frac{128}{128} \right)$

NOTE

$$1 \text{ LSB} = (2^{-7}) (V_{REF}) = \frac{1}{128} (V_{REF})$$

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APPLICATION HINTS

General Ground Management: AC or transient voltages between AGND and DGND can appear as noise at the 8408's analog output. Note that in Figures 5 and 6, IOUT2A/IOUT2B and IOUT 2C/IOUT 2D are connected to AGND. Therefore, it is recommended that AGND and DGND be tied together at the 8408 socket. In systems where AGND and DGND are tied together on the backplane, two diodes (1N914 or equivalent) should be connected in inverse parallel between AGND and DGND.

Write Enable Timing: During the period when both \overline{DS} and $\overline{R/W}$ are held low, the DAC latches are transparent and the analog output responds directly to the digital data input. To prevent unwanted variations of the analog output, the $\overline{R/W}$ should not go low until the data bus is fully settled (DATA VALID).

SINGLE SUPPLY, VOLTAGE OUTPUT OPERATION

The 8408 can be connected with a single +5 V supply to produce DAC output voltages from 0 V to +1.5 V. In Figure 10, the 8408 R-2R ladder is inverted from its normal connection. A +1.500 V reference is connected to the current output pin 4 (IOUT 1A), and the normal VREF input pin becomes the DAC output. Instead of a normal current output, the R-2R ladder outputs a voltage. The OP-490, consisting of four precision low power op amps that can operate its inputs and outputs to zero volts, buffers the DAC to produce a low impedance output voltage from 0 V to +1.5 V full-scale. Table 7 shows the code table.

With the supply and reference voltages as shown, better than 1/2 LSB differential and integral nonlinearity can be expected. To maintain this performance level, the +5 V supply must not drop below 4.75 V. Similarly, the reference voltage must be no higher than 1.5 V. This is because the CMOS switches require a minimum level of bias in order to maintain the linearity performance.

TABLE 7. SINGLE SUPPLY BINARY CODE TABLE (REFER TO FIGURE 10)

DAC Data Input		Analog Output
MSB	LSB	
1	1 1 1 1 1 1 1 1	$V_{REF} \left(\frac{255}{256} \right), +1.4941 \text{ V}$
1	0 0 0 0 0 0 0 1	$V_{REF} \left(\frac{129}{256} \right), +0.7559 \text{ V}$
1	0 0 0 0 0 0 0 0	$V_{REF} \left(\frac{128}{256} \right), +0.7500 \text{ V}$
0	1 1 1 1 1 1 1 1	$V_{REF} \left(\frac{127}{256} \right), +0.7441 \text{ V}$
0	0 0 0 0 0 0 0 1	$V_{REF} \left(\frac{1}{256} \right), +0.0059 \text{ V}$
0	0 0 0 0 0 0 0 0	$V_{REF} \left(\frac{0}{256} \right), 0.0000 \text{ V}$

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FIGURE 10. UNIPOLAR SUPPLY, VOLTAGE OUTPUT DAC OPERATION

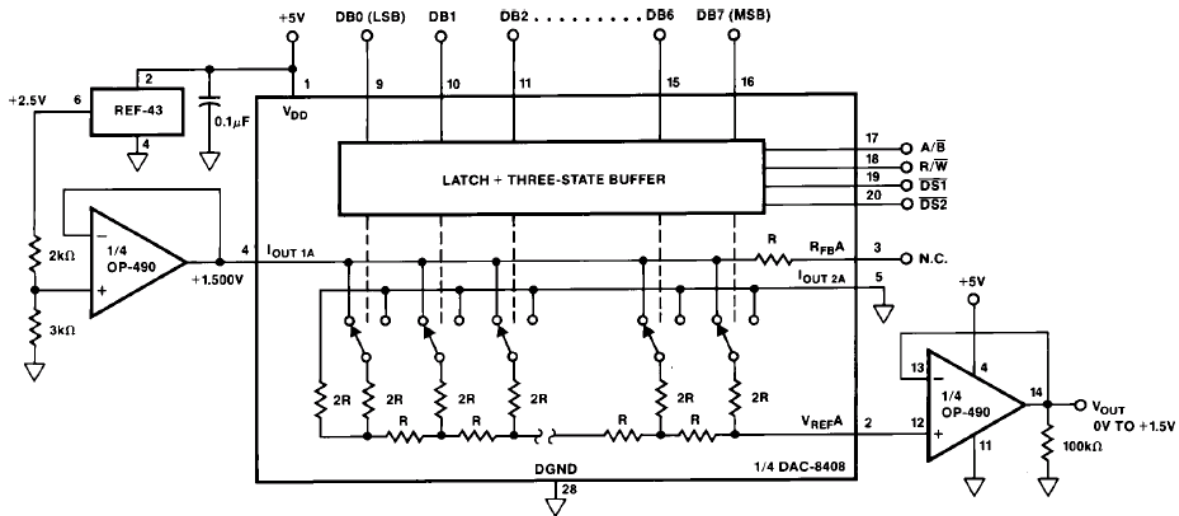
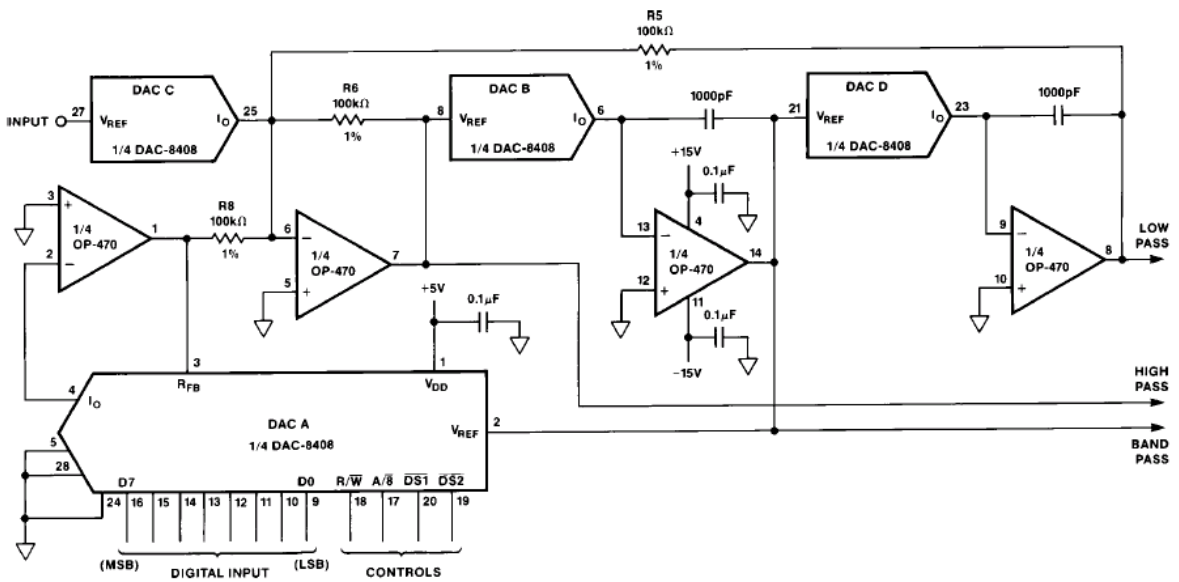


FIGURE 11. A DIGITALLY PROGRAMMABLE UNIVERSAL ACTIVE FILTER



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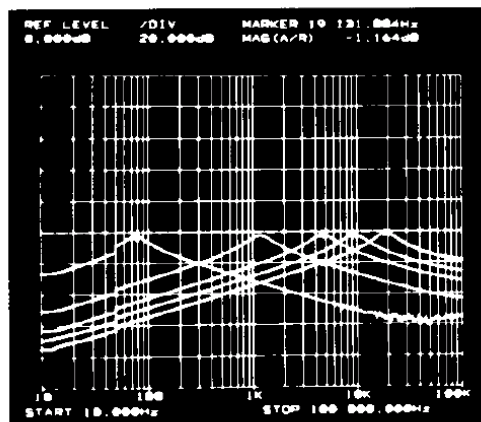
8408

A DIGITALLY PROGRAMMABLE ACTIVE FILTER

A powerful D/A converter application is a programmable active filter design as shown in Figure 11. The design is based on the state-variable filter topology which offers stable and repeatable filter characteristics. DAC B and DAC D can be programmed in tandem with a single digital byte load which sets the center frequency of the filter. DAC A sets the Q of the filter. DAC C sets the gain of the filter transfer function. The unique feature of this design is that varying the gain of filter does not affect the Q of the filter. Similarly, the reverse is also true. This makes the programmability of the filter extremely reliable and predictable. Note that low-pass, high-pass, and bandpass outputs are available. This sophisticated function is achieved in only two IC packages.

The network analyzer photo shown in Figure 12 superimposes five actual bandpass responses ranging from the lowest frequency of 75 Hz (1 LSB ON) to a full-scale frequency of 19.132 kHz (all bits ON), which is equivalent to a 256 to 1 dynamic range. The frequency is determined by $f_C = 1/2\pi RC$ where R is the ladder resistance (RIN) of the 8408, and C is 1000 pF. Note that from device to device, the resistance RIN varies. Thus some tuning may be necessary.

FIGURE 12. PROGRAMMABLE ACTIVE FILTER BAND-PASS FREQUENCY RESPONSE



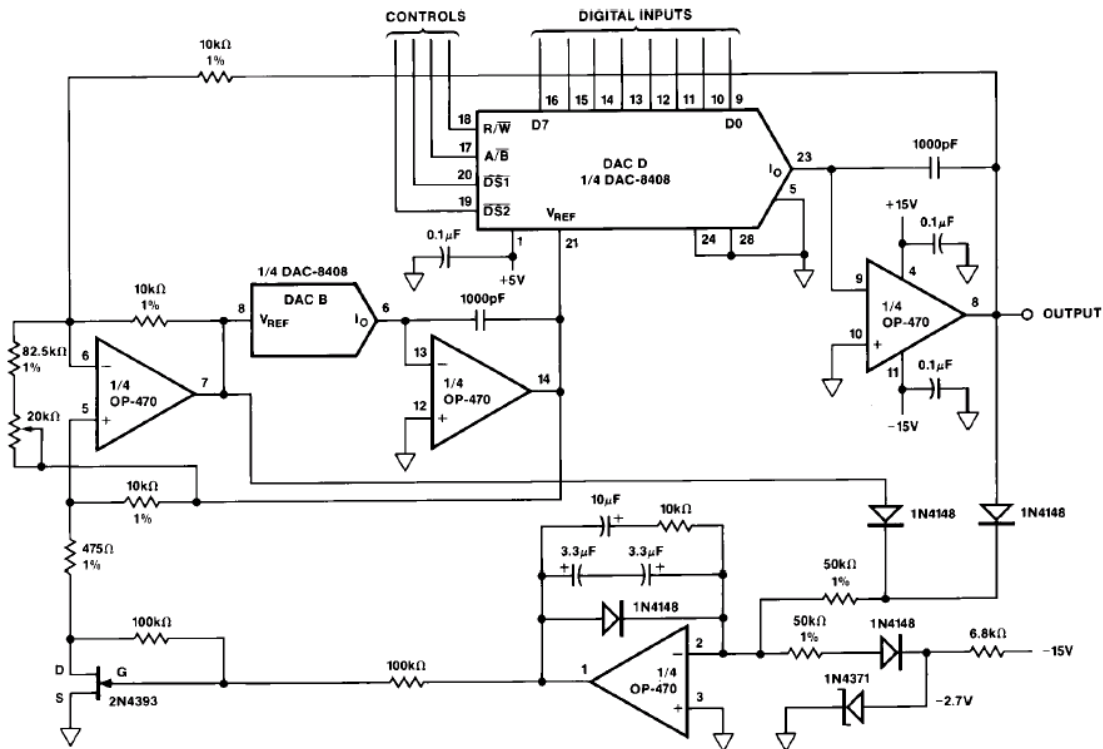
**THE CIRCUIT PROVIDES FULL 8-BIT
(> 2 DECADE) DYNAMIC RANGE OF
FREQUENCY CONTROL**

All components used are available off-the-shelf. Using low drift thin-film resistors, the 8408 exhibits very stable performance over temperature. The wide bandwidth of the OP-470 produces excellent high frequency and high Q response. In addition, the OP470's low input offset voltage assures an unusually low dc offset at the filter output.

Quad 8-Bit Multiplying CMOS D/A Converter with Memory

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FIGURE 13. A DIGITALLY PROGRAMMABLE, LOW-DISTORTION SINEWAVE OSCILLATOR



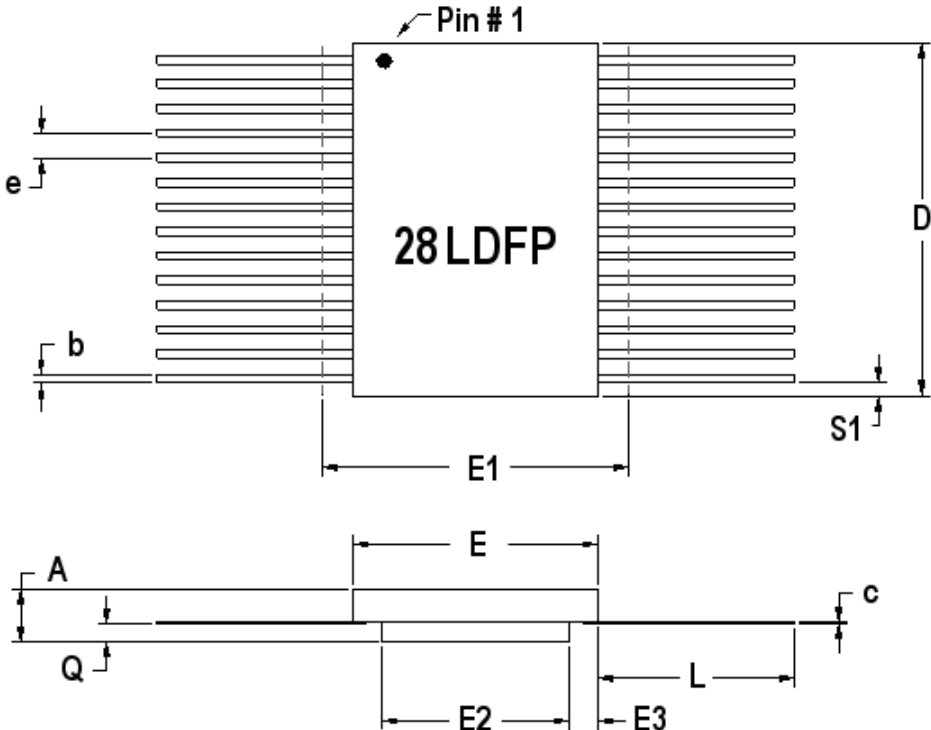
A LOW-DISTORTION, PROGRAMMABLE SINEWAVE OSCILLATOR

By varying the previous state-variable filter topology slightly, one can obtain a very low distortion sinewave oscillator with programmable frequency feature as shown in Figure 13. Again, DAC B and DAC D in tandem control the oscillating frequency based on the relationship $fC = 1/2\pi RC$. Positive feedback is accomplished via the 82.5 kΩ and the 20 kΩ potentiometer. The Q of the oscillator is determined by the ratio of 10 kΩ and 475Ω in series with the FET transistor, which acts as an automatic gain control variable resistor. The AGC action maintains a very stable sinewave amplitude at any frequency. Again, only two ICs accomplish a very useful function.

At the highest frequency setting, the harmonic distortion level measures 0.016%. As the frequencies drop, distortion also drops to a low of 0.006%. At the lowest frequency setting, distortion came back up to a worst case of 0.035%

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28 PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.190	0.207	0.224
b	0.015	0.017	0.022
c	0.004	0.005	0.009
D	--	0.720	0.740
E	0.380	0.410	0.420
E1	--	--	0.440
E2	0.180	0.250	--
E3	0.030	0.080	--
e	0.050 BSC		
L	0.360	0.370	0.380
Q	0.062	0.073	0.081
S1	0.000	0.027	--
N	28		

F28-02

Note: All dimensions in inches

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Product Ordering Options

