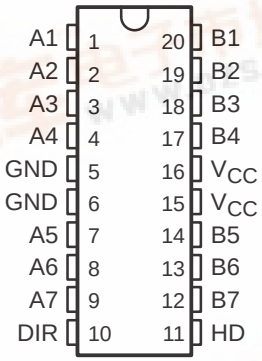
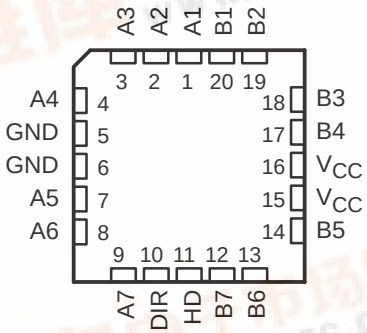
- 3-State Outputs Directly Drive Bus Lines
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Designed for the IEEE 1284-I (Level 1 Type) and IEEE 1284-II (Level 2 Type) Electrical Specifications
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and DIP (N) Packages, Ceramic Chip Carriers (FK), Flat (W), and DIP (J) Packages

SN54ACT1284 . . . J OR W PACKAGE
SN74ACT1284 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



description

The ’ACT1284 are designed for asynchronous two-way communication between data buses. The control function minimizes external timing requirements.

The devices allow data transmission in either the A-to-B or the B-to-A direction for bits 1, 2, 3, and 4, depending on the logic level at the direction-control (DIR) input. Bits 5, 6, and 7, however, always transmit in the A-to-B direction.

The output drive for each mode is determined by the high drive (HD) control pin. When HD is high, the high drive is delivered by the totem-pole configuration, and when HD is low, the outputs are open drain. This meets the drive requirements as specified in the IEEE 1284-I (level 1 type) and the IEEE 1284-II (level 2 type) parallel peripheral-interface specification.

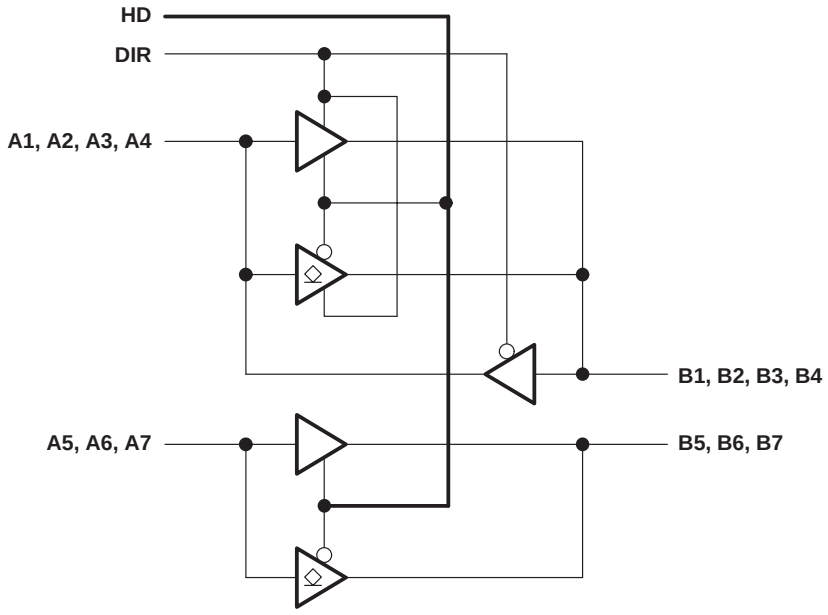
The SN54ACT1284 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ACT1284 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS		OUTPUT	MODE
DIR	HD		
L	L	Open drain	A to B: Bits 5, 6, 7
		Totem pole	B to A: Bits 1, 2, 3, 4
L	H	Totem pole	B to A: Bits 1, 2, 3, 4 and A to B: Bits 5, 6, 7
H	L	Open drain	A to B: Bits 1, 2, 3, 4, 5, 6, 7
H	H	Totem pole	A to B: Bits 1, 2, 3, 4, 5, 6, 7

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
B-port input and output voltage range, V_I and V_O (see Notes 1 and 2) . . . . . –2 V to 7 V
A-port input and output voltage range, V_I and V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±200 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package . . . . . 115°C/W
DW package . . . . . 97°C/W
N package . . . . . 67°C/W
PW package . . . . . 128°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The ac input voltage pulsewidth is limited to 20 ns if the input voltage goes more negative than –0.5 V.
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

			SN54ACT1284		SN74ACT1284		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.7	5.5	4.7	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Open drain output voltage	HD low	0	5.5	0	5.5	V
I_{OH}	High-level output current	B port, HD high		–14		–14	mA
		A port		–4		–4	
I_{OL}	Low-level output current	B port		14		14	mA
		A port		4		4	
T_A	Operating free-air temperature		–55	125	0	70	°C

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

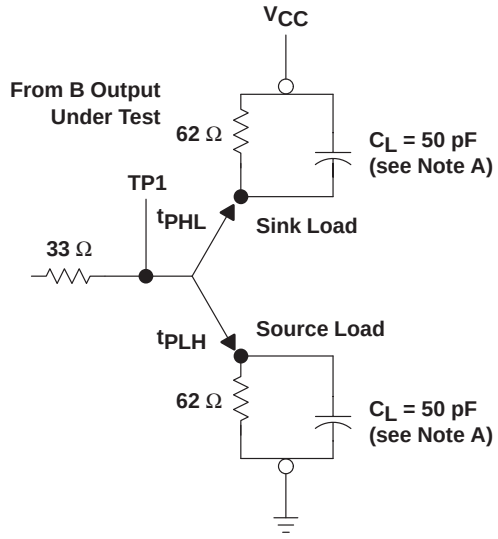
PARAMETER		TEST CONDITIONS	V_{CC}†	SN54ACT1284			SN74ACT1284			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{hys}	Input hysteresis	$V_{IT+} – V_{IT–}$ for all inputs	5 V	0.4			0.4			V
			4.7 V	0.2			0.2			
V_{OH}	B port	I_{OH} = –14 mA	4.7 V	2.4			2.4			V
	A port	I_{OH} = –50 µA	MIN to MAX	V_{CC}–0.2			V_{CC}–0.2			
		I_{OH} = –4 mA	4.7 V	3.7			3.7			
V_{OL}	B port	I_{OL} = 14 mA	4.7 V			0.4			0.4	V
	A port	I_{OL} = 50 µA	4.7 V			0.2			0.2	
		I_{OL} = 4 mA				0.4			0.4	
I_I		$V_I = V_{CC}$ or GND	5.5 V			±1			±1	µA
I_{OZ}	A or B ports‡	$V_O = V_{CC}$ or GND	5.5 V			±20			±20	µA
I_{OFF}	B port	V_I or $V_O \le 7$ V	0 V			±100			±100	µA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			1.5			1.5	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4			4		pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		12			12		pF
Z_O	B port	I_{OH} = –20 mA, I_{OH} = –50 mA	5 V	8		30	8		30	Ω

† For I/O ports, the parameter I_{OZ} includes the input leakage current I_I.
‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

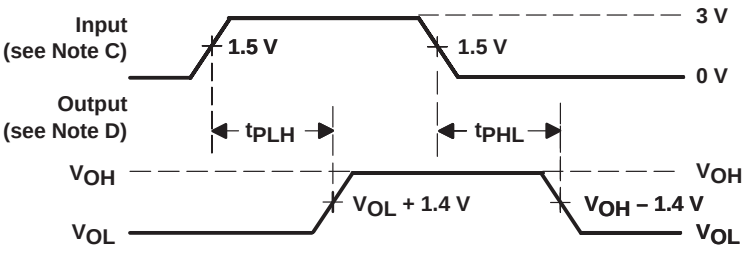
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	SN54ACT1284		SN74ACT1284		UNIT
				MIN	MAX	MIN	MAX	
t_{PLH}	Totem pole	A or B	B or A	1	20	1	20	ns
t_{PHL}				1	20	1	20	
SR	Totem pole	B output		0.05	0.4	0.05	0.4	V/ns
t_{pd}(EN)	Totem pole	HD	B	1	20	1	20	ns
t_{pd}(DIS)				1	20	1	20	
t_r, t_f	Open drain	A	B		120		120	ns

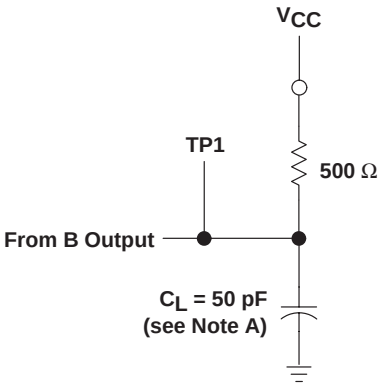
PARAMETER MEASUREMENT INFORMATION



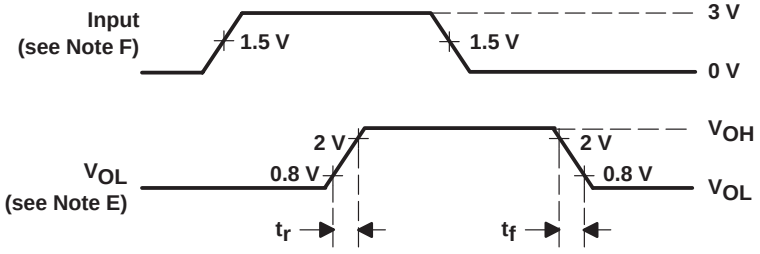
A-TO-B LOAD (totem pole)



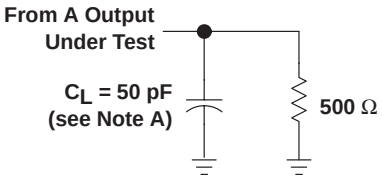
VOLTAGE WAVEFORMS MEASURED AT TP1
PROPAGATION DELAY TIMES (A to B)



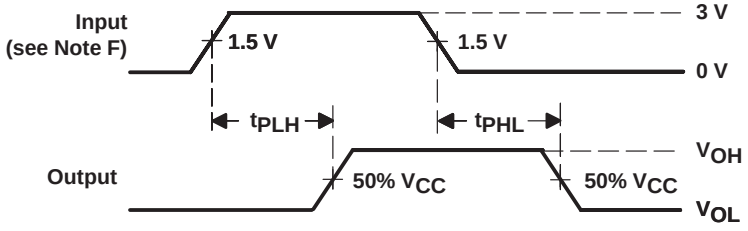
A-TO-B LOAD (open drain)



VOLTAGE WAVEFORMS MEASURED AT TP1 (B SIDE)



B-TO-A LOAD (totem pole)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)

NOTES: A. CL includes probe and jig capacitance.
B. The outputs are measured one at a time with one transition per measurement.
C. Input rise and fall times are 3 ns, 150 ns < pulsewidth <10 μs for both low-to-high and high-to-low transitions.
D. Slew rate is defined as 10% and 90% of the transition times.
E. Rise and fall times, open drain, are <120 ns.
F. Input rise and fall times are 3 ns.

Figure 1. Load Circuits and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.