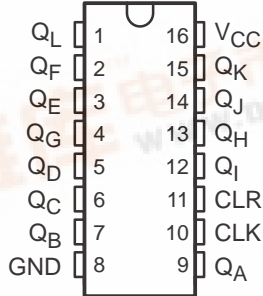
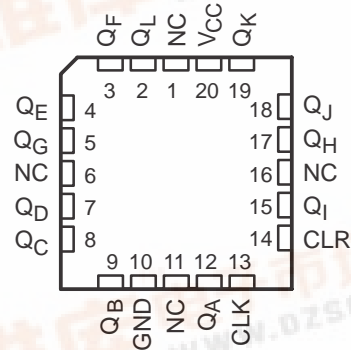


- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 12$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max

SN54HC4040 . . . J OR W PACKAGE
 SN74HC4040 . . . D, DB, N, NS, OR PW PACKAGE
 (TOP VIEW)



SN54HC4040 . . . FK PACKAGE
 (TOP VIEW)



NC – No internal connection

description/ordering information

The 'HC4040 devices are 12-stage asynchronous binary counters, with the outputs of all stages available externally. A high level at the clear (CLR) input asynchronously clears the counter and resets all outputs low. The count is advanced on a high-to-low transition at the clock (CLK) input. Applications include time-delay circuits, counter controls, and frequency-dividing circuits.

ORDERING INFORMATION

| T_A | PACKAGE† | PACKAGE† | ORDERABLE PART NUMBER | TOP-SIDE MARKING | |
|----------------|--------------|---------------|-----------------------|------------------|--------|
| -40°C to 85°C | PDIP – N | Tube of 25 | SN74HC4040N | SN74HC4040N | |
| | | Tube of 40 | SN74HC4040D | HC4040 | |
| | SOIC – D | Reel of 2500 | SN74HC4040DR | | |
| | | Reel of 250 | SN74HC4040DT | | |
| | SOP – NS | SSOP – DB | Reel of 2000 | SN74HC4040NSR | HC4040 |
| | | | Reel of 2000 | SN74HC4040DBR | HC4040 |
| TSSOP – PW | | | Tube of 90 | SN74HC4040PW | HC4040 |
| | Reel of 2000 | SN74HC4040PWR | | | |
| | Reel of 250 | SN74HC4040PWT | | | |
| -55°C to 125°C | CDIP – J | Tube of 25 | SNJ54HC4040J | SNJ54HC4040J | |
| | CFP – W | Tube of 150 | SNJ54HC4040W | SNJ54HC4040W | |
| | LCCC – FK | Tube of 55 | SNJ54HC4040FK | SNJ54HC4040FK | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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 On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54HC4040, SN74HC4040

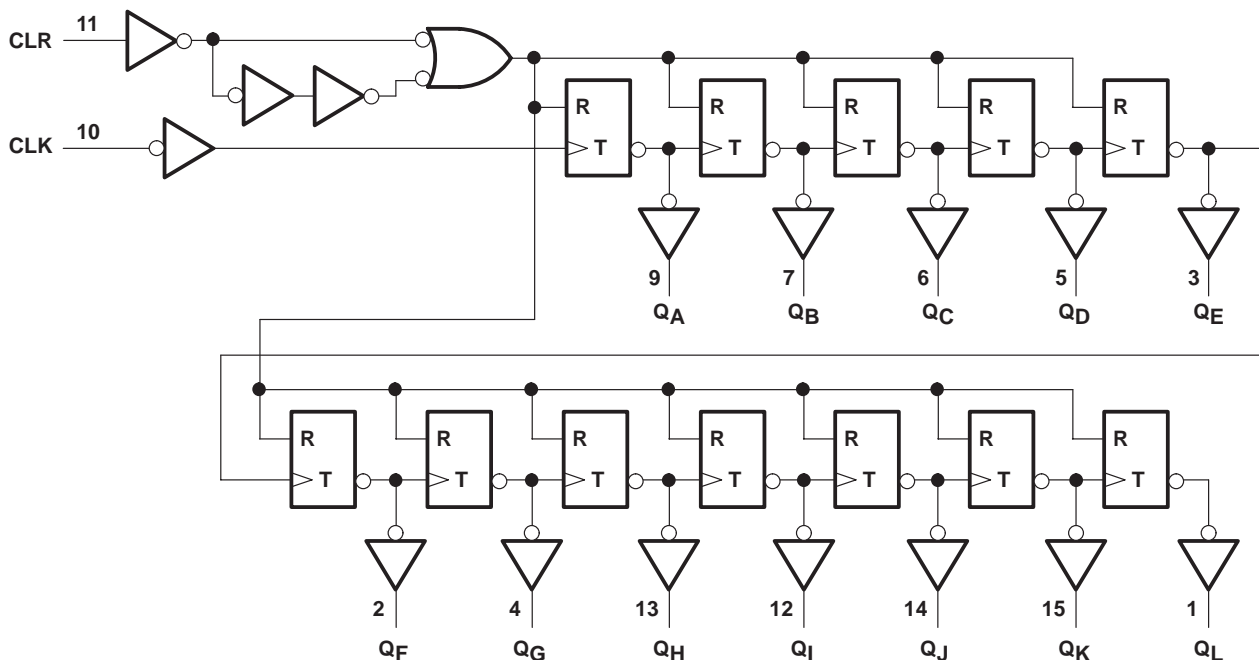
12-BIT ASYNCHRONOUS BINARY COUNTERS

SCLS160D – DECEMBER 1982 – REVISED SEPTEMBER 2003

FUNCTION TABLE
(each buffer)

| INPUTS | | FUNCTION |
|--------|-----|-----------------------|
| CLK | CLR | |
| ↑ | L | No change |
| ↓ | L | Advance to next stage |
| X | H | All outputs L |

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) | ± 20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) | ± 20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ± 25 mA |
| Continuous current through V_{CC} or GND | ± 50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): | |
| D package | 73°C/W |
| DB package | 82°C/W |
| N package | 67°C/W |
| NS package | 64°C/W |
| PW package | 108°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54HC4040, SN74HC4040

12-BIT ASYNCHRONOUS BINARY COUNTERS

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recommended operating conditions (see Note 3)

| | | SN54HC4040 | | | SN74HC4040 | | | UNIT |
|--------------------|---------------------------------|-------------------------|-----------------|------|------------|-----------------|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 2 | 5 | 6 | 2 | 5 | 6 | V |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | | 1.5 | 1.5 | | V | |
| | | V _{CC} = 4.5 V | | 3.15 | 3.15 | | | |
| | | V _{CC} = 6 V | | 4.2 | 4.2 | | | |
| V _{IL} | Low-level input voltage | V _{CC} = 2 V | | | 0.5 | | V | |
| | | V _{CC} = 4.5 V | | | 1.35 | | | |
| | | V _{CC} = 6 V | | | 1.8 | | | |
| V _I | Input voltage | 0 | V _{CC} | | 0 | V _{CC} | | V |
| V _O | Output voltage | 0 | V _{CC} | | 0 | V _{CC} | | V |
| Δt/Δv [†] | Input transition rise/fall time | V _{CC} = 2 V | | 1000 | | 1000 | | ns |
| | | V _{CC} = 4.5 V | | 500 | | 500 | | |
| | | V _{CC} = 6 V | | 400 | | 400 | | |
| T _A | Operating free-air temperature | -55 | | 125 | -40 | | 85 | °C |

[†] If this device is used in the threshold region (from V_{ILmax} = 0.5 V to V_{IHmin} = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | SN54HC4040 | | SN74HC4040 | | UNIT |
|-----------------|---|--------------------------|-----------------------|------|-------|------------|-------|------------|------|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = -20 μA | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | V |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | |
| | | I _{OH} = -4 mA | 4.5 V | 3.98 | 4.3 | | 3.7 | | 3.84 | |
| | | | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 μA | 2 V | | 0.002 | 0.1 | | 0.1 | 0.1 | V |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | 0.1 | |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | 0.1 | |
| | | I _{OL} = 4 mA | 4.5 V | | 0.17 | 0.26 | | 0.4 | 0.33 | |
| | | | 6 V | | 0.15 | 0.26 | | 0.4 | 0.33 | |
| I _I | V _I = V _{CC} or 0 | 6 V | | ±0.1 | ±100 | | ±1000 | ±1000 | nA | |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | 6 V | | | 8 | | 160 | 80 | μA | |
| C _i | | 2 V to 6 V | | 3 | 10 | | 10 | 10 | pF | |

SN54HC4040, SN74HC4040

12-BIT ASYNCHRONOUS BINARY COUNTERS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | V _{CC} | T _A = 25°C | | SN54HC4040 | | SN74HC4040 | | UNIT |
|--------------------|--------------------------------------|-----------------|-----------------------|-----|------------|-----|------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | 2 V | 5.5 | | 3.7 | | 4.3 | | MHz |
| | | 4.5 V | 28 | | 19 | | 22 | | |
| | | 6 V | 33 | | 22 | | 25 | | |
| t _w | Pulse duration | CLK high or low | 2 V | 90 | 135 | | 115 | | ns |
| | | | 4.5 V | 18 | 27 | | 23 | | |
| | | | 6 V | 15 | 23 | | 20 | | |
| | CLR high | 2 V | 70 | 105 | | 90 | | | |
| | | 4.5 V | 14 | 21 | | 18 | | | |
| | | 6 V | 12 | 18 | | 15 | | | |
| t _{su} | Setup time, CLR inactive before CLK↓ | 2 V | 60 | 90 | | 75 | | ns | |
| | | 4.5 V | 12 | 18 | | 15 | | | |
| | | 6 V | 10 | 15 | | 13 | | | |

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | T _A = 25°C | | | SN54HC4040 | | SN74HC4040 | | UNIT |
|------------------|--------------|----------------|-----------------|-----------------------|-----|-----|------------|-----|------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f _{max} | | | 2 V | 5.5 | 10 | 3.7 | | 4.3 | | MHz | |
| | | | 4.5 V | 28 | 45 | 19 | | 22 | | | |
| | | | 6 V | 33 | 53 | 22 | | 25 | | | |
| t _{pd} | CLK | Q _A | 2 V | 62 150 | | 225 | | 190 | | ns | |
| | | | 4.5 V | 16 30 | | 45 | | 38 | | | |
| | | | 6 V | 12 26 | | 38 | | 32 | | | |
| t _{PHL} | CLR | Any | 2 V | 63 140 | | 210 | | 175 | | ns | |
| | | | 4.5 V | 17 28 | | 42 | | 35 | | | |
| | | | 6 V | 13 24 | | 36 | | 30 | | | |
| t _t | | Any | 2 V | 28 75 | | 110 | | 95 | | ns | |
| | | | 4.5 V | 8 15 | | 22 | | 19 | | | |
| | | | 6 V | 6 13 | | 19 | | 16 | | | |

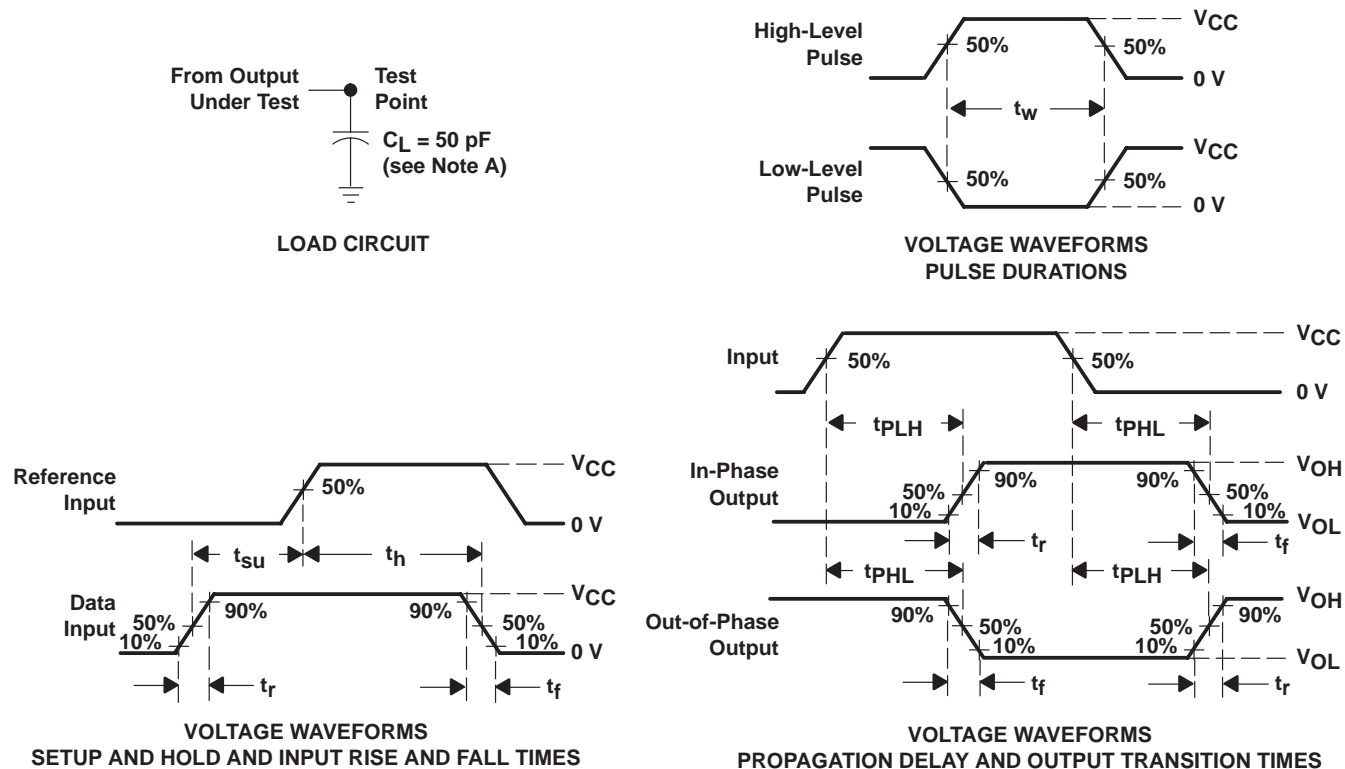
operating characteristics, T_A = 25°C

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|---|-----------------|-----|------|
| C _{pd} Power dissipation capacitance | No load | 88 | pF |

SN54HC4040, SN74HC4040 12-BIT ASYNCHRONOUS BINARY COUNTERS

SCLS160D – DECEMBER 1982 – REVISED SEPTEMBER 2003

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|--|
| 85004012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | Call TI | Level-NC-NC-NC |
| 8500401EA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| 8500401FA | ACTIVE | CFP | W | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| SN54HC4040J | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| SN74HC4040D | ACTIVE | SOIC | D | 16 | 40 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HC4040DBLE | OBSOLETE | SSOP | DB | 16 | | TBD | Call TI | Call TI |
| SN74HC4040DBR | ACTIVE | SSOP | DB | 16 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HC4040DR | ACTIVE | SOIC | D | 16 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HC4040DT | ACTIVE | SOIC | D | 16 | 250 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HC4040DWR | OBSOLETE | SOIC | DW | 16 | | TBD | Call TI | Call TI |
| SN74HC4040N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| SN74HC4040N3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI |
| SN74HC4040NSR | ACTIVE | SO | NS | 16 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HC4040PW | ACTIVE | TSSOP | PW | 16 | 90 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN74HC4040PWLE | OBSOLETE | TSSOP | PW | 16 | | TBD | Call TI | Call TI |
| SN74HC4040PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN74HC4040PWT | ACTIVE | TSSOP | PW | 16 | 250 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SNJ54HC4040FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | Call TI | Level-NC-NC-NC |
| SNJ54HC4040J | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| SNJ54HC4040W | ACTIVE | CFP | W | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



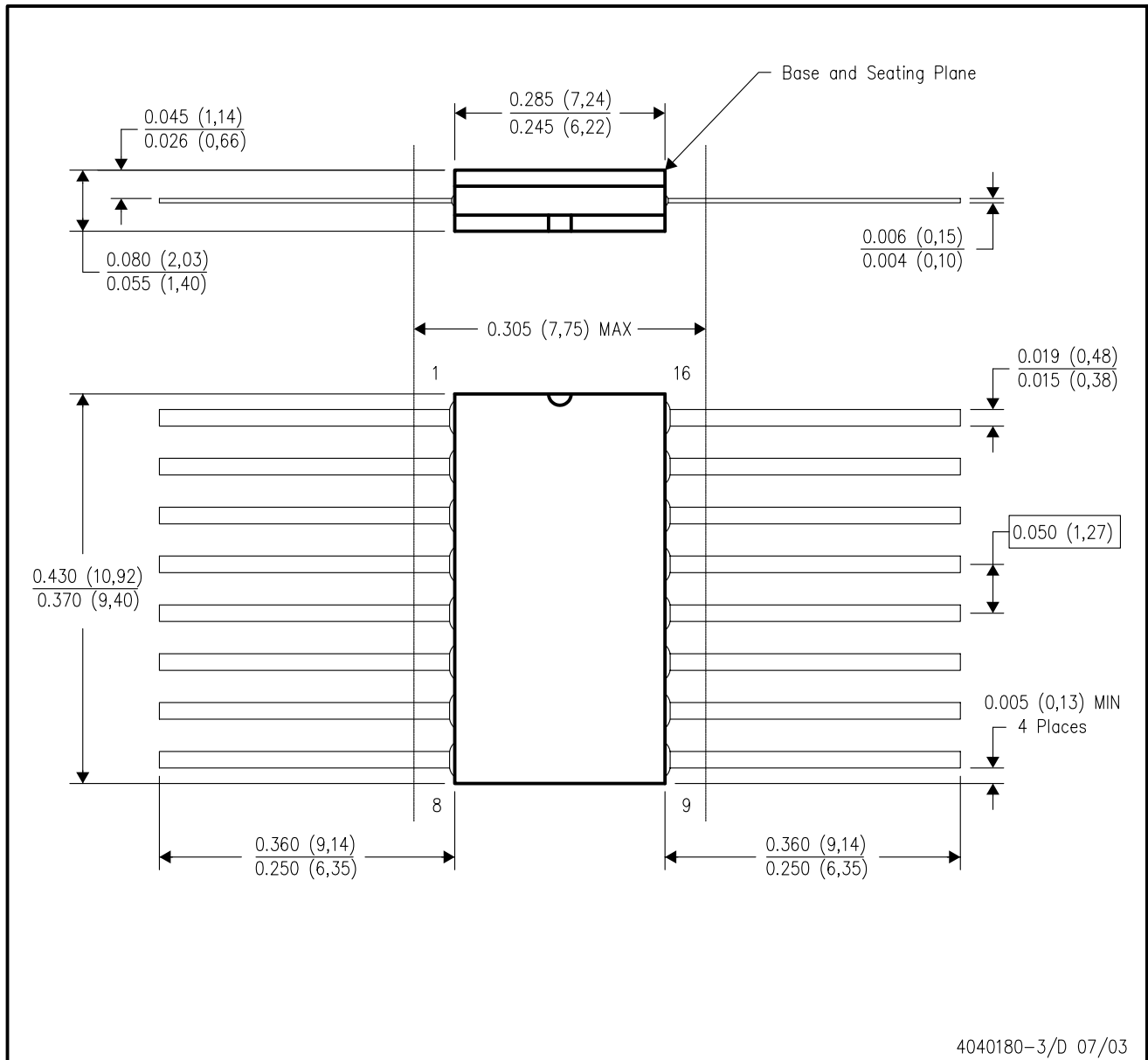
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

MECHANICAL DATA

MLCC006B – OCTOBER 1996

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



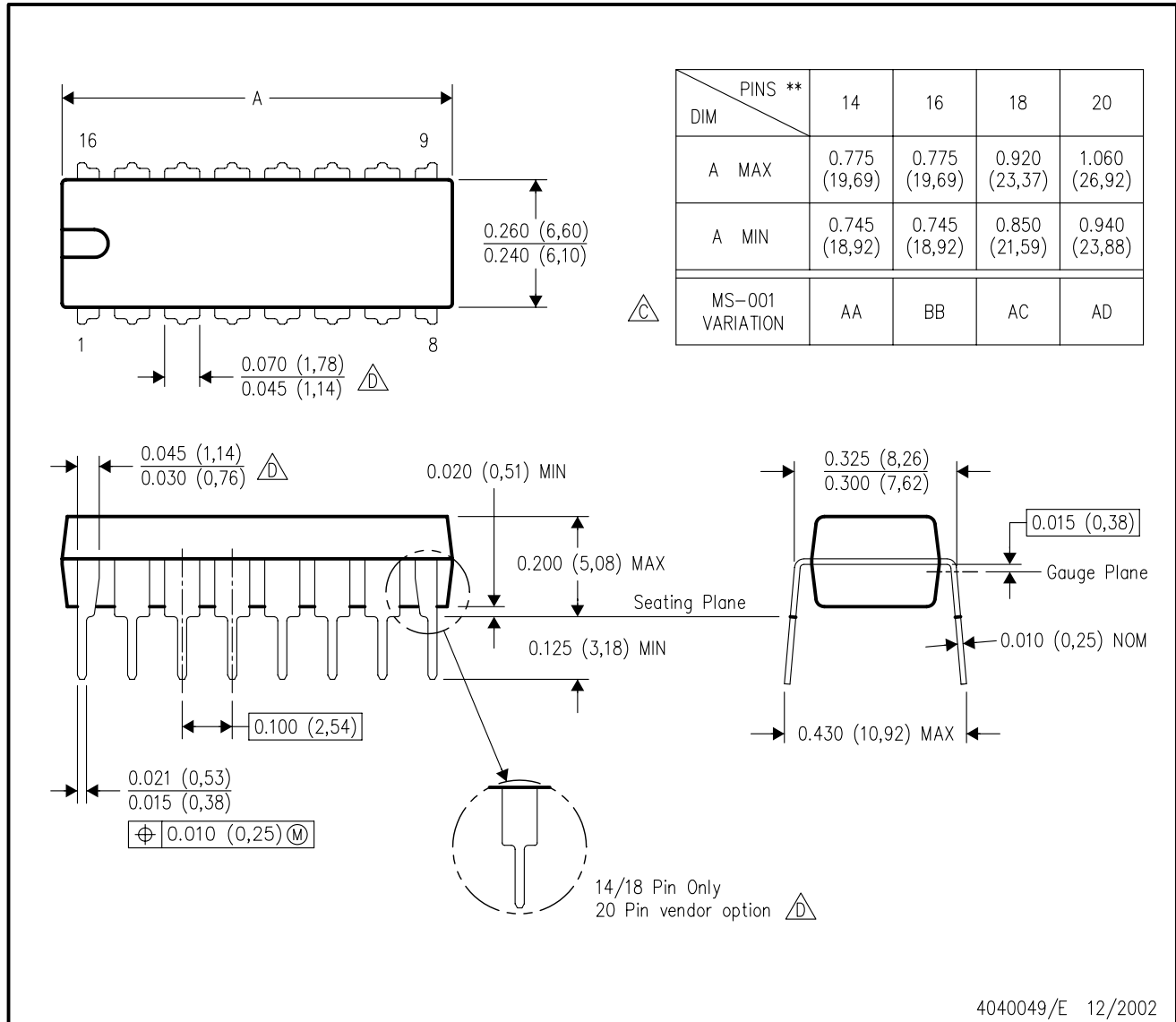
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

MECHANICAL DATA

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



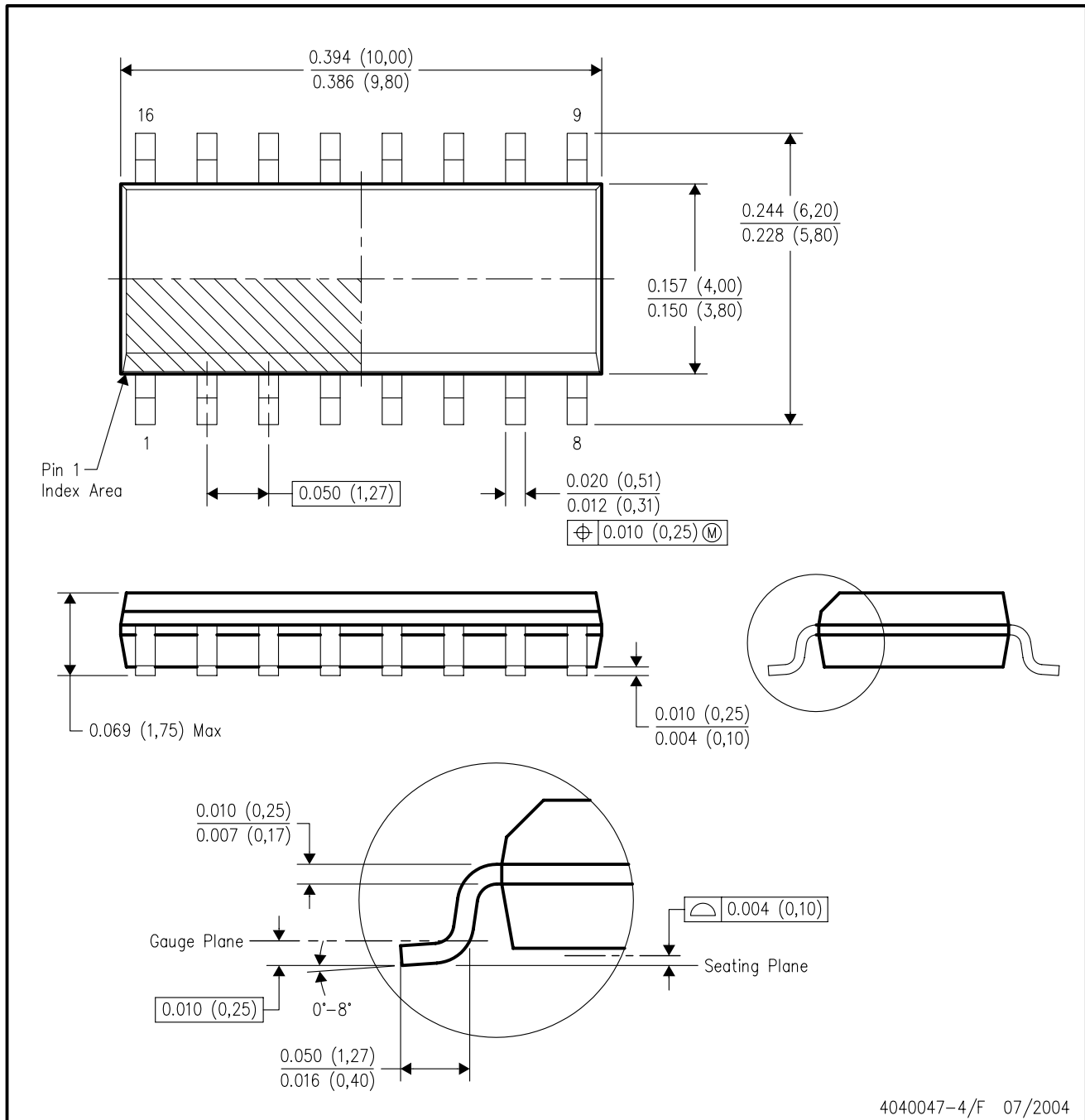
4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

D (R-PDSO-G16)

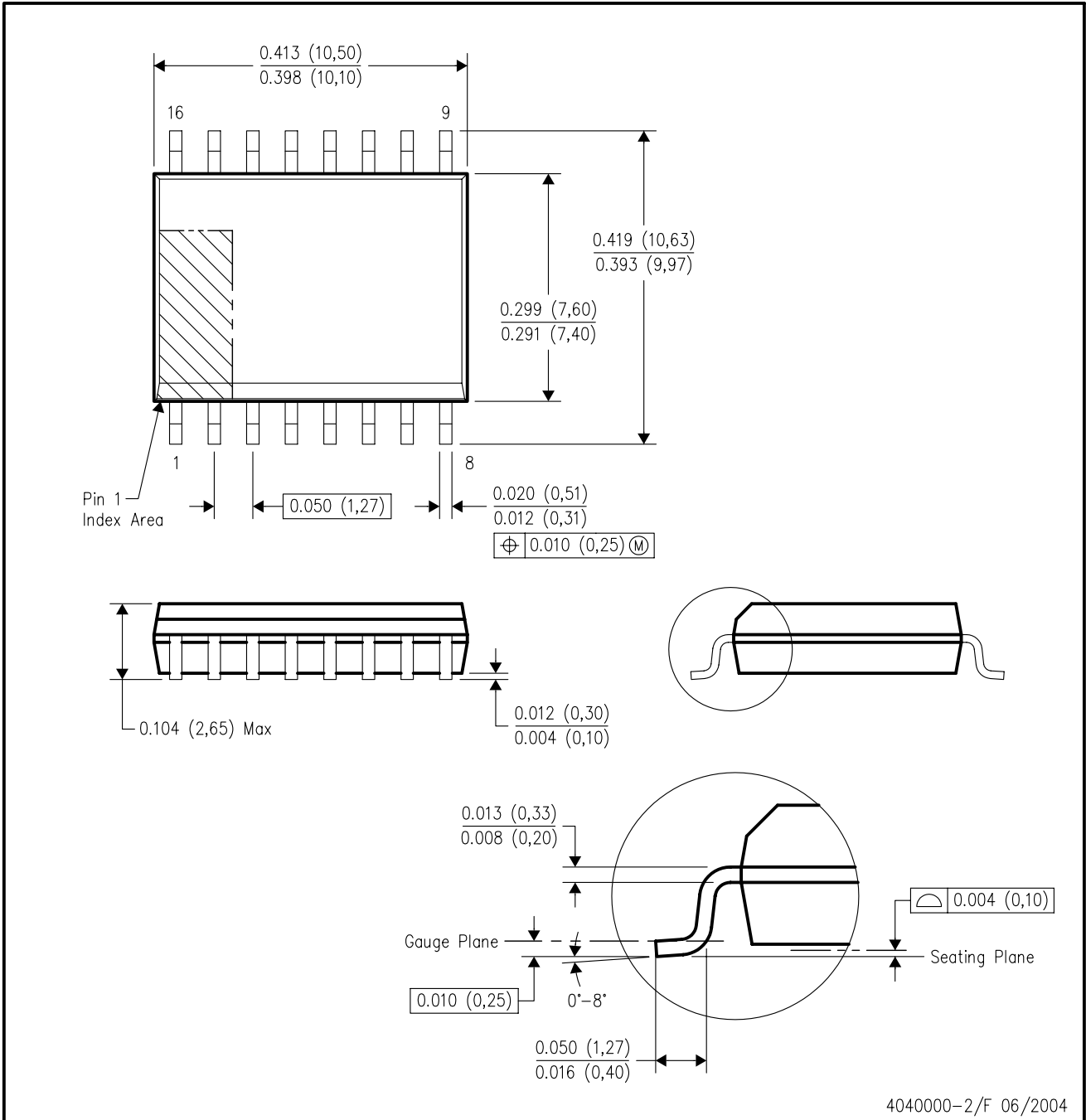
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-012 variation AC.

DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



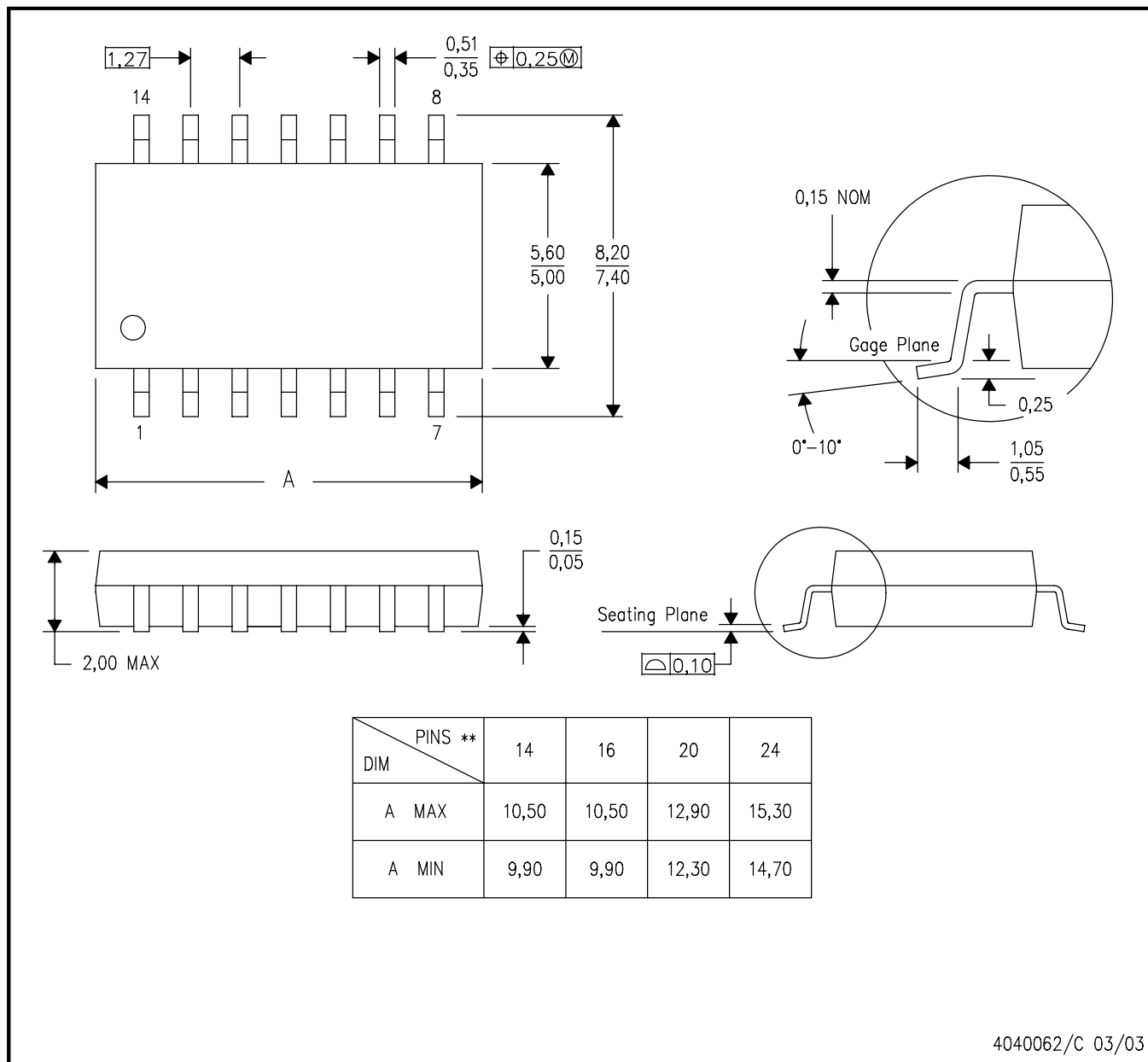
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AA.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

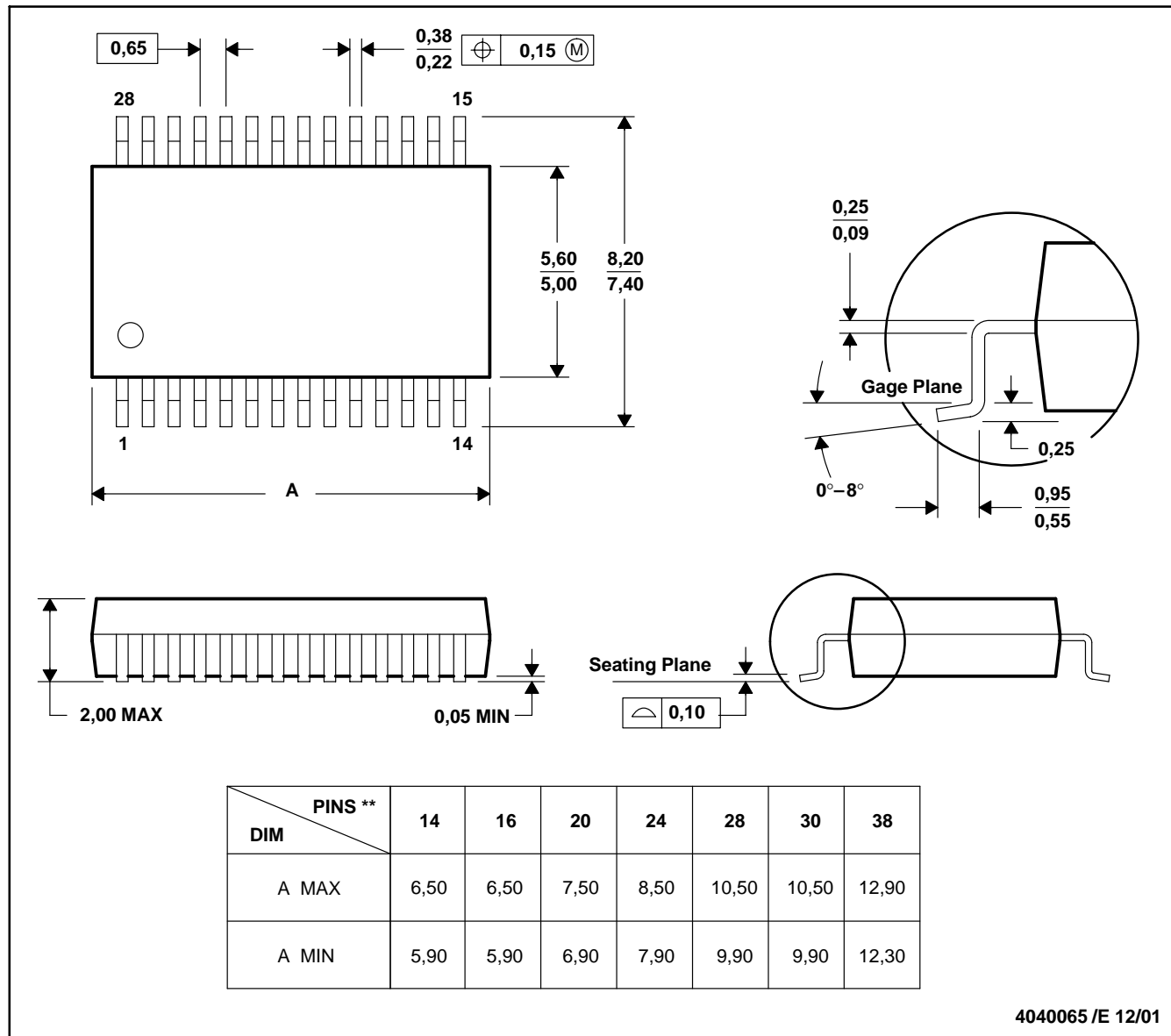
MECHANICAL DATA

MSS0002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - Falls within JEDEC MO-150

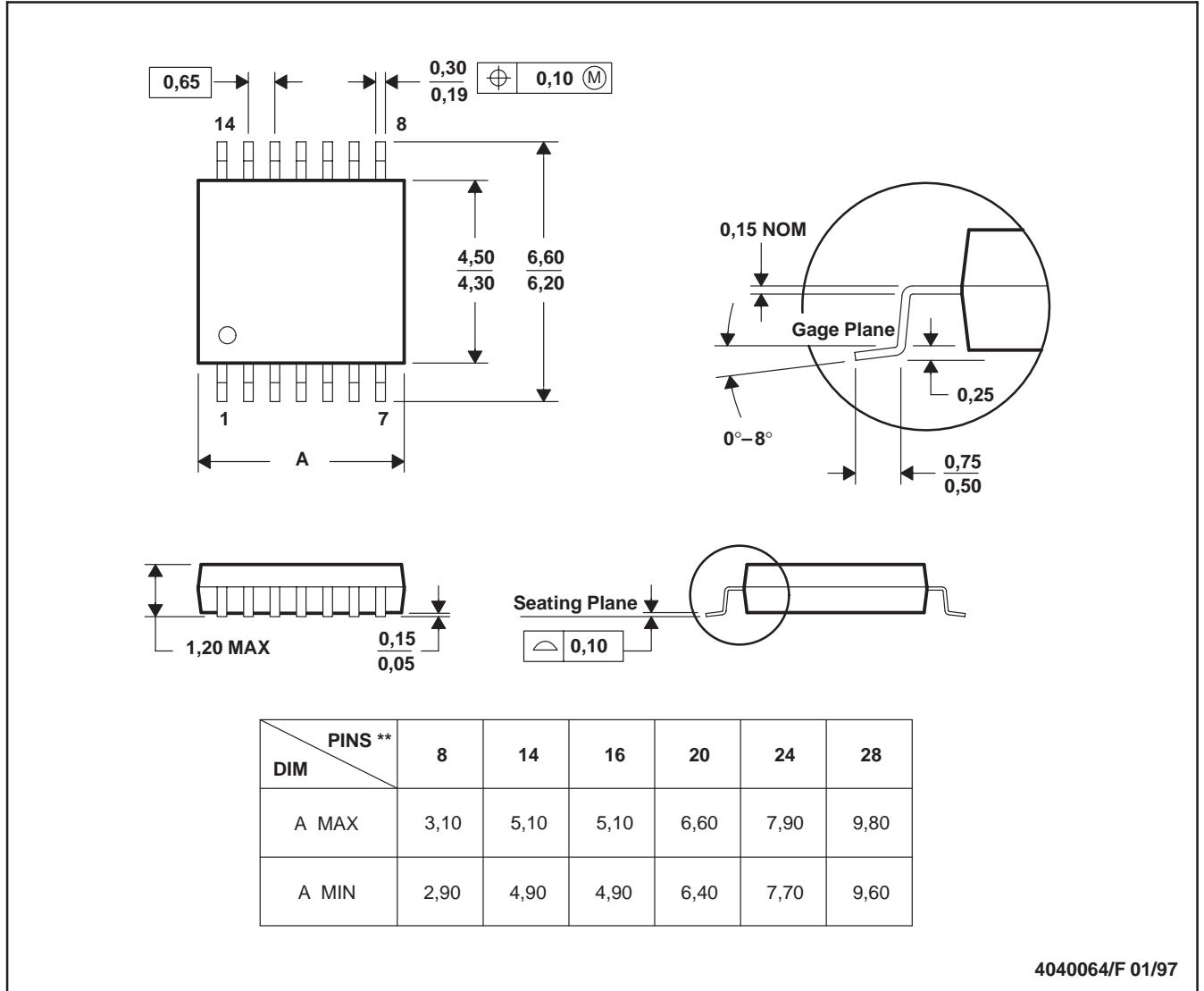
MECHANICAL DATA

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

PW (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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