



March 2001
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SSTV16859

Dual Output 13-Bit Register with SSTL-2 Compatible I/O and Reset

General Description

The SSTV16859 is a dual output 13-bit register designed for use with 184 and 232 pin DDR-1 memory modules. The device has a differential input clock, SSTL-2 compatible data inputs and a LVCMOS compatible RESET input. The device has been designed to meet the JEDEC DDR module register specifications.

The device has been fabricated on an advanced sub-micron CMOS process and is designed to operate at power supplies of less than 3.6V's.

Features

- Compliant with DDR-I registered module specifications
- Operates at $2.5V \pm 0.2V V_{DD}$
- SSTL-2 compatible input structure
- SSTL-2 compliant output structure
- Differential SSTL-2 compatible clock inputs
- Low power mode when device is reset
- Industry standard 64 pin TSSOP package
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

Ordering Code:

| Order Number | Package Number | Package Description |
|--------------------------------|----------------|---|
| SSTV16859G (Note 1)(Note 2) | BGA96A | 96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide |
| SSTV16859MTD (Note 2) | MTD64 | 64-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |

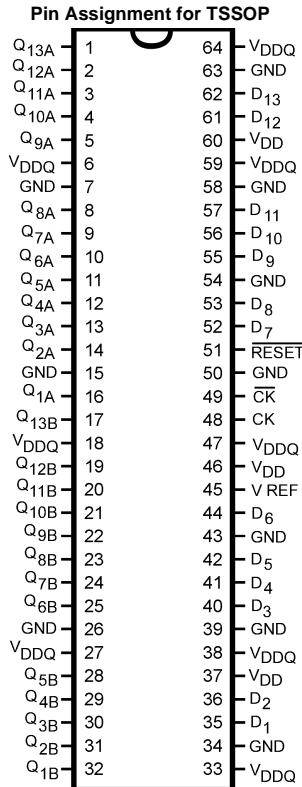
Note 1: Ordering code "G" indicates Trays.

Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

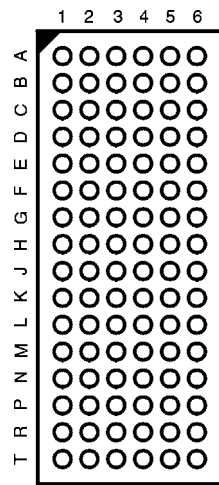
SSTV16859 Dual Output 13-Bit Register with SSTL-2 Compatible I/O and Reset



Connection Diagrams



Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

| Pin Name | Description |
|--|---|
| Q _{1A} -Q _{13A} Q _{1B} -Q _{13B} | SSTL-2 Compatible Register Outputs |
| D ₁ -D ₁₃ | SSTL-2 Compatible Register Inputs |
| RESET | Asynchronous LVCMOS Reset Input |
| CK | Positive Master Clock Input |
| CK | Negative Master Clock Input |
| V _{REF} | Voltage Reference Pin for SSTL level inputs |
| V _{DDQ} | Power Supply Voltage for Output Signals |
| V _{DD} | Power Supply Voltage for Inputs |
| NC | Electrically Isolated No Connect |

FBGA Pin Assignments

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|------------------|------------------|------------------|------------------|-----------------|-----------------|
| A | NC | NC | NC | NC | NC | NC |
| B | Q _{12A} | Q _{13A} | GND | GND | NC | NC |
| C | Q _{10A} | Q _{11A} | GND | GND | NC | NC |
| D | Q _{8A} | Q _{9A} | V _{DDQ} | V _{DDQ} | D ₁₃ | D ₁₂ |
| E | Q _{6A} | Q _{7A} | V _{DDQ} | V _{DD} | D ₁₁ | D ₁₀ |
| F | Q _{4A} | Q _{5A} | V _{DDQ} | V _{DD} | D ₉ | D ₈ |
| G | Q _{2A} | Q _{3A} | GND | GND | D ₇ | RESET |
| H | Q _{1A} | Q _{13B} | GND | GND | NC | CK |
| J | Q _{12B} | Q _{11B} | GND | V _{REF} | NC | CK |
| K | Q _{10B} | Q _{9B} | V _{DDQ} | V _{DD} | NC | NC |
| L | Q _{8B} | Q _{7B} | V _{DDQ} | V _{DD} | D ₅ | D ₆ |
| M | Q _{6B} | Q _{5B} | V _{DDQ} | V _{DDQ} | D ₃ | D ₄ |
| N | Q _{4B} | Q _{3B} | GND | GND | D ₁ | D ₂ |
| P | Q _{2B} | Q _{1B} | GND | GND | NC | NC |
| R | NC | NC | NC | NC | NC | NC |
| T | NC | NC | NC | NC | NC | NC |

Truth Table

| RESET | D _n | CK | CK | Q _n |
|-------|----------------|---------------|---------------|------------------|
| L | X or Floating | X or Floating | X or Floating | L |
| H | L | ↑ | ↓ | L |
| H | H | ↑ | ↓ | H |
| H | X | L | H | Q _{n-1} |
| H | X | H | L | Q _{n-1} |

L = Logic LOW
H = Logic HIGH
X = Don't Care but not floating unless noted
↑ = LOW-to-HIGH Clock Transition
↓ = HIGH-to-LOW Clock Transition
Q_{n-1} = Output Remains in Previously Clocked State

Functional Description

The SSTV16859 is a 13-bit dual register with SSTL-2 compatible inputs and outputs. Input data is transferred to output data on the rising edge of the differential clock pair. When the $\overline{\text{RESET}}$ signal is asserted LOW all outputs are placed into the LOW logic state and all input comparators are disabled for power savings. Output glitches are prevented by disabling the internal registers more quickly than the input comparators. When $\overline{\text{RESET}}$ is removed, the system designer must insure the clock and data inputs to the

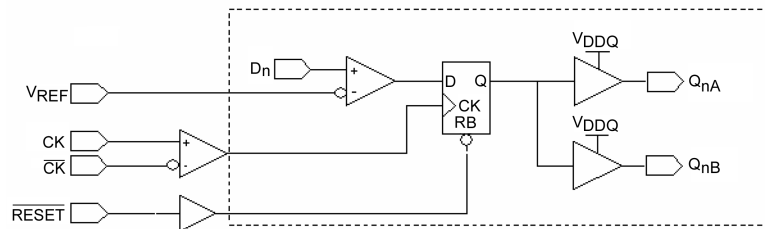
device are stable during the rising transition of the $\overline{\text{RESET}}$ signal.

The SSTL-2 data inputs transition based on the value of V_{REF} . V_{REF} is a stable system reference used for setting the trip point of the input buffers of the SSTV16859 and other SSTL-2 compatible devices.

The $\overline{\text{RESET}}$ signal is a standard CMOS compatible input and is not referenced to the V_{REF} signal.

Logic Diagram

For $n = 1$ to 13



Absolute Maximum Ratings (Note 3)

| | |
|--|---------------------------|
| Supply Voltage (V_{DDQ}) | -0.5V to +3.6V |
| Supply Voltage (V_{DD}) | -0.5V to +3.6V |
| Reference Voltage (V_{REF}) | -0.5V to +3.6V |
| Input Voltage (V_I) | -0.5V to $V_{DD} + 0.5V$ |
| Output Voltage (V_O) | |
| Outputs Active (Note 4) | -0.5V to $V_{DDQ} + 0.5V$ |
| DC Input Diode Current (I_{IK}) | |
| $V_I < 0V$ | -50 mA |
| $V_I > V_{DD}$ | +50 mA |
| DC Output Diode Current (I_{OK}) | |
| $V_O < 0V$ | -50 mA |
| $V_O > V_{DDQ}$ | +50 mA |
| DC Output Source/Sink Current (I_{OH}/I_{OL}) | ±50 mA |
| DC V_{DD} or Ground Current per Supply Pin (I_{DD} or Ground) | ±100 mA |
| Storage Temperature Range (T_{stg}) | -65°C to +150°C |
| ESD (Human Body Model) | ≥ 7000V |

Recommended Operating Conditions (Note 5)

| | |
|--|---------------------|
| Power Supply (V_{DDQ}) | 2.3V to 2.7V |
| Power Supply (V_{DD}) | |
| Operating Range | V_{DDQ} to 2.7V |
| Reference Supply ($V_{REF} = V_{DDQ}/2$) | 1.15 to 1.35 |
| Termination Voltage (V_{TT}) | $V_{REF} \pm 40$ mV |
| Input Voltage | 0 to V_{DD} |
| Output Voltage (V_O) | |
| Output in Active States | 0V to V_{DDQ} |
| Output Current I_{OH}/I_{OL} | |
| $V_{DD} = 2.3V$ to 2.7V | ±20 mA |
| Free Air Operating Temperature (T_A) | 0°C to +70°C |

Note 3: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: IO Absolute Maximum Rating must be observed.

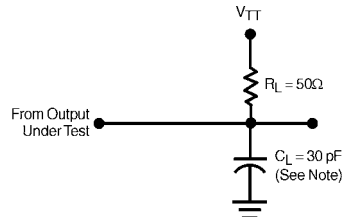
Note 5: The RESET input of the device must be held at V_{DD} or GND to ensure proper device operation. The differential inputs must not be floating, unless RESET is asserted LOW.

DC Electrical Characteristics ($2.3V \leq V_{DD} \leq 2.7V$)

| Symbol | Parameter | Conditions | V_{DD} (V) | Min | Typ | Max | Units |
|-------------|--|---|-------------------|------------------------|-----|--------------------|-------------|
| V_{IKL} | Input LOW Clamp Voltage | $I_I = -18$ mA | 2.3 | | | -1.2 | V |
| V_{IKH} | Input HIGH Clamp Voltage | $I_I = +18$ mA | 2.3 | | | 3.5 | V |
| V_{IH-AC} | AC HIGH Level Input Voltage | Data Inputs | | $V_{REF} + 310$ mV | | | V |
| V_{IL-AC} | AC LOW Level Input Voltage | Data Inputs | | | | $V_{REF} - 310$ mV | V |
| V_{IH-DC} | DC HIGH Level Input Voltage | Data Inputs | | $V_{REF} + 150$ mV | | | V |
| V_{IL-DC} | DC LOW Level Input Voltage | Data Inputs | | | | $V_{REF} - 150$ mV | V |
| V_{IH} | HIGH Level Input Voltage | RESET | | 1.7 | | | V |
| V_{IL} | LOW Level Input Voltage | RESET | | | | 0.7 | V |
| V_{ICR} | Common Mode Input Voltage Range | CK, \overline{CK} | | 0.97 | | 1.53 | V |
| $V_{I(PP)}$ | Peak to Peak Input Voltage | CK, \overline{CK} | | 360 | | | mV |
| V_{OH} | HIGH Level Output Voltage | $I_{OH} = -100$ μ A $I_{OH} = -16$ mA | 2.3 to 2.7 2.3 | $V_{DD} - 0.2$ 1.95 | | | V |
| V_{OL} | LOW Level Output Voltage | $I_{OL} = 100$ μ A $I_{OL} = 16$ mA | 2.3 to 2.7 2.3 | | | 0.2 0.35 | V |
| I_I | Input Leakage Current | $V_I = V_{DD}$ or GND | 2.7 | | | ±5.0 | μ A |
| I_{DD} | Static Standby | RESET = GND, $I_O = 0$ | 2.7 | | | 10 | μ A |
| | Static Operating | RESET = V_{DD} , $I_O = 0$ $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ | | | | 25 | mA |
| I_{DD} | Dynamic Operating Current Clock Only | RESET = V_{DD} , $I_O = 0$ $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ CK, \overline{CK} Duty Cycle 50% | 2.7 | | | 120 | μ A/MHz |
| | Dynamic Operating Current per Data Input | RESET = V_{DD} , $I_O = 0$ $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ CK, \overline{CK} Duty Cycle 50% Data Input = 1/2 Clock Rate 50% Duty Cycle | | | | 15 | μ A/MHz |

| DC Electrical Characteristics (Continued) | | | | | | | |
|--|---|---|------------------------|-----|-------|--|-------|
| Symbol | Parameter | Conditions | V _{DD} (V) | Min | Typ | Max | Units |
| R _{OH} | Output HIGH On Resistance | I _{OH} = -20 mA | 2.3 to 2.7 | 7 | | 20 | Ω |
| R _{OL} | Output LOW On Resistance | I _{OL} = 20 mA | 2.3 to 2.7 | 7 | | 20 | Ω |
| R _{OΔ} | R _{OH} - R _{OL} | I _O = 20 mA, T _A = 25°C | 2.5 | | | 4 | Ω |
| AC Electrical Characteristics (Note 6) | | | | | | | |
| Symbol | Parameter | T _A = 0°C to +70°C, C _L = 30 pF, R _L = 50Ω | | | Units | | |
| | | V _{DD} = 2.5V ± 0.2V; V _{DDQ} = 2.5V ± 0.2V | | | | | |
| | | Min | Typ | Max | | | |
| f _{MAX} | Maximum Clock Frequency | | 200 | | | | MHz |
| t _W | Pulse Duration, CK, $\overline{\text{CK}}$ HIGH or LOW (Figure 2) | | 2.5 | | | | ns |
| t _{ACT} (Note 7) | Differential Inputs Activation Time, data inputs must be LOW after $\overline{\text{RESET}}$ HIGH (Figure 3) | | 22 | | | | ns |
| t _{INACT} (Note 7) | Differential Inputs De-activation Time, data and clock inputs must be held at valid levels (not floating) after $\overline{\text{RESET}}$ LOW | | 22 | | | | ns |
| t _S | Setup Time, Fast Slew Rate (Note 8)(Note 9) (Figure 5) | | 0.75 | | | | ns |
| | Setup Time, Slow Slew Rate (Note 9)(Note 10) (Figure 5) | | 0.9 | | | | |
| t _H | Hold Time, Fast Slew Rate (Note 8)(Note 10) (Figure 5) | | 0.75 | | | | ns |
| | Hold Time, Slow Slew Rate (Note 9)(Note 10) (Figure 5) | | 0.9 | | | | |
| t _{REM} | Reset Removal Time (Figure 7) | | 10 | | | | ns |
| t _{PHL} , t _{PLH} | Propagation Delay CK, $\overline{\text{CK}}$ to Q _n (Figure 4) | | 1.1 | | | 2.8 | ns |
| t _{PHL} | Propagation Delay $\overline{\text{RESET}}$ to Q _n (Figure 6) | | | | | 5.0 | ns |
| <p>Note 6: Refer to Figure 1 through Figure 7.</p> <p>Note 7: This parameter is not production tested.</p> <p>Note 8: For data signal input slew rate ≥ 1 V/ns.</p> <p>Note 9: For data signal input slew rate ≥ 0.5 V/ns and < 1 V/ns.</p> <p>Note 10: For CK, $\overline{\text{CK}}$ signals input slew rates are ≥ 1 V/ns.</p> | | | | | | | |
| Capacitance (Note 11) | | | | | | | |
| Symbol | Parameter | Min | Typ | Max | Units | Conditions | |
| C _{IN} | Data Pin Input Capacitance | 2.2 | | 3.2 | pF | V _{DD} = 2.5V, V _I = V _{REF} ± 310 mV | |
| | CK, $\overline{\text{CK}}$ - Input Capacitance | 2.2 | | 3.2 | pF | V _{DD} = 2.5V, V _{ICR} = 1.25, V _{I(PP)} = 360 mV | |
| | $\overline{\text{RESET}}$ | 2.3 | | 3.3 | pF | V _{DD} = 2.5V, V _I = V _{DD} or GND | |
| <p>Note 11: T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.</p> | | | | | | | |

AC Loading and Waveforms (See Notes A through F below)



Note: C_L includes probe and jig capacitance

FIGURE 1. AC Test Circuit

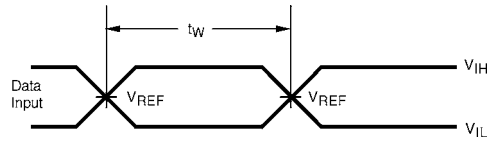
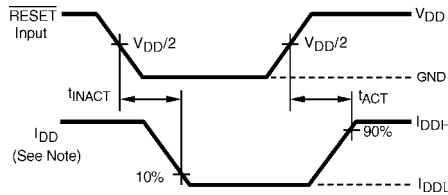


FIGURE 2. Voltage Waveforms - Pulse Duration



Note: I_{DD} tested with clock and data inputs held at V_{DD} or GND, and $I_O = 0$ mA.

FIGURE 3. Voltage and Current Waveforms Inputs Active and Inactive Times

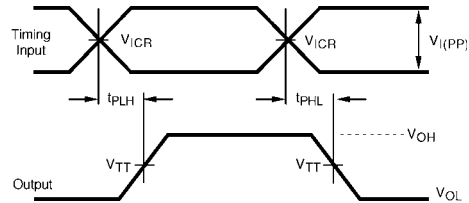


FIGURE 4. Voltage Waveforms - Propagation Delay Times

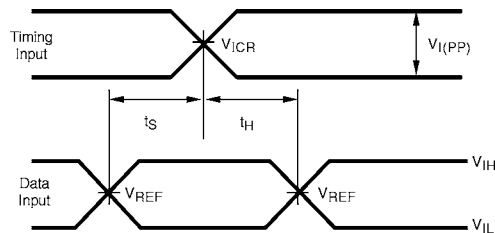


FIGURE 5. Voltage Waveforms - Setup and Hold Times

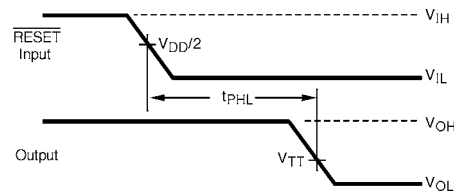


FIGURE 6. Voltage Waveforms - RESET Propagation Delay Times

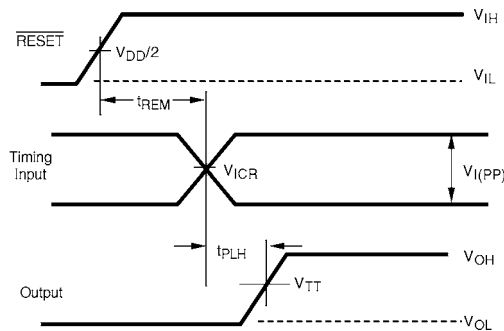


FIGURE 7. Voltage Waveforms - RESET Removal Delay Times

Note A: All input pulses are supplied by generators having the following characteristics:

PRR \leq 10 MHz, $Z_0 = 50\Omega$, input slew rate = 1V/ns \pm 20% (unless otherwise specified).

Note B: The outputs are measured one at a time with one transition per measurement.

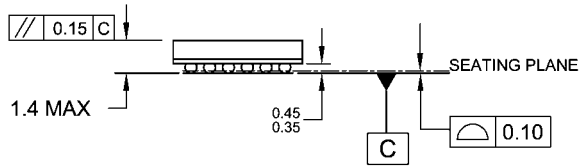
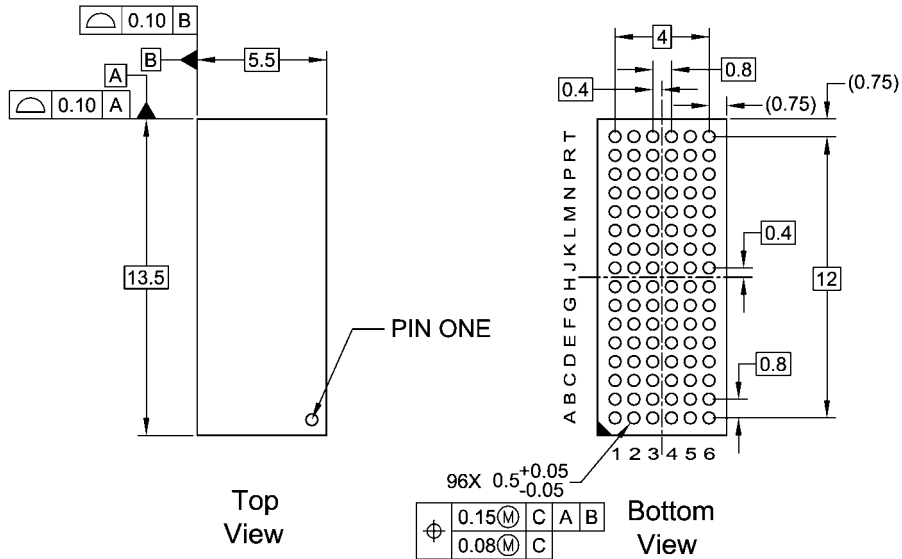
Note C: $V_{TT} = V_{REF} = V_{DD}/2$.

Note D: $V_{IH} = V_{REF} + 310$ mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS input.

Note E: $V_{IL} = V_{REF} - 310$ mV (AC voltage levels) for differential inputs. $V_{IL} = GND$ for LVCMOS input.

Note F: Removal time (t_{REM}) is tested with one data input held active HIGH. The propagation time from CK to the corresponding output must meet valid timing specifications for the measurement to be accurate.

Physical Dimensions inches (millimeters) unless otherwise noted

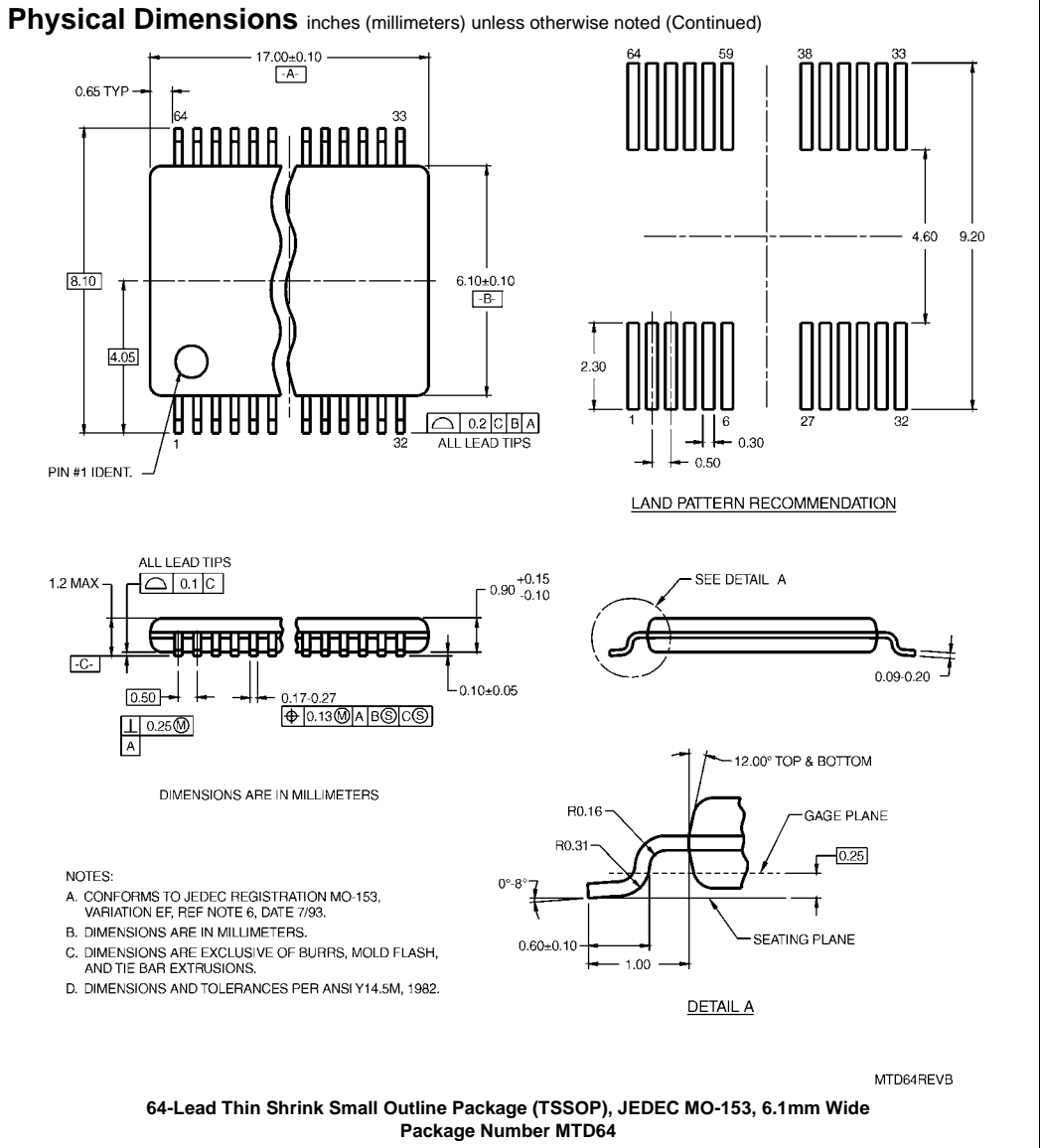


NOTES:

- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA96ArevE

**96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC M0-205, 5.5mm Wide
Package Number BGA96A**



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