



CYPRESS

CY7C186

8Kx8 Static RAM

Features

- High speed
 - 20 ns
- Low active power
 - 605 mW
- Low standby power
 - 110 mW
- CMOS for optimum speed/power
- Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

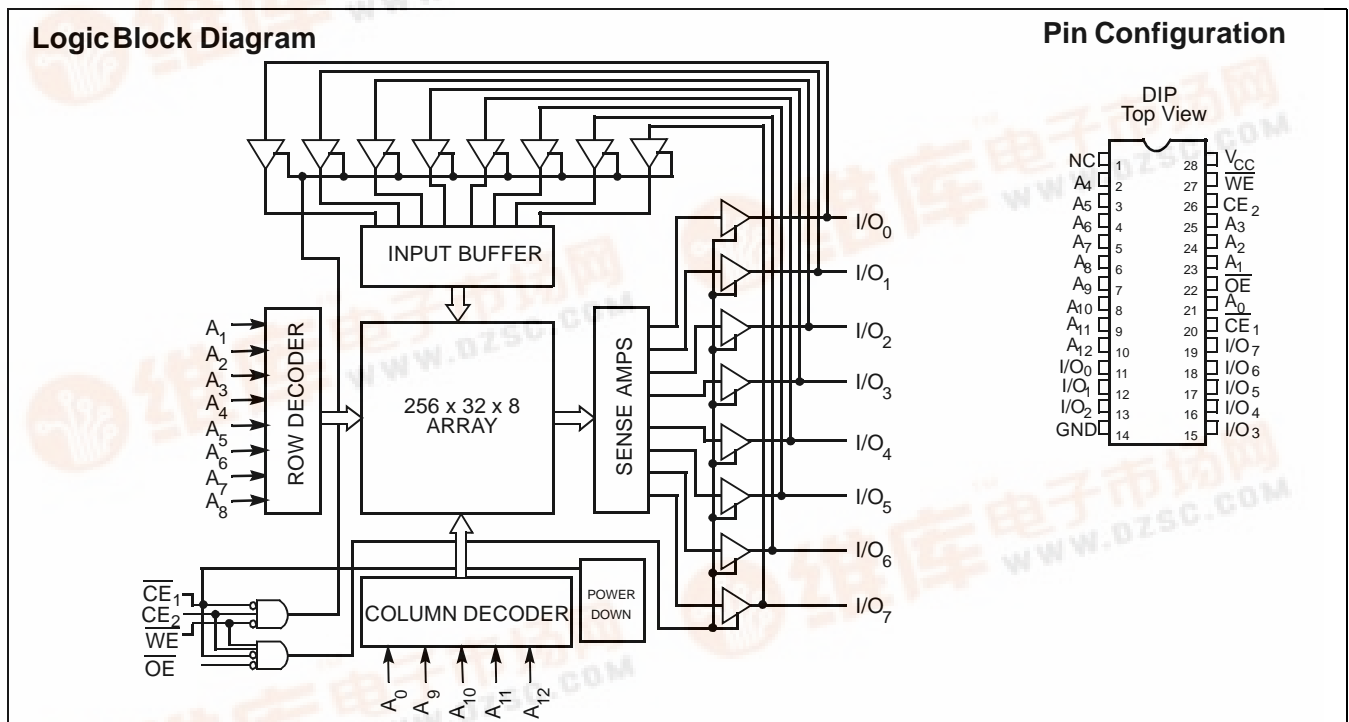
Functional Description

The CY7C186 is a high-performance CMOS static RAM organized as 8192 words by 8 bits. Easy memory expansion is

provided by an active LOW chip enable (\overline{CE}_1), an active HIGH chip enable (CE_2), and active LOW output enable (\overline{OE}) and three-state drivers. The device has an automatic power-down feature (\overline{CE}_1), reducing the power consumption by over 80% when deselected. The CY7C186 is in a 600-mil-wide PDIP package and a 32-pin TSOP (std. pinout).

An active LOW write enable signal (\overline{WE}) controls the writing/reading operation of the memory. When \overline{CE}_1 and \overline{WE} inputs are both LOW and CE_2 is HIGH, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, \overline{CE}_1 and \overline{OE} active LOW, CE_2 active HIGH, while \overline{WE} remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable (\overline{WE}) is HIGH. A die coat is used to insure alpha immunity.

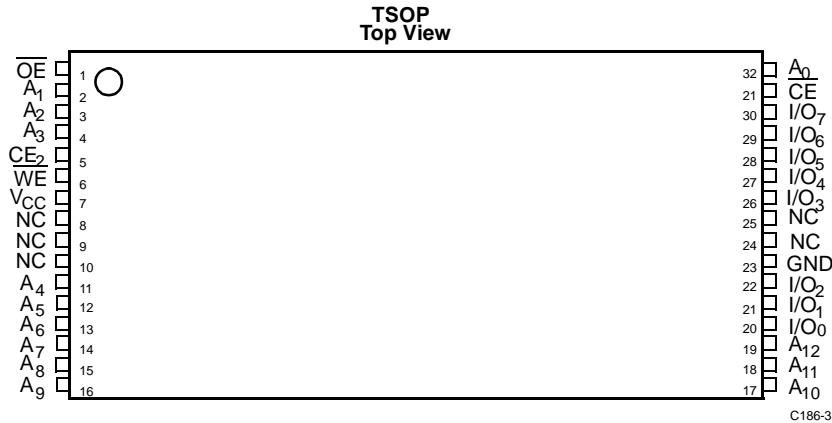


Selection Guide^[1]

| | 7C186-20 | 7C186-25 | 7C186-35 |
|--------------------------------|----------|----------|----------|
| Maximum Access Time (ns) | 20 | 25 | 35 |
| Maximum Operating Current (mA) | 110 | 100 | 100 |
| Maximum Standby Current (mA) | 20/15 | 20/15 | 20/15 |

Notes:
For military specifications, see the CY7C186A datasheet.



Pin Configurations (continued)


C186-3

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage to Ground Potential -0.5V to +7.0V

 DC Voltage Applied to Outputs in High Z State^[2] -0.5V to +7.0V

 DC Input Voltage^[2] -0.5V to +7.0V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

| Range | Ambient Temperature | V _{CC} |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C | 5V ± 10% |

Electrical Characteristics Over the Operating Range

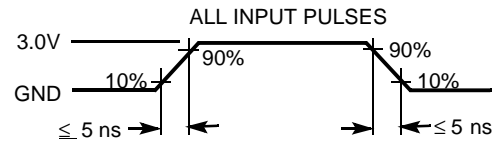
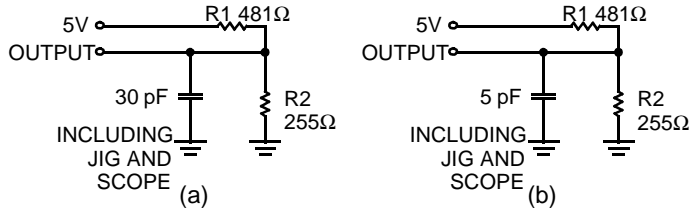
| Parameter | Description | Test Conditions | 7C186-20 | | 7C186-25,35 | | Unit |
|------------------|--|---|----------|-----------------|-------------|-----------------|------|
| | | | Min. | Max. | Min. | Max. | |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., I _{OH} = -4.0 mA | 2.4 | | 2.4 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., I _{OL} = 8.0 mA | | 0.4 | | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2.2 | V _{CC} | 2.2 | V _{CC} | V |
| V _{IL} | Input LOW Voltage ^[2] | | -0.5 | 0.8 | -0.5 | 0.8 | V |
| I _{Ix} | Input Load Current | GND ≤ V _I ≤ V _{CC} | -5 | +5 | -5 | +5 | μA |
| I _{OZ} | Output Leakage Current | GND ≤ V _I ≤ V _{CC} , Output Disabled | -5 | +5 | -5 | +5 | μA |
| I _{OS} | Output Short Circuit Current ^[3] | V _{CC} = Max., V _{OUT} = GND | | -300 | | -300 | mA |
| I _{CC} | V _{CC} Operating Supply Current | V _{CC} = Max., I _{OUT} = 0 mA | | 110 | | 100 | mA |
| I _{SB1} | Automatic CE ₁ Power-Down Current | Max. V _{CC} , CE ₁ ≥ V _{IH} , Min. Duty Cycle=100% | | 20 | | 20 | mA |
| I _{SB2} | Automatic CE ₁ Power-Down Current | Max. V _{CC} , CE ₁ ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V | | 15 | | 15 | mA |

Capacitance^[4]

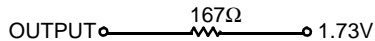
| Parameter | Description | Test Conditions | Max. | Unit |
|------------------|--------------------|-----------------------------------|------|------|
| C _{IN} | Input Capacitance | T _A = 25°C, f = 1 MHz, | 7 | pF |
| C _{OUT} | Output Capacitance | V _{CC} = 5.0V | 7 | pF |

Notes:

- Minimum voltage is equal to -3.0V for pulse durations less than 30 ns.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms


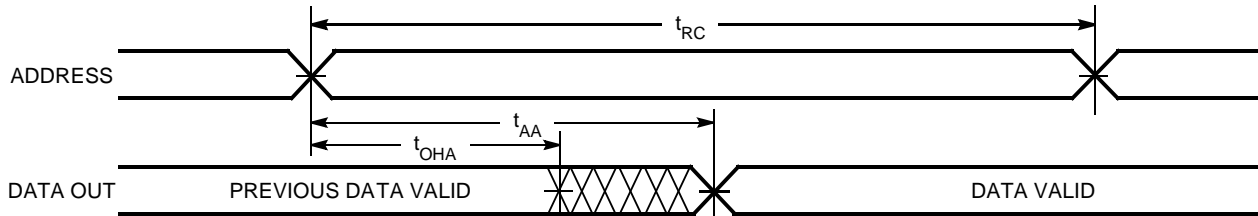
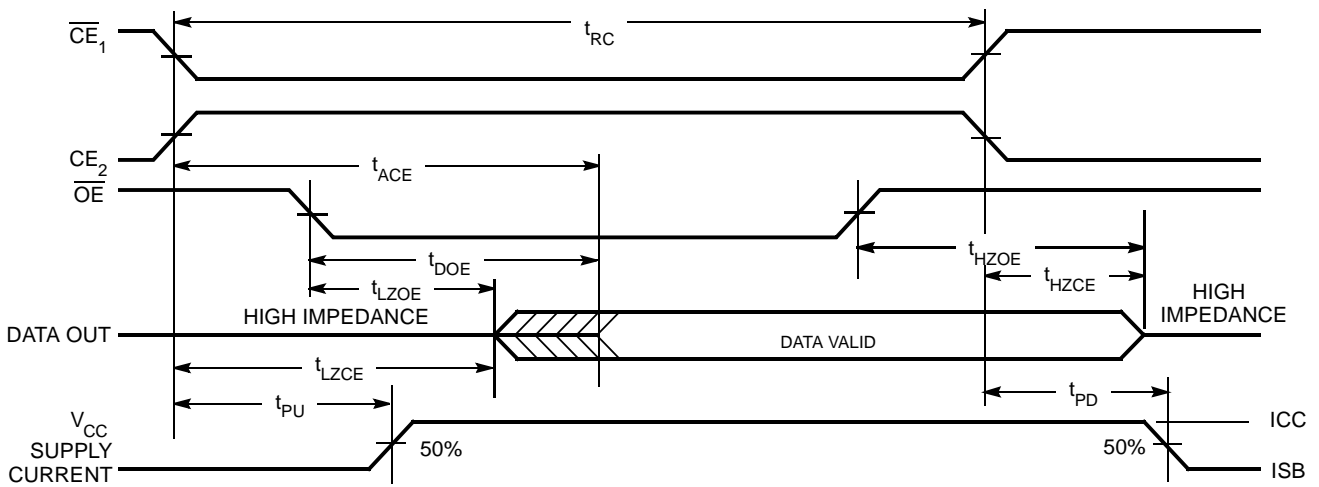
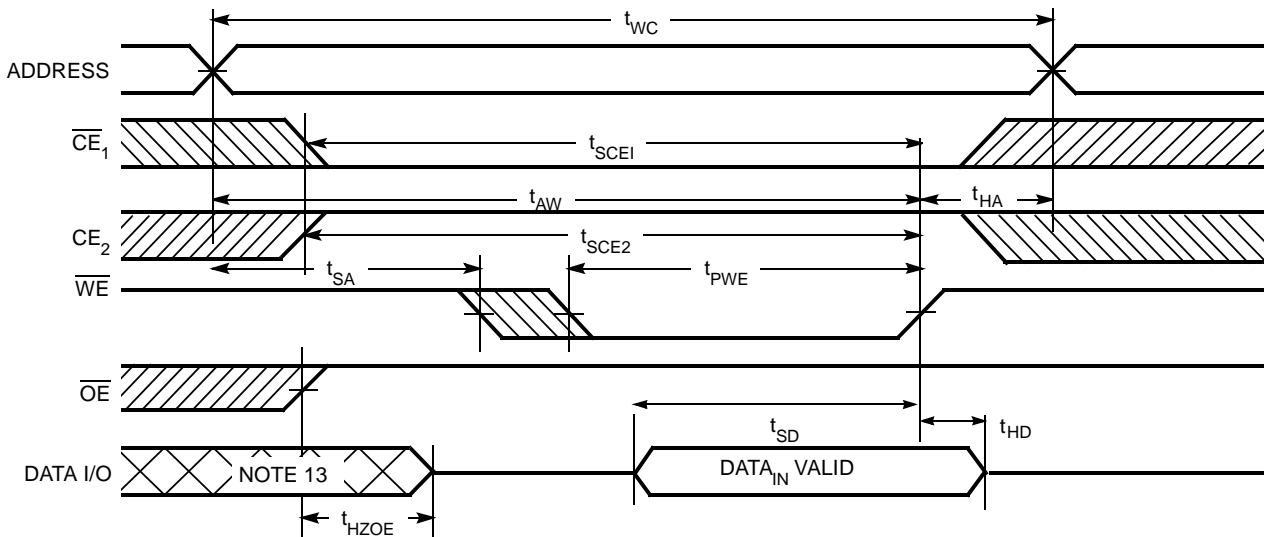
Equivalent to: THÉVENIN EQUIVALENT


Switching Characteristics Over the Operating Range^[5]

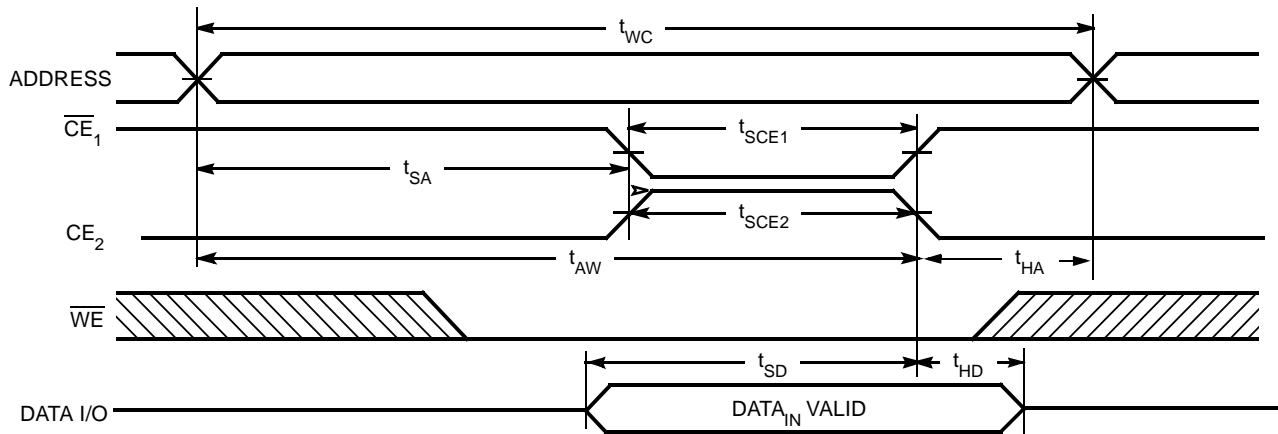
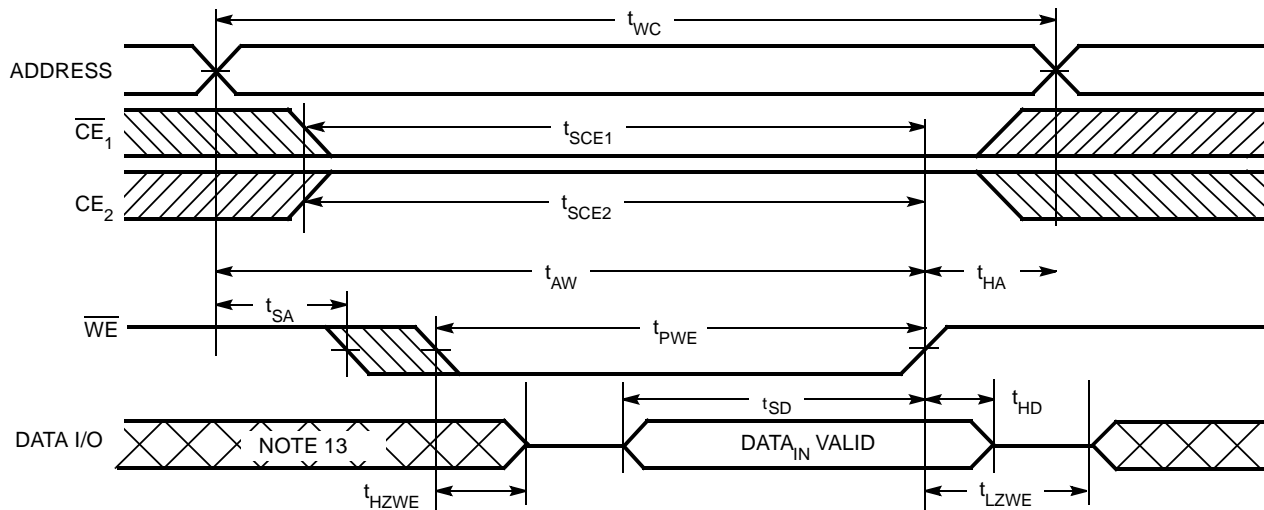
| Parameter | Description | 7C186-20 | | 7C186-25 | | 7C186-35 | | Unit |
|----------------------------------|--|----------|------|----------|------|----------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | |
| t_{RC} | Read Cycle Time | 20 | | 25 | | 35 | | ns |
| t_{AA} | Address to Data Valid | | 20 | | 25 | | 35 | ns |
| t_{OHA} | Data Hold from Address Change | 5 | | 5 | | 5 | | ns |
| t_{ACE1} | \overline{CE}_1 LOW to Data Valid | | 20 | | 25 | | 35 | ns |
| t_{ACE2} | CE_2 HIGH to Data Valid | | 20 | | 25 | | 35 | ns |
| t_{DOE} | \overline{OE} LOW to Data Valid | | 9 | | 12 | | 15 | ns |
| t_{LZOE} | \overline{OE} LOW to Low Z | 3 | | 3 | | 3 | | ns |
| t_{HZOE} | \overline{OE} HIGH to High Z ^[6] | | 8 | | 10 | | 10 | ns |
| t_{LZCE1} | \overline{CE}_1 LOW to Low Z ^[7] | 5 | | 5 | | 5 | | ns |
| t_{LZCE2} | CE_2 HIGH to Low Z | 3 | | 3 | | 3 | | ns |
| t_{HZCE} | \overline{CE}_1 HIGH to High Z ^[6, 7] CE_2 LOW to High Z | | 8 | | 10 | | 10 | ns |
| t_{PU} | \overline{CE}_1 LOW to Power-Up | 0 | | 0 | | 0 | | ns |
| t_{PD} | \overline{CE}_1 HIGH to Power-Down | | 20 | | 20 | | 20 | ns |
| WRITE CYCLE^[8] | | | | | | | | |
| t_{WC} | Write Cycle Time | 20 | | 25 | | 35 | | ns |
| t_{SCE1} | \overline{CE}_1 LOW to Write End | 15 | | 20 | | 20 | | ns |
| t_{SCE2} | CE_2 HIGH to Write End | 15 | | 20 | | 20 | | ns |
| t_{AW} | Address Set-Up to Write End | 15 | | 20 | | 25 | | ns |
| t_{HA} | Address Hold from Write End | 0 | | 0 | | 0 | | ns |
| t_{SA} | Address Set-Up to Write Start | 0 | | 0 | | 0 | | ns |
| t_{PWE} | \overline{WE} Pulse Width | 15 | | 15 | | 20 | | ns |
| t_{SD} | Data Set-Up to Write End | 10 | | 10 | | 12 | | ns |
| t_{HD} | Data Hold from Write End | 0 | | 0 | | 0 | | ns |
| t_{HZWE} | \overline{WE} LOW to High Z ^[6] | | 7 | | 7 | | 8 | ns |
| t_{LZWE} | \overline{WE} HIGH to Low Z | 5 | | 5 | | 5 | | ns |

Notes:

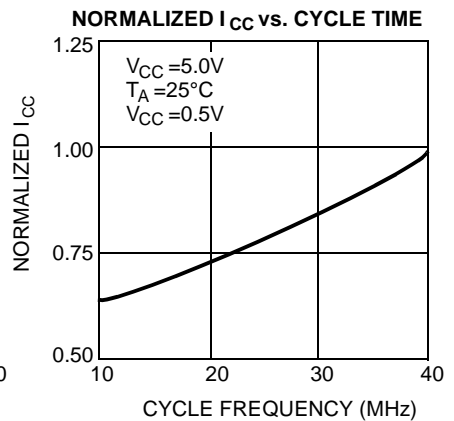
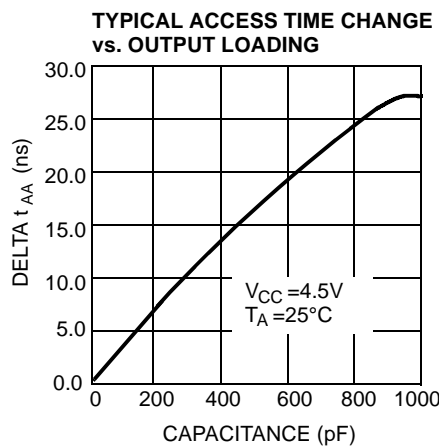
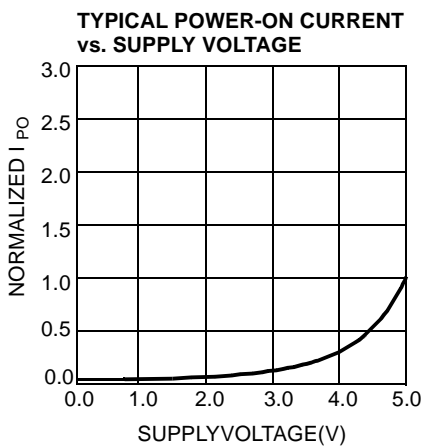
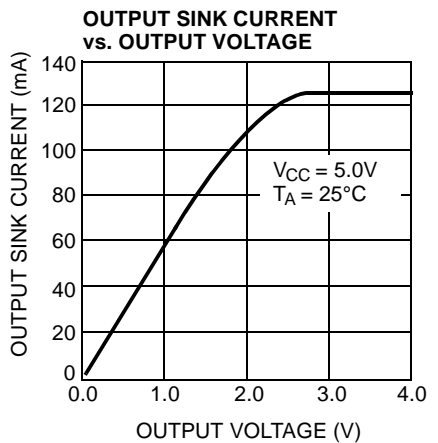
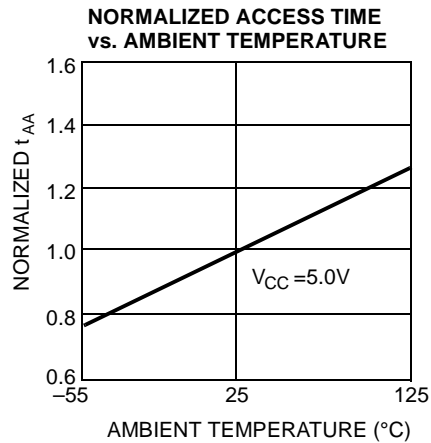
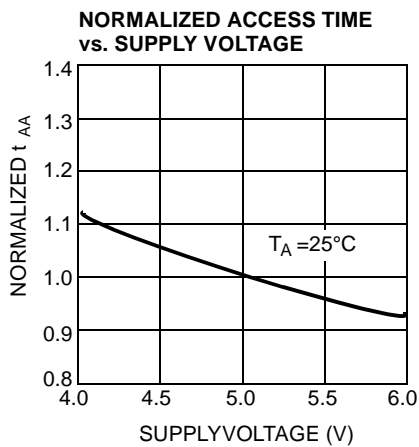
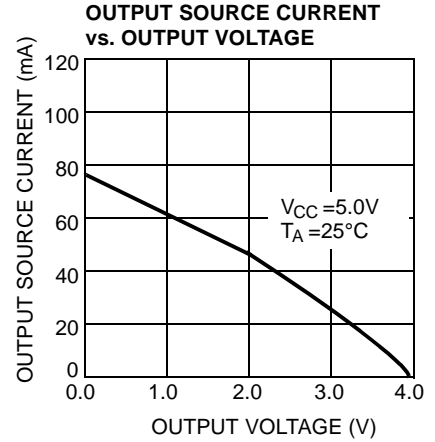
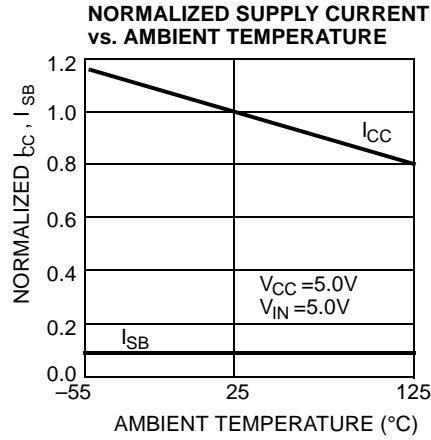
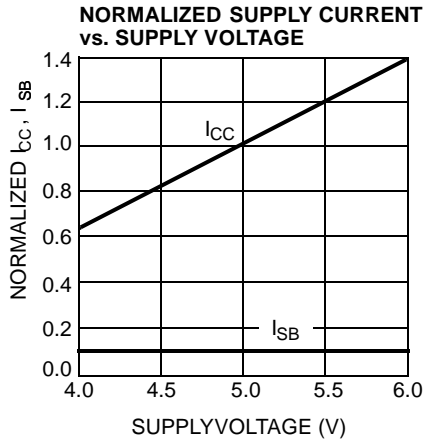
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW. All signals must be active to initiate a write, and any signal can terminate a write by going inactive. The data input set-up and hold timing should be referenced to the trailing edge of the signal that terminates the write.

Switching Waveforms
Read Cycle No. 1^[9]

Read Cycle No. 2^[10, 11]

Write Cycle No. 1 (WE Controlled)^[11, 12]

Notes:

9. Device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$. $CE_2 = V_{IH}$.
10. WE is HIGH for read cycle.
11. Data I/O is High Z if $\overline{OE} = V_{IH}$, $\overline{CE}_1 = V_{IH}$, or $\overline{WE} = V_{IL}$.
12. Address valid prior to or coincident with \overline{CE}_1 transition LOW and CE_2 transition HIGH.
13. During this period, the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)
Write Cycle No. 2 (\overline{CE} Controlled)^[11,12,14]

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[11, 14]

Notes:

14. If \overline{CE}_1 goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics


Truth Table

| CE ₁ | CE ₂ | WE | OE | Input/Output | Mode |
|-----------------|-----------------|----|----|--------------|---------------------|
| H | X | X | X | High Z | Deselect/Power-Down |
| X | L | X | X | High Z | Deselect |
| L | H | H | L | Data Out | Read |
| L | H | L | X | Data In | Write |
| L | H | H | H | High Z | Deselect |

Address Designators

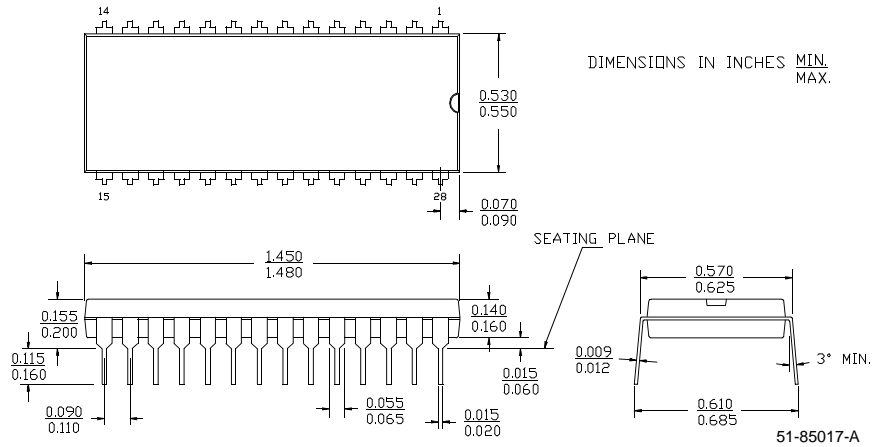
| Address Name | Address Function | DIP Pin Number | TSOP Pin Number |
|--------------|------------------|----------------|-----------------|
| A4 | X3 | 2 | 11 |
| A5 | X4 | 3 | 12 |
| A6 | X5 | 4 | 13 |
| A7 | X6 | 5 | 14 |
| A8 | X7 | 6 | 15 |
| A9 | Y1 | 7 | 16 |
| A10 | Y4 | 8 | 17 |
| A11 | Y3 | 9 | 18 |
| A12 | Y0 | 10 | 19 |
| A0 | Y2 | 21 | 32 |
| A1 | X0 | 23 | 2 |
| A2 | X1 | 24 | 3 |
| A3 | X2 | 25 | 4 |

Ordering Information

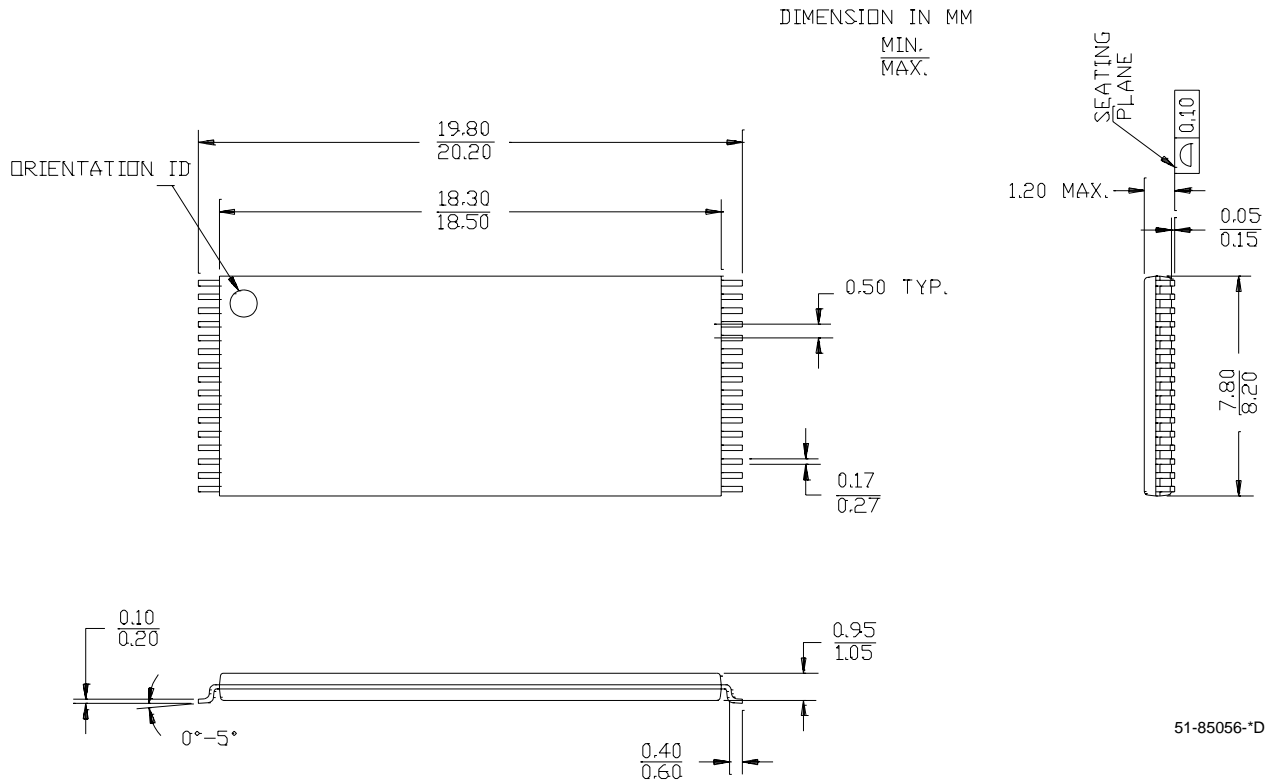
| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|---------------|--------------|------------------------------------|-----------------|
| 20 | CY7C186-20PC | P15 | 28-Lead (600-Mil) Molded DIP | Commercial |
| | CY7C186-20ZC | Z32 | 32-Lead Thin Small Outline Package | |
| 25 | CY7C186-25PC | P15 | 28-Lead (600-Mil) Molded DIP | Commercial |
| 35 | CY7C186-35PC | P15 | 28-Lead (600-Mil) Molded DIP | Commercial |

Package Diagrams

28-Lead (600-Mil) Molded DIP P15



32-Lead Thin Small Outline Package Type I (8x20 mm) Z32





| Document Title: CY7C186 8Kx8 Static RAM Document Number: 38-05280 | | | | |
|--|----------------|-------------------|------------------------|---|
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 114447 | 3/26/02 | DSG | Change from Spec number: 38-00240 to 38-05280 |