



# LC86P7248

## 8-Bit Single-Chip Microcontroller with the One-Time Programmable PROM Built in

### Preliminary

#### Overview

The LC86P7248 is a CMOS 8-bit single chip microcontroller with one-time PROM for the LC867200 series. This microcontroller has the function and the pin description of the LC867200 series mask ROM version, and 48K-byte EPROM.

QIP package are available for shipping as well as LC867200 series. It is suitable to set up first release, prototyping, developing and testing of set.

#### Features

- (1) Option switching by PROM data

The option function of the LC867200 series can be specified by the PROM data.

LC86P7248 can be checked the functions of the trial pieces using the mass production board.

- (2) Internal one-time PROM capacity : 49408 bytes
- (3) Internal RAM capacity : 1152 bytes

Used PROM or RAM capacity are equal ROM or RAM capacity of mask ROM version which applies LC86P7248.

Mask ROM version	EPROM capacity	RAM capacity
LC867248	49152 bytes	1152 bytes
LC867240	40960 bytes	1152 bytes
LC867232	32768 bytes	1152 bytes
LC867224	24576 bytes	1152 bytes

#### Programming service

We offers various services at nominal charges. These include ROM writing, ROM reading and package stamping and screening. Contact local our representative for further information.

■ Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.

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## LC86P7248

- (4) Operating supply voltage : 4.5V to 6.0V  
 (5) Instruction cycle time : 1μs to 366μs  
 (6) Operating temperature : -30°C to +70°C  
 (7) The pin compatible with the LC867200 series mask ROM devices  
 (8) Applicable mask ROM version : LC867248/LC867240/LC867232/LC867224  
 (9) Factory shipment : QIP100E

### Notice for use

LC86P7248 is provided for the first release and small shipping of the LC867200 series.  
 At using, take notice of the followings.

- (1) A point of difference LC86P7248 and LC867200 series

Item	LC86P7248	LC867248/40/32/24
Operation after reset releasing	The option is specified until 3ms after going to a 'H' level to the reset terminal by degrees. The program is executed from 00H of the program counter.	The program is executed from 00H of the program counter immediately after going to a 'H' level to the reset terminal.
Operating supply voltage range (VDD)	4.5V to 6.0V	2.5V to 6.0V
Power dissipation	Refer to 'electrical characteristics' on the semiconductor news.	

LC86P7248 uses 256 bytes that is addressed on 0FF00H to FFFFH in the program memory as the option configuration data area. This option configuration can execute all options which LC867200 series have.

- A kind of the option of the LC86P7248

A kind of option	Pins, Circuits	Contents of the option
Input/output form of input/output ports	Port 0	1. N-channel open drain output 2. CMOS output *1
		1. Pull-up MOS Tr. 2. No Pull-up MOS Tr. *2
	Port 1	1. Input : Programmable pull-up MOS Tr. Output : N-channel open drain 2. Input : Programmable pull-up MOS Tr. Output : CMOS *1
	Port 3	1. Input : No Programmable pull-up MOS Tr. Output : N-channel open drain 2. Input : Programmable pull-up MOS Tr. Output : CMOS *1
Pull-up MOS Tr. of input port	Ports 70, 71, 72, 73 *1	1. No Pull-up MOS Tr. 2. Pull-up MOS Tr.

\*1) Specified in a bit.

\*2) Specified in nibble unit. Pull-up MOS Tr. is not provided in N-channel open drain output port.

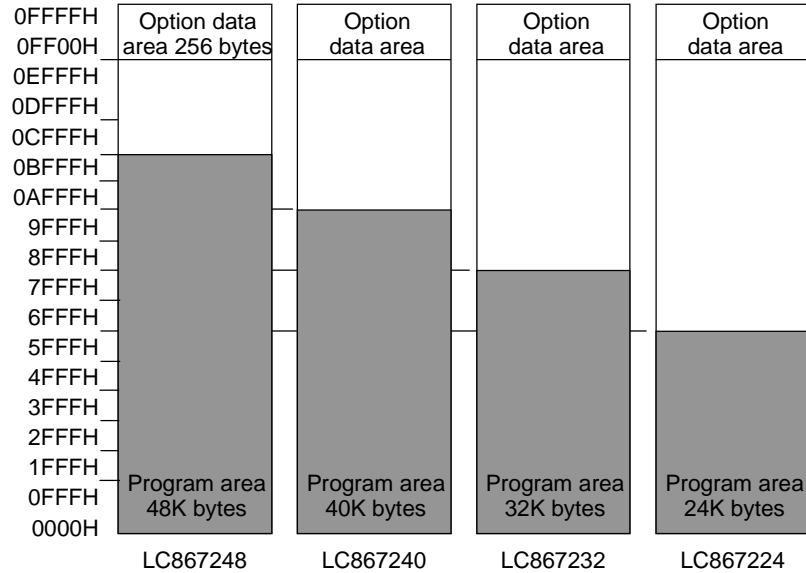
## LC86P7248

### (1) Option

The option data is created by the option specified program "SU86K.EXE". The created option data is linked to the program area by linkage loader "L86K.EXE".

### (2) ROM space

LC86P7248 and LC867200 series use 256 bytes that is addressed on 0FF00H to 0FFFFH in the program memory as the option specified data area. These program memory capacity are 49152 bytes that is addressed on 0000H to 0BFFFH.



### (3) Ordering information

1. When ordering the identical mask ROM and PROM devices simultaneously.

Provide an EPROM containing the target memory contents together with the separate order forms for each of the mask ROM and PROM versions.

2. When ordering a PROM device.

Provide an EPROM containing the target memory contents together with an order form.

## LC86P7248

### How to use

#### (1) Specification of option

Programming data for PROM of the LC86P7248 is required.

Debugged evaluation file (EVA file) must be converted to an INTEL-HEX formatted file (HEX file) with file converter program, EVA2HEX.EXE. The HEX file is used as the programming data for the LC86P7248.

#### (2) How to program for the PROM

The LC86P7248 can be programmed by PROM programmer with attachment ; W86EP7248Q

- Recommended EPROM programmer

Productor	EPROM programmer
Advantest	R4945, R4944, R4943
Andou	AF-9704
AVAL	PKW-1100, PKW-3000
Minato electronics	MODEL1890A

- “27512 (Vpp=12.5V) Intel high speed programming” mode available. The address must be set to “0 to 0FFFFH” and a jumper (DASEC) must be set to ‘OFF’ at programming.

#### (3) How to use the data security function

“Data security” is the disabled function to read the data of the PROM.

The following is the process in order to execute the data security.

1. Set ‘ON’ the jumper of attachment.

2. Program again. Then PROM programmer displays the error. The error means normally activity of the data security.

It is not a trouble of the PROM programmer or the LSI.

Notes

- Data security is not executed when the data of all address have ‘FFH’ at the sequence 2 above.
- The programming by a sequential operation “BLANK=>PROGRAM=>VERIFY” cannot be executed data security at the sequence 2 above.
- Set to ‘OFF’ the jumper after executing the data security.

Data security

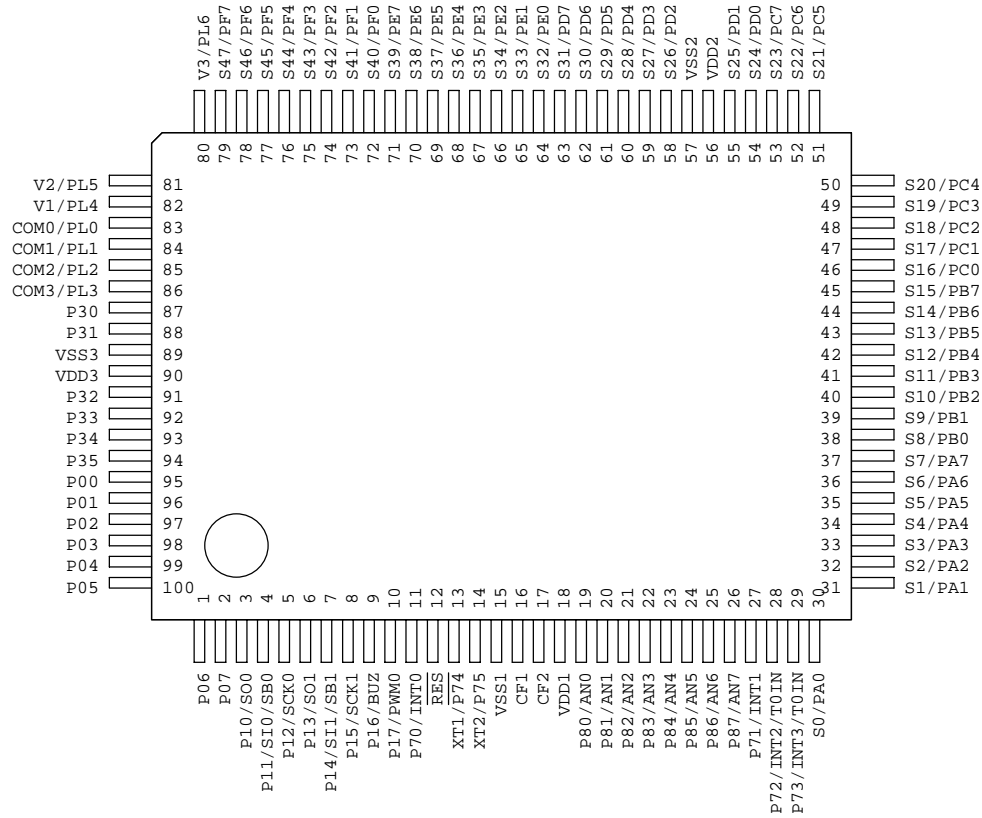


Not data security

W86EP7248Q

# LC86P7248

## Pin Assignment



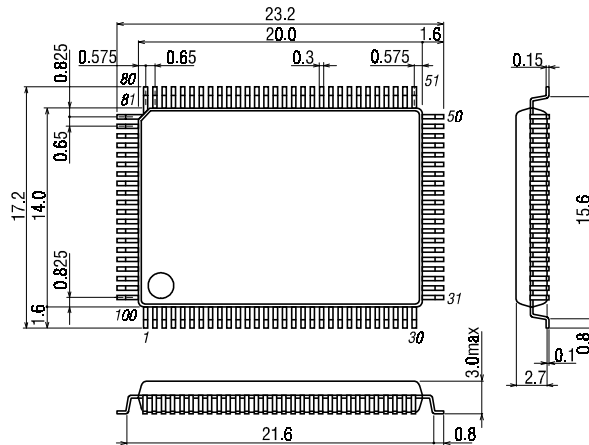
### Notes

- The QIP packages should be heat-soaked for 12 hours at 125°C immediately prior to mounting (This baking is called pre-baking).
- After pre-baking, a controlled environment must be maintained until soldering. The environment must be held at a temperature of 30°C or less and a humidity level of 70% or less. Please solder within 24 hours.

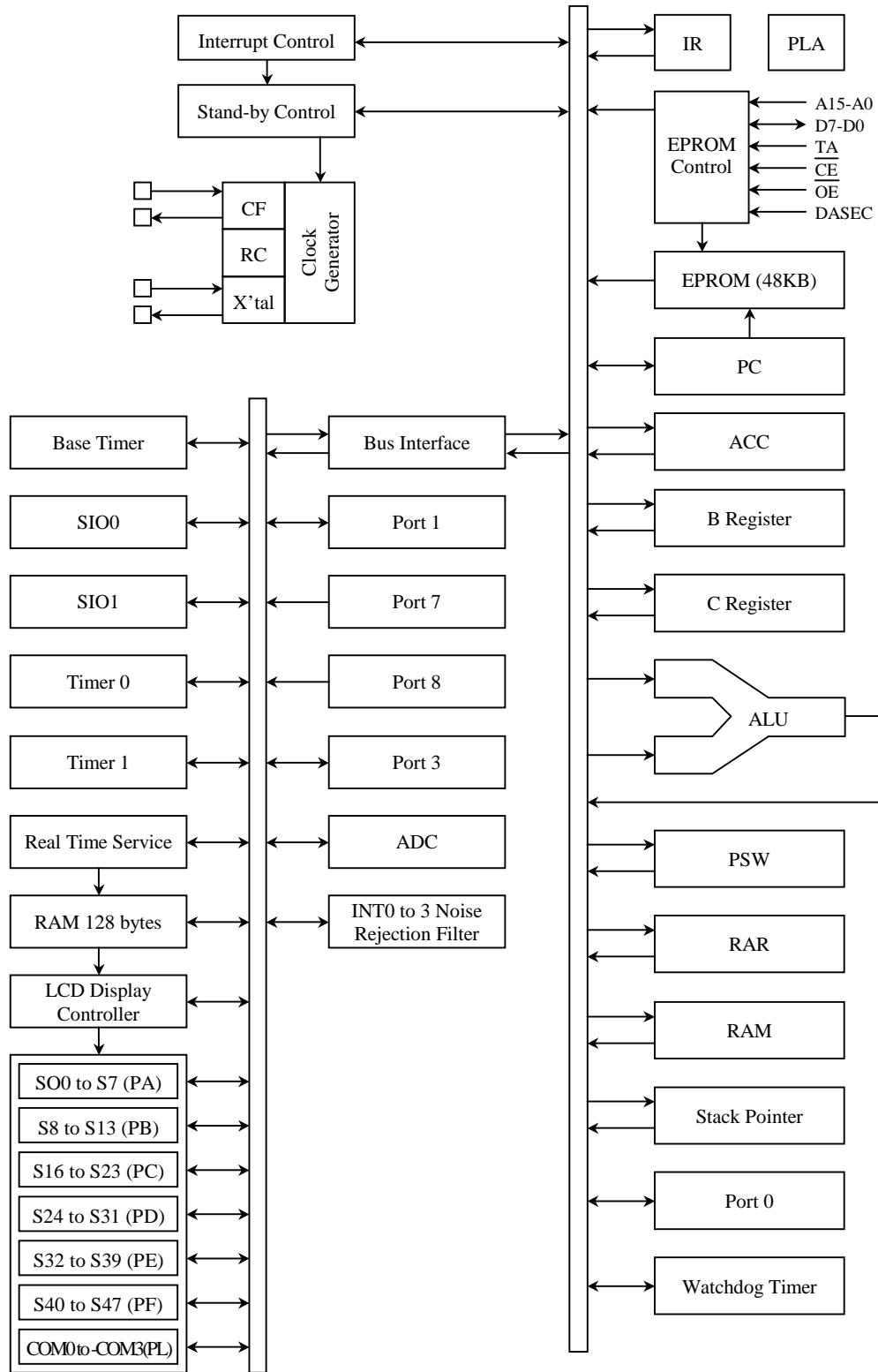
### Package Dimension

(unit : mm)

3151



System Block Diagram



LC86P7248

Pin Description

Pin name	I/O	Function description	Option	PROM mode																																			
VSS1, 2, 3 *1	-	Power pin (-)	-	-																																			
VDD1, 2, 3 *1	-	Power pin (+)	-	-																																			
PORT0 P00 to P07	I/O	<ul style="list-style-type: none"> <li>8-bit input/output port</li> <li>Input/output in nibble units</li> <li>Input for port 0 interrupt</li> <li>Input for HOLD release</li> </ul>	<ul style="list-style-type: none"> <li>Pull-up resistor : Provided/Not provided (specified in nibble units)</li> <li>Output form (P00 – P07) : CMOS/N-channel open drain (specified in a bit)</li> </ul>	-																																			
PORT1 P10 to P17	I/O	<ul style="list-style-type: none"> <li>8-bit input/output port</li> <li>Input/output can be specified in bit unit</li> <li>Other pin functions</li> <li>P10 : SIO0 data output</li> <li>P11 : SIO0 data input/bus input/output</li> <li>P12 : SIO0 clock input/output</li> <li>P13 : SIO1 data output</li> <li>P14 : SIO1 data input/bus input/output</li> <li>P15 : SIO1 clock input/output</li> <li>P16 : Buzzer output</li> <li>P17 : Timer1 output (PWM output)</li> </ul>	<ul style="list-style-type: none"> <li>Output form : CMOS/N-channel open drain (specified in a bit)</li> </ul>	Data line D0 to D7																																			
PORT3 P30 to P35	I/O	<ul style="list-style-type: none"> <li>6-bit input/output port</li> <li>Input/output can be specified in bit unit</li> </ul>	<ul style="list-style-type: none"> <li>Output form : CMOS/N-channel open drain (specified in a bit)</li> </ul>	-																																			
PORT7 P70 P71 to P73	I/O  I	<ul style="list-style-type: none"> <li>6-bit input port</li> <li>Other pin functions</li> <li>P70 : INT0 input/HOLD release input/ N-ch Tr. output for watchdog timer</li> <li>P71 : INT1 input/HOLD release input</li> <li>P72 : INT2 input/timer 0 event input</li> <li>P73 : INT3 input with noise filter/timer 0 event input</li> <li>Interrupt received form, vector address</li> </ul> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th></th> <th>rising</th> <th>falling</th> <th>rising &amp; falling</th> <th>high level</th> <th>low level</th> <th>vector</th> </tr> </thead> <tbody> <tr> <td>INT0</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> <td>03H</td> </tr> <tr> <td>INT1</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> <td>0BH</td> </tr> <tr> <td>INT2</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> <td>13H</td> </tr> <tr> <td>INT3</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> <td>1BH</td> </tr> </tbody> </table>		rising	falling	rising & falling	high level	low level	vector	INT0	enable	enable	disable	enable	enable	03H	INT1	enable	enable	disable	enable	enable	0BH	INT2	enable	enable	enable	disable	disable	13H	INT3	enable	enable	enable	disable	disable	1BH	<ul style="list-style-type: none"> <li>Pull-up resistor : Provided/Not provided (specified in a bit) (P70, P71, P72, P73)</li> <li>* <math>\overline{P74}</math>, P75 don't have the pull-up resistor option.</li> </ul>	Power for programming  PROM control signals DASEC (*2) $\overline{OE}$ (*3) $\overline{CE}$ (*4)
	rising	falling	rising & falling	high level	low level	vector																																	
INT0	enable	enable	disable	enable	enable	03H																																	
INT1	enable	enable	disable	enable	enable	0BH																																	
INT2	enable	enable	enable	disable	disable	13H																																	
INT3	enable	enable	enable	disable	disable	1BH																																	
$\overline{P74}$ , P75	I	<ul style="list-style-type: none"> <li>P74 : XT1 terminal for crystal oscillation</li> <li>P75 : XT2 terminal for crystal oscillation</li> </ul>																																					
Port8 P80 to P87	I	<ul style="list-style-type: none"> <li>8-bit input port</li> <li>Other function</li> <li>AD input port (8 port pins)</li> </ul>	-	-																																			

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Pin name	I/O	Function description	Option	PROM mode
Port A (S0/PA0 to S7/PA7)	I/O	<ul style="list-style-type: none"> <li>• Segment output terminal for LCD display</li> <li>• Can be used as a general input/output port</li> </ul>	-	Address input A0 to A7
Port B (S8/PB0 to S15/PB7)	I/O	<ul style="list-style-type: none"> <li>• Segment output terminal for LCD display</li> <li>• Can be used as a general input/output port</li> </ul>	-	Address input A8 to A13
Port C (S16/PC0 to S23/PC7)	I/O	<ul style="list-style-type: none"> <li>• Segment output terminal for LCD display</li> <li>• Can be used as a general input/output port</li> </ul>	-	PROM control signal input • TA (*5) Address input • A14, A15
Port D (S24/PD0 to S31/PD7)	I/O	<ul style="list-style-type: none"> <li>• Segment output terminal for LCD display</li> <li>• Can be used as a general input/output port</li> </ul>	-	-
Port E (S32/PE0 to S39/PE7)	I/O	<ul style="list-style-type: none"> <li>• Segment output terminal for LCD display</li> <li>• Can be used as a general input/output port</li> </ul>	-	-
Port F (S40/PF0 to S47/PF7)	I/O	<ul style="list-style-type: none"> <li>• Segment output terminal for LCD display</li> <li>• Can be used as a general input/output port</li> </ul>	-	-
Port L (COM0/PL0 to COM3/PL3)	I/O	<ul style="list-style-type: none"> <li>• Common output terminal for LCD display</li> <li>• Can be used as a general input port</li> </ul>	-	-
V1/PL4 – V3/PL6	I	<ul style="list-style-type: none"> <li>• Bias power terminal for LCD drive</li> <li>• Can be used as a general input port</li> </ul>	-	-
$\overline{\text{RES}}$	I	Reset pin	-	-
XT1/ $\overline{\text{P74}}$	I	<ul style="list-style-type: none"> <li>• Input pin for 32.768kHz crystal oscillation</li> <li>In case of non use, connect to VDD.</li> <li>• Other function</li> <li>A general input port <math>\overline{\text{P74}}</math></li> </ul>	-	-
XT2/P75	O  (I)	<ul style="list-style-type: none"> <li>• Output pin for 32.768kHz crystal oscillation</li> <li>In case of non use, should be left unconnected</li> <li>• Other function</li> <li>A general input port P75</li> </ul>	-	-
CF1	I	Input pin for ceramic resonator oscillation	-	-
CF2	O	Output pin for ceramic resonator oscillation	-	-

\* All of port options can be specified in bit unit except the pull-up resistor of port 0.

[Notes] • The VDD1, VDD2 and VDD3 terminals must be shorted electrically each other.

• The VSS1, VSS2 and VSS3 terminals must be shorted electrically each other.

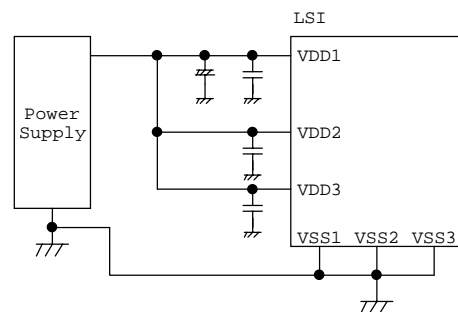
\*1 Connect like the following figure to reduce noise into a VDD terminals.

\*2 Memory select input for data security

\*3 Output enable input

\*4 Chip enable input

\*5 TA → PROM control signal input





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### 1. Absolute Maximum Ratings at Ta=25°C, VSS=VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD[V]	min.	typ.		max.
Supply voltage	VDDMAX	VDD1, VDD2 VDD3	VDD1=VDD2= VDD3		-0.3		+7.0	V
LCD display voltage	VLCD	V1/PL6, V2/PL5 V3/PL4	VDD1=VDD2= VDD3		-0.3		VDD	
Input voltage	VI	•Ports 71, 72, 73 •Ports $\overline{74}$ , 75 •Port 8, Port L • $\overline{\text{RES}}$			-0.3		VDD+0.3	
Input/output voltage	VIO	•Port 0, 1, 3 •Port 70 •Ports A,B,C,D,E,F			-0.3		VDD+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 3	•CMOS output •At each pins			-4	mA
		IOPH(2)	Ports A,B,C,D,E,F				-4	
	Total output current	$\Sigma$ IIOAH(1)	Ports 0, 1, 32, 33, 34, 35	Total all pins			-38	
		$\Sigma$ IIOAH(2)	Ports 30, 31	Total all pins			-4	
		$\Sigma$ IIOAH(3)	Ports S0 to S25	Total all pins			-25	
	$\Sigma$ IIOAH(4)	Ports S26 to S47	Total all pins			-25		
Low level output current	Peak output current	IOPL(1)	Ports 0, 1, 3	At each pins			20	
		IOPL(2)	Ports A,B,C,D,E,F	At each pins			20	
		IOPL(3)	Port 70	At each pins			15	
	Total output current	$\Sigma$ IOAL(1)	Ports 0, 1, 32, 33, 34, 35	Total all pins			50	
		$\Sigma$ IOAL(2)	Ports 30, 31	Total all pins			20	
		$\Sigma$ IOAL(3)	Ports S0 to S25	Total all pins			39	
		$\Sigma$ IOAL(4)	Ports S26 to S47	Total all pins			33	
	$\Sigma$ IOAL(5)	Port 70	Total all pins			10		
Maximum power dissipation	Pdmax	QIP100E	Ta=-30 to +70°C				515	mW
Operating temperature range	Topr				-30		+70	°C
Storage temperature range	Tstg				-55		+125	

#### Notes

- The QIP packages should be heat-soaked for 12 hours at 125°C immediately prior to mounting (This baking is called pre-baking).
- After pre-baking, a controlled environment must be maintained until soldering. The environment must be held at a temperature of 30°C or less and a humidity level of 70% or less. Please solder within 24 hours.

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2. Recommended Operating Range at Ta=-30°C to +70°C, VSS=VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD[V]	min.	typ.		max.
Operating supply voltage range	VDD(1)	VDD1=VDD2=VDD3	0.98μs ≤ tCYC ≤ 400μs		4.5		6.0	V
	VDD(2)		3.9μs ≤ tCYC ≤ 400μs		2.5		6.0	
Hold voltage	VHD	VDD1=VDD2=VDD3	RAMs and the registers hold voltage at HOLD mode.		2.0		6.0	
Input high voltage	VIH(1)	Port 0	Output disable	4.5 to 6.0	0.4VDD +0.9		VDD	
	VIH(2)	•Ports 1, 3 •Ports A,B,C,D,E,F,L •Ports 72, 73	Output disable	4.5 to 6.0	0.75VDD		VDD	
	VIH(3)	•Port 70 Port input/interrupt •Port 71 •RES	Output N-channel Tr. OFF	4.5 to 6.0	0.75VDD		VDD	
	VIH(4)	Port 70 Watchdog timer	Output N-channel Tr. OFF	4.5 to 6.0	0.9VDD		VDD	
	VIH(5)	•Port 8 •Port 74, 75	Using as port	4.5-6.0	0.75VDD		VDD	
Input low voltage	VIL(1)	Port 0	Output disable	4.5 to 6.0	VSS		0.2VDD	
	VIL(2)	•Ports 1, 3 •Ports A,B,C,D,E,F,L •Ports 72, 73	Output disable	4.5 to 6.0	VSS		0.25VDD	
	VIL(3)	•Port 70 Port input/interrupt •Port 71 •RES	Output N-channel Tr. OFF	4.5 to 6.0	VSS		0.25VDD	
	VIL(4)	Port 70 Watchdog timer	Output N-channel Tr. OFF	4.5 to 6.0	VSS		0.8VDD -1.0	
	VIL(5)	•Port 8 •Port 74, 75	Using as port	4.5 to 6.0	VSS		0.25VDD	
Operation cycle time	tCYC			4.5 to 6.0	0.98		400	μs
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 1	4.5 to 6.0		6		MHz
	FmCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 1	4.5 to 6.0		3		
	FmRC		RC oscillation	4.5 to 6.0	0.4	0.8	3.0	
	FsXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 2	4.5 to 6.0		32.768		kHz
Oscillation stabilizing time period (Note 1)	tmsCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 to 6.0				ms
	tmsCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 to 6.0				
	tssXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 3	4.5 to 6.0				s

(Note 1) The oscillation constant is shown on table 1 and table 2.

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3. Electrical Characteristics at Ta=-30°C to +70°C, VSS=VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings			unit
					min.	typ.	max.	
Input high current	IIH(1)	•Port 1 •Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr. OFF. VIN=VDD (including the off-leak current of the output Tr.)	4.5 to 6.0			1	μA
	IIH(2)	•Port 7 without pull-up MOS Tr. •Port 8	VIN=VDD	4.5 to 6.0			1	
	IIH(3)	Port 3	VIN=VDD	4.5 to 6.0			1	
	IIH(4)	Ports A,B,C,D,E,F,L	VIN=VDD	4.5 to 6.0			1	
	IIH(5)	$\overline{\text{RES}}$	VIN=VDD	4.5 to 6.0			1	
	IIH(6)	Ports $\overline{74}, 75$	Using as port VIN=VDD	4.5 to 6.0			1	
Input low current	IIL(1)	•Port 1 •Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr. OFF. VIN=VSS (including the off-leak current of the output Tr.)	4.5 to 6.0	-1			V
	IIL(2)	•Port 7 without pull-up MOS Tr. •Port 8	VIN=VSS	4.5 to 6.0	-1			
	IIL(3)	Port 3	VIN=VSS	4.5 to 6.0	-1			
	IIL(4)	Ports A,B,C,D,E,F,L	VIN=VSS	4.5 to 6.0	-1			
	IIL(5)	$\overline{\text{RES}}$	VIN=VSS	4.5 to 6.0	-1			
	IIL(6)	Ports $\overline{74}, 75$	Using as port VIN=VSS	4.5 to 6.0	-1			
Output high voltage	VOH(1)	Ports 0,1 of CMOS output	IOH=-1.0mA	4.5 to 6.0	VDD-1			V
	VOH(2)	•Port 3 of CMOS output •Ports A,B,C,D,E,F of CMOS output	IOH=-1.0mA	4.5 to 6.0	VDD-1			
Output low voltage	VOL(1)	Ports 0, 1	IOL=10mA	4.5 to 6.0			1.5	
	VOL(2)		IOL=1.6mA	4.5 to 6.0			0.4	
	VOL(3)	Port 70	IOL=1mA	4.5 to 6.0			0.4	
	VOL(4)	Port 3	IOL=10mA	4.5 to 6.0			1.5	
	VOL(5)		IOL=1.6mA	4.5 to 6.0			0.4	
	VOL(6)	Ports A,B,C,D,E,F Of CMOS output	IOL=8mA	4.5 to 6.0			1.5	
	VOL(7)		IOL=1.6mA	4.5 to 6.0			0.4	

Continue.

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Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD[V]	min.	typ.		max.
LCD output regulation	VODLS	S0 to S47	•Deference voltage to ideal value •VLCD, 2/3VLCD, 1/3VLCD	4.5 to 6.0	0		±0.2	V
	VODLC	COM0 to COM3	•Deference voltage to ideal value •VLCD, 2/3VLCD, 1/2VLCD, 1/3VLCD	4.5 to 6.0	0		±0.2	
LCD ladder resistor	RLCD(1)		Resistance at a ladder resistor	4.5 to 6.0		60		kΩ
	RLCD(2)		•Resistance at a ladder resistor •1/2R mode	4.5 to 6.0		30		
Pull-up MOS Tr. resistor	Rpu	•Ports 0, 1, 3 •Ports A,B,C,D,E,F •Ports 70, 71, 72, 73	VOH=0.9VDD	4.5 to 6.0	15	40	70	
Hysteresis voltage	VHIS	•Port 1 •Ports 70, 71, 72, 73 •RES	Output disable	4.5 to 6.0		0.1VDD		V
Pin capacitance	CP	All pins	•f=1MHz •Unmeasurement terminals for the input are set to VSS level. •Ta=25°C	4.5 to 6.0		10		pF

4. Serial Input/Output Characteristics at Ta=-30°C to +70°C, VSS=VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit		
				VDD[V]	min.	typ.		max.	
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0, SCK1	Refer to figure 5.	4.5 to 6.0	2		tCYC
		Low Level pulse width	tCKL(1)				1		
		High Level pulse width	tCKH(1)				1		
	Output clock	Cycle	tCKCY(2)	SCK0, SCK1	•Use pull-up resistor (1kΩ) when open drain output. •Refer to figure 5.	4.5 to 6.0	2		
		Low Level pulse width	tCKL(2)					1/2 tCKCY	
		High Level pulse width	tCKH(2)					1/2 tCKCY	
Serial input	Data set up time	tICK	•SI0,SI1 •SB0,SB1	•Data set-up to SCK0, 1 •Data hold from SCK0, 1 •Refer to figure 5.	4.5 to 6.0	0.1		μs	
	Data hold time	tCKI			4.5 to 6.0	0.1			
Serial output	Output delay time (Serial clock is external clock)	tCKO(1)	•SO0, SO1 •SB0, SB1	•Use pull-up resistor (1kΩ) when open drain output. •Data hold from SCK0, 1 •Refer to figure 5.	4.5 to 6.0			7/12tCYC +0.2	
	Output delay time (Serial clock is internal clock)	tCKO(2)			4.5 to 6.0			1/3tCYC +0.2	

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5. Pulse Input Conditions at Ta=-30°C to +70°C, VSS=VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD[V]	min.	typ.		max.
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN	•Interrupt acceptable •Timer0-countable	4.5 to 6.0	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock is selected to 1/1.)	•Interrupt acceptable •Timer0-countable	4.5 to 6.0	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock is selected to 1/16.)	•Interrupt acceptable •Timer0-countable	4.5 to 6.0	32			
	tPIH(4) tPIL(4)	INT3/T0IN (The noise rejection clock is selected to 1/64.)	•Interrupt acceptable •Timer0-countable	4.5 to 6.0	128			
	tPIL(5)	RES	Reset acceptable	4.5 to 6.0	200			μs

6. AD Converter Characteristics at Ta=-30°C to + 70°C, VSS=VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD[V]	min.	typ.		max.
Resolution	NAD			4.5 to 6.0		8		bit
Absolute precision (Note 2)	ETAD			4.5 to 6.0			±1.5	LSB
Conversion time	tCAD		AD conversion time = 16 × tCYC (ADCR2=0) (Note 3)	4.5 to 6.0	15.68 (tCYC= 0.98μs)		65.28 (tCYC= 4.08μs)	μs
			AD conversion time = 32 × tCYC (ADCR2=1) (Note 3)		31.36 (tCYC= 0.98μs)		130.56 (tCYC= 4.08μs)	
Analog input voltage range	VAIN	AN0 - AN7		4.5 to 6.0	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5 to 6.0			1	μA
	IAINL		VAIN=VSS	4.5 to 6.0	-1			

(Note 2) Absolute precision excepts quantizing error (±1/2 LSB).

(Note 3) The conversion time means the time from executing the AD conversion instruction to setting the complete digital conversion value to the register.

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7. Current Dissipation Characteristics at Ta=-30°C to +70°C, VSS=VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD[V]	min.	typ.		max.
Current dissipation during basic operation (Note 4)	IDDOP(1)	VDD1= VDD2= VDD3	<ul style="list-style-type: none"> <li>•FmCF=6MHz Ceramic resonator oscillation</li> <li>•FsXtal=32.768kHz crystal oscillation</li> <li>•System clock : CF oscillation</li> <li>•Internal RC oscillation stops</li> <li>•1/1 divided</li> </ul>	4.5 to 6.0		15	30	mA
	IDDOP(2)		<ul style="list-style-type: none"> <li>•FmCF=3MHz Ceramic resonator oscillation</li> <li>•FsXtal=32.768kHz crystal oscillation</li> <li>•System clock : CF oscillation</li> <li>•Internal RC oscillation stops</li> <li>•1/2 divided</li> </ul>	4.5 to 6.0		6	15	
	IDDOP(3)		<ul style="list-style-type: none"> <li>•FmCF=0Hz (when oscillation stops)</li> <li>•FsXtal=32.768kHz crystal oscillation</li> <li>•System clock : RC oscillation</li> <li>•1/2 divided</li> </ul>	4.5 to 6.0		4	13	
	IDDOP(4)		<ul style="list-style-type: none"> <li>•FmCF=0Hz (when oscillation stops)</li> <li>•FsXtal=32.768kHz crystal oscillation</li> <li>•System clock : crystal oscillation</li> <li>•Internal RC oscillation stops</li> <li>•1/2 divided</li> </ul>	4.5 to 6.0		4	9	

Continue.

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Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD[V]	min.	typ.		max.
Current dissipation in HALT mode (Note 4)	IDDHALT(1)	VDD1= VDD2= VDD3	<ul style="list-style-type: none"> <li>•HALT mode</li> <li>•FmCF=6MHz Ceramic resonator oscillation</li> <li>•FsXtal=32.768kHz crystal oscillation</li> <li>•System clock : CF oscillation</li> <li>•Internal RC oscillation stops</li> <li>•1/1 divided</li> </ul>	4.5 to 6.0		6	11	mA
	IDDHALT(2)		<ul style="list-style-type: none"> <li>•HALT mode</li> <li>•FmCF=3MHz Ceramic resonator oscillation</li> <li>•FsXtal=32.768kHz crystal oscillation</li> <li>•System clock : CF oscillation</li> <li>•Internal RC oscillation stops</li> <li>•1/2 divided</li> </ul>	4.5 to 6.0		2.2	9	
	IDDHALT(3)		<ul style="list-style-type: none"> <li>•HALT mode</li> <li>FmCF=0Hz (when oscillation stops)</li> <li>•FsXtal=32.768kHz crystal oscillation</li> <li>•System clock : RC oscillation</li> <li>•1/2 divided</li> </ul>	4.5 to 6.0		500	1700	μA
	IDDHALT(4)		<ul style="list-style-type: none"> <li>•HALT mode</li> <li>FmCF=0Hz (when oscillation stops)</li> <li>•FsXtal=32.768kHz crystal oscillation</li> <li>•System clock : crystal oscillation</li> <li>•Internal RC oscillation stops</li> <li>•1/2 divided</li> </ul>	4.5 to 6.0		25	100	
	IDDHALT(5)							
Current dissipation in HOLD mode (Note 4)	IDDHOLD(1)	VDD1= VDD2= VDD3	HOLD mode	4.5 to 6.0		0.05	30	

(Note 4) The currents of the output transistors and the pull-up MOS transistors are ignored.

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Table 1. Ceramic resonator oscillation guaranteed constant (main clock)

Oscillation type	Maker	Oscillator	C1	C2
6MHz ceramic resonator oscillation				
3MHz ceramic resonator oscillation				

\* Both C1 and C2 must use K rank ( $\pm 10\%$ ) and SL characteristics.

Table 2. Crystal oscillation recommended constant (sub clock)

Oscillation type	Maker	Oscillator	C3	C4	Rd
32.768kHz crystal oscillation					

- (Notes)
- Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
  - If you use other oscillators herein, we provide no guarantee for the characteristics.

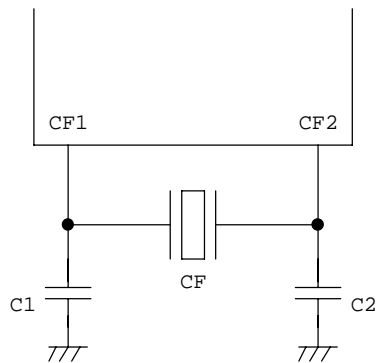


Figure 1 Ceramic oscillation circuit

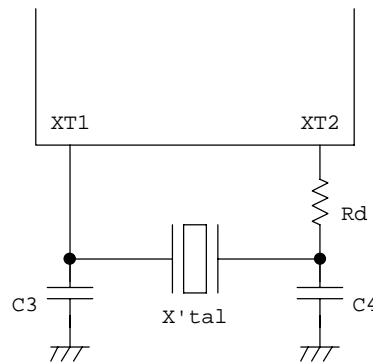


Figure 2 Crystal oscillation circuit



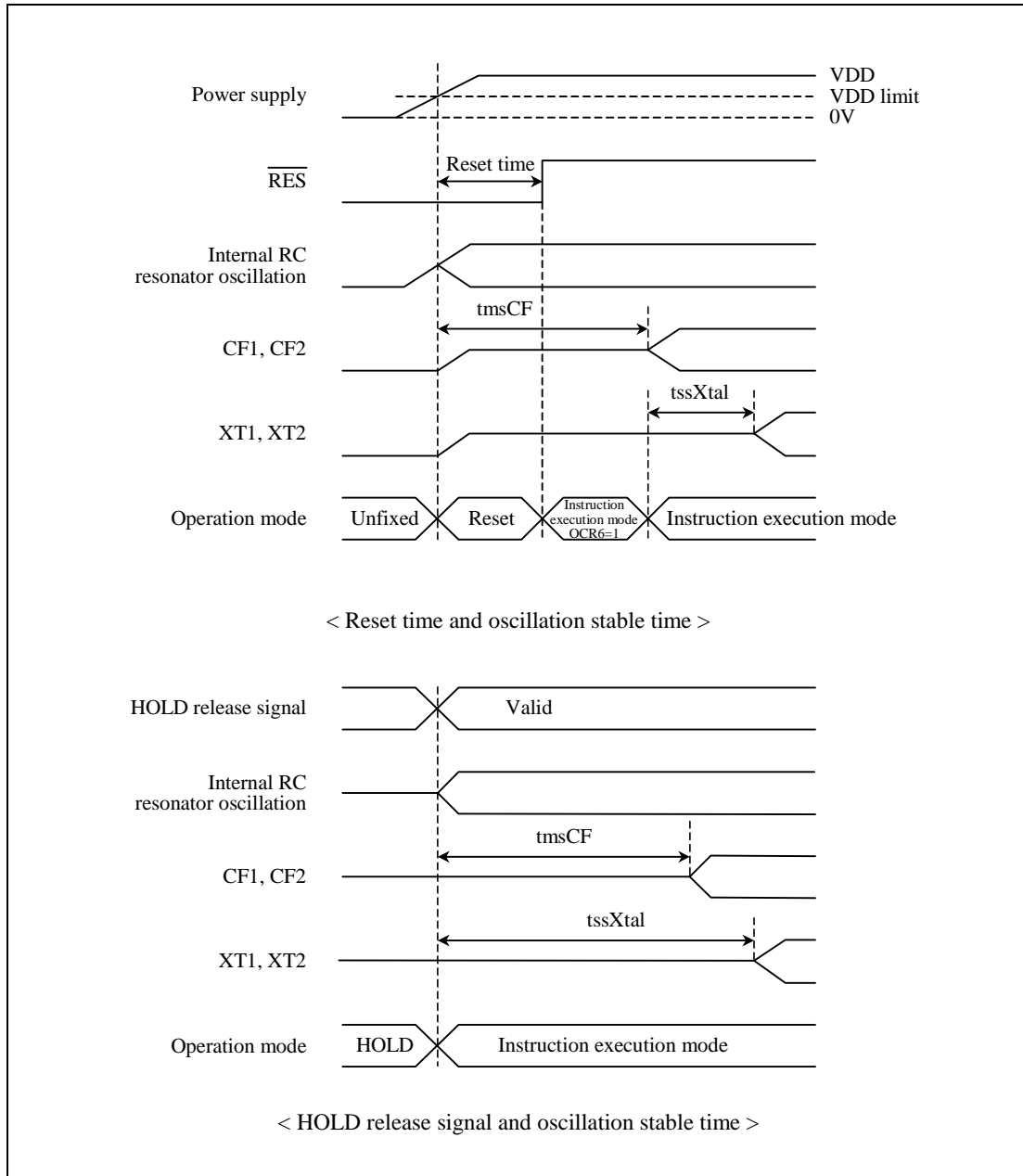
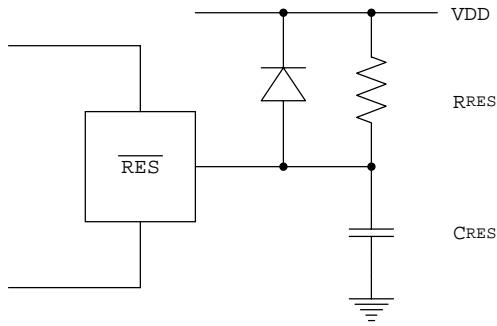


Figure 3 Oscillation stable time



(Note) Fix the value of CRES, RRES that is sure to reset until 200 $\mu$ s, after Power supply has been over inferior limit of supply voltage.

Figure 4 Reset circuit

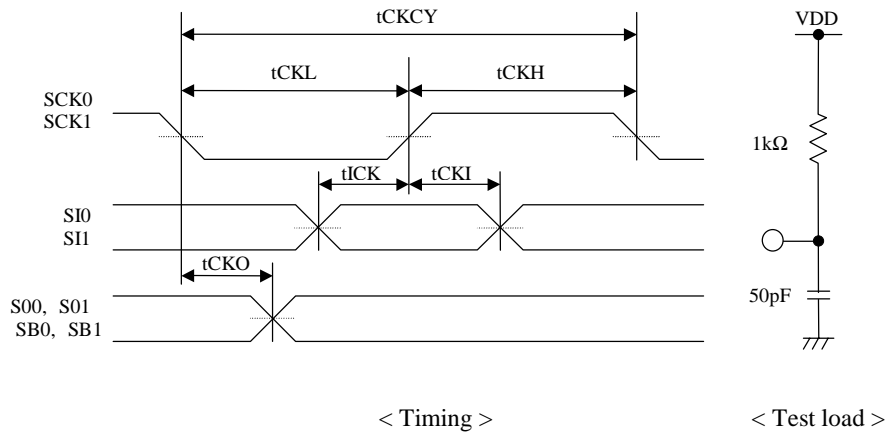
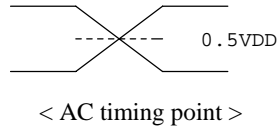


Figure 5 Serial input / output test condition

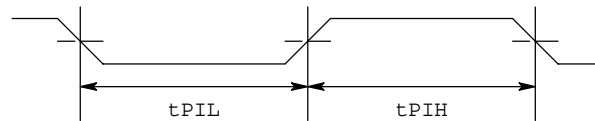
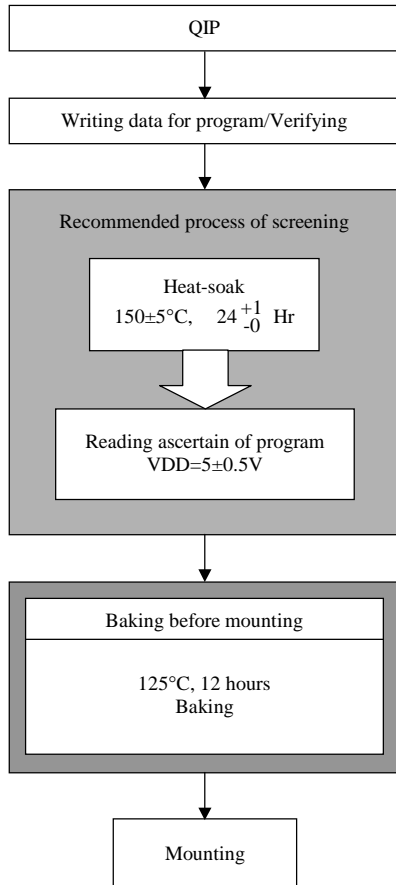


Figure 6 Pulse input timing condition

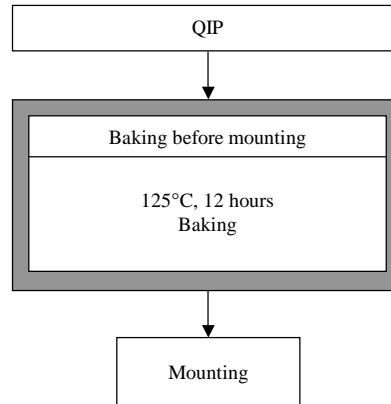
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- The construction of the one-time programmable microcomputer with a blank built-in PROM makes it impossible for Sanyo to completely factory-test it before shipping. To probe reliability of the programmed devices, the screening procedure shown in the following figure should always be followed.
- It is not possible to perform a writing test on the blank PROM. 100% yield, therefore, cannot be guaranteed.
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The environment must be held at a temperature of 30°C or less and a humidity level of 70% or less.
- After opening the packing  
The preparation procedures shown in the following figure should always be followed prior to mounting the packages on the substrate. Note that the QIP package should be heat-soaked for 12 hours at 125°C immediately prior to mounting (This baking is called pre-baking). After pre-baking, a controlled environment must be maintained until soldering. The environment must be held at a temperature of 30°C or less and a humidity level of 70% or less. Please solder within 24 hours.

a. Shipping with a blank PROM  
(Programming the data by yourself)



b. Shipping with a programmed PROM  
(Programming the data by Sanyo)



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