E2A0035-16-X0

This version: Jan. 1998
Previous version: Nov. 1996

OKI Semiconductor

MSM6882-3/6882-5

2400/1200 bps Single Chip MSK Modem

GENERAL DESCRIPTION

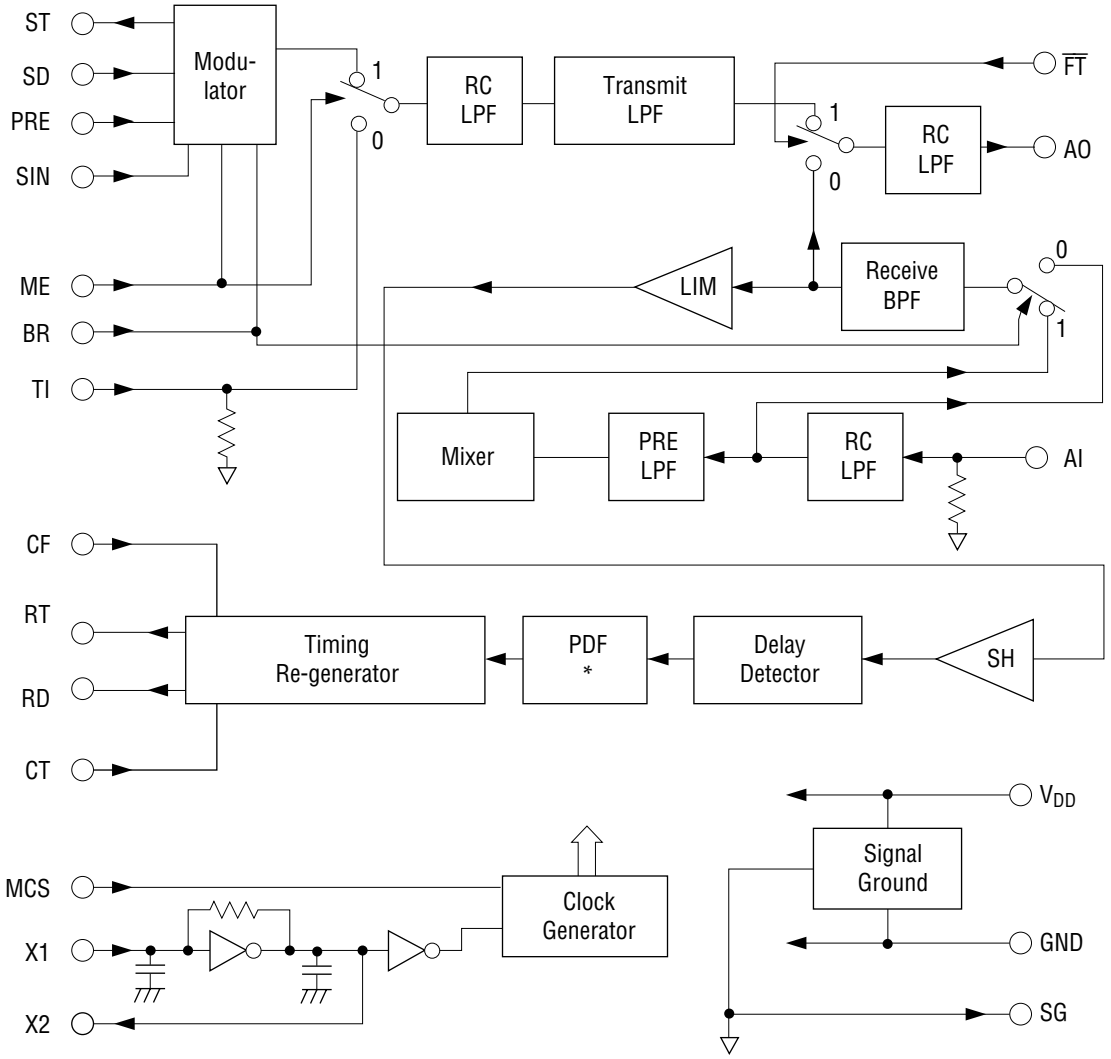
The MSM6882-3/6882-5 is a single chip MSK (Minimum Shift Keying) modem which is fabricated by Oki's low power consumption CMOS silicon gate technology.
The demodulator receives the data to be transmitted (SD) synchronized with the transmit timing clock (ST) generated by the on-chip clock generator. The signal, which is modulated by MSK method, is output.
The demodulator converts the received MSK signal to the received data (RD) by means of a delay detection technique after limiting the band of the received MSK signal. This signal is input to the digital PLL and the re-generated timing clock (RT) is output from the demodulator, synchronized with the RD.

FEATURES

- Signal power supply: +3.6 V (MSM6882-3)
  +5 V (MSM6882-5)
- On-chip SCF (Switched Capacitor Filter)
- The transmit filter can be also used as voice splatter filter.
- The receive timing re-generator has two different lock-in time performance options to be chosen from.
- Bit rate 2400/1200 bps
- CCIR Rec. 623
- The modulation method can be selected from COS-FFSK and SIN-FFSK.
- Built-in crystal oscillation circuit.
- Package options:

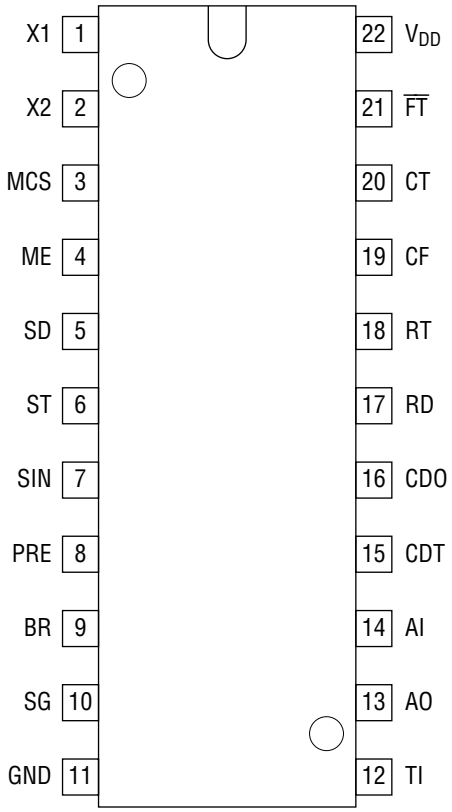
22-pin plastic DIP	(DIP22-P-400-2.54)	(Product name: MSM6882-3RS)
		(Product name: MSM6882-5RS)
24-pin plastic SOP	(SOP24-P-430-1.27-K)	(Product name: MSM6882-3GS-K)
		(Product name: MSM6882-5GS-K)

BLOCK DIAGRAM

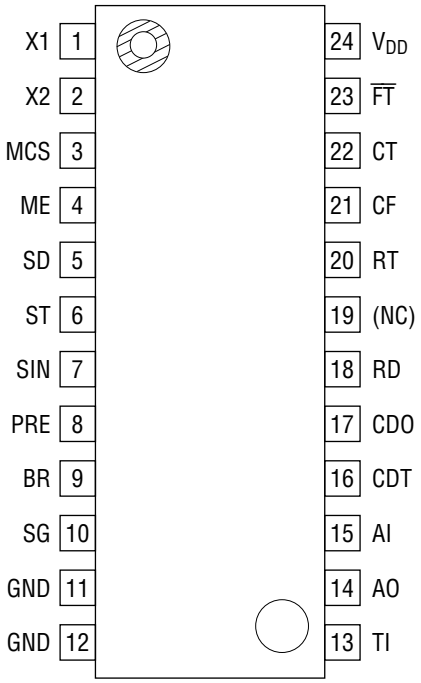


* Post Detection Filter

PIN CONFIGURATION (TOP VIEW)



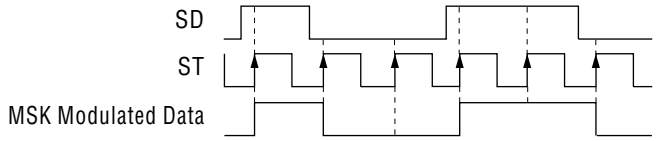
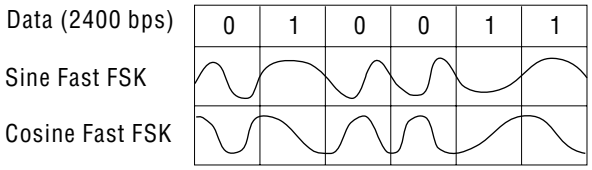
22-Pin Plastic DIP

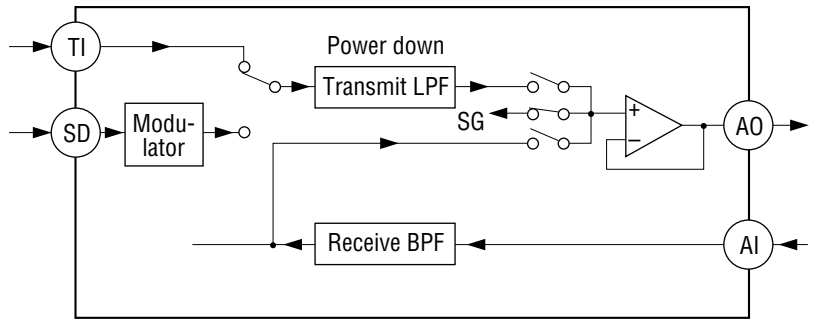


24-Pin Plastic SOP

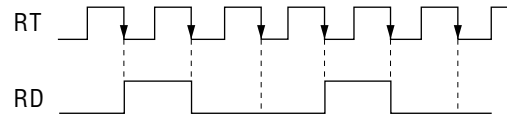
NC : No connect pin

PIN DESCRIPTION

<table>
<tr><th>Name</th><th>Description</th></tr>
<tr><td>X1</td><td rowspan="2">Crystal connection pins.
A 3.6864 MHz or 7.3728 MHz crystal shall be connected.
When an external clock is applied for MSM6882's oscillation source, it has to be input to X2.
In this case, X2 has to be AC-coupled by the capacitor of 200 pF. X1 shall be left open.</td></tr>
<tr><td>X2</td></tr>
<tr><td>MCS</td><td>Master clock selection.
<table><tr><th>MCS</th><th>Crystal or External Clock</th></tr><tr><td>0</td><td>3.6864 MHz</td></tr><tr><td>1</td><td>7.3728 MHz</td></tr></table></td></tr>
<tr><td>ME</td><td>Modulator enable.
When a "high" is input on this pin, MSK modulator output is connected to the input of transmit LPF.
When a "low" is input on this pin, TI is connected to the input of transmit LPF.</td></tr>
<tr><td>SD</td><td>Send data input.
The data on this pin is synchronized with the rising edge of ST and input to MSK modulator as an actual transmit data.
 
</td></tr>
<tr><td>ST</td><td>This timing signal is used to latch serial input data on the SD pin.
The frequency of ST coincides with the transmission bit rate.</td></tr>
<tr><td>SIN</td><td>Modulation method selection.
Data put on this pin selects either SINE FAST FSK or COSINE FAST FSK.
 
</td></tr>
<tr><td>PRE</td><td>Preamble or data transmission selection.
When a "low" is input on this pin, the data put on the SD pin is output on the AO pin.
When a "high" is input on this pin, the data put on the SD pin is neglected and preamble data is output.
Data put on PRE is latched on the rising edge of ST.
Preamble means to modulate as 010101...pattern.</td></tr>
</table>

<table>
<tr><th>Name</th><th>Description</th></tr>
<tr><td>BR</td><td>Baud rate selection.
<table>
<tr><th rowspan="2">Master Clock (MHz)</th><th rowspan="2">MCS</th><th rowspan="2">BR</th><th rowspan="2">Bit Rate (bps)</th><th colspan="2">Carrier Freq. (Hz)</th></tr>
<tr><th>Mark</th><th>Space</th></tr>
<tr><td rowspan="2">7.3728</td><td>1</td><td>1</td><td>2400</td><td>1200</td><td>2400</td></tr>
<tr><td>1</td><td>0</td><td>1200</td><td>1200</td><td>1800</td></tr>
<tr><td>3.6864</td><td>0</td><td>0</td><td>1200</td><td>1200</td><td>1800</td></tr>
<tr><td rowspan="2">3.6864</td><td>1</td><td>1</td><td>1200</td><td>600</td><td>1200</td></tr>
<tr><td>1</td><td>0</td><td>600</td><td>600</td><td>900</td></tr>
</table></td></tr>
<tr><td>SG</td><td>Built-in analog signal ground.
The DC voltage is approximately half of V_{DD}, so the analog interfaces signals of AI, AO, and TI with peripheral circuits which must be implemented by AC-coupling. To make this voltage source impedance lower and ensure the device performance of this device, more than 0.1 μF bypass capacitors should be connected from SG to GND and from SG to V_{DD}.</td></tr>
<tr><td>GND</td><td>Ground. (0 V)</td></tr>
<tr><td>TI</td><td>Voice signal input.
The signal input to this pin can be sent out to AO through the transmit LPF, the characteristics of which, gives the splatter filter for voice band signal.
When this function is used, digital "0" must be input to ME.
TI is biased to SG through internal resistor.</td></tr>
<tr><td>AO</td><td>Transmit analog signal output.
The data put on ME and $\overline{FT}$ can set the status of AO as follows.
<table>
<tr><th>$\overline{FT}$</th><th>ME</th><th>Transmit LPF</th><th>State of AO</th></tr>
<tr><td>"1"</td><td>"1"</td><td rowspan="2">Power On</td><td>MSK Signal</td></tr>
<tr><td>"1"</td><td>"0"</td><td>Voice Signal</td></tr>
<tr><td>"0"</td><td>"1"</td><td rowspan="2">Power Down</td><td>The Output of Receive BPF</td></tr>
<tr><td>"0"</td><td>"0"</td><td>No-signal (SG level)</td></tr>
</table>


The state when $\overline{FT}$ and ME = "0" is shown above. When the input digital data on $\overline{FT}$ changes to "1" from "0", AO remains to be connected to SG during about 2 ms and after that, and AO is switched to transmit LPF.
This delay time prevents AO from outputting meaningless signal during transient time from power down to on of LPF.</td></tr>
</table>

<table>
<tr><th>Name</th><th>Description</th></tr>
<tr><td>AI</td><td>Receive analog signal input.
AI is biased internally to SG with about 100 kΩ same as TI.</td></tr>
<tr><td>CDT</td><td>Device test.
This pin should be connected to GND.</td></tr>
<tr><td>CDO</td><td>Device test.
This pin should be opened.</td></tr>
<tr><td>RD</td><td>Demodulated serial data output.
This data is synchronized with the re-generated timing clock RT.</td></tr>
<tr><td>RT</td><td>Receive data timing clock output.
This signal is re-generated by internal digital PLL.
Synchronizing to negative edge of RT, RD is output.
 
</td></tr>
<tr><td>CF</td><td>Receive data timing clock is re-generated by digital PLL of which phase correcting speed can be selected with CF.
When a digital "1" is put on CF and phase difference between receive data timing and RT is more than 22.5 degree, phase correcting speed is high. In this case, as the phase difference enters within 22.5 degrees, that speed changes to low immediately.
When digital "0" is input to CF, phase correcting speed of PLL remains low regardless of the phase difference.
Usually, CF is connected to digital "1".</td></tr>
<tr><td>CT</td><td>PLL's lock-in characteristics can be selected with CT.
When digital "1" is put on CT, PLL requires max. 50 bit alternative data pattern. On the other hand, when digital "0" is input to CT,
PLL can be locked in below 18-bit data.
<table>
<tr><th>CF</th><th>CT</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td>1</td><td>0</td><td>—</td><td>—</td><td>18</td><td rowspan="2">bit</td></tr>
<tr><td>1</td><td>1</td><td>—</td><td>—</td><td>50</td></tr>
</table></td></tr>
<tr><td>$\overline{FT}$</td><td>Control signal for the internal connection of AO.
Refer to column AO.
When digital "0" is input to this pin, transmit LPF enters in power down mode, but the output buffer operational amplifier remains active. In this case, AO is at SG level.</td></tr>
<tr><td>V_{DD}</td><td>Power supply.
MSM6882-3: 3.6 V
MSM6882-5: 5 V
This device is sensitive to supply noise as switched capacitor techniques are utilized.
A bypass capacitor of more than 2.2 μF between V_{DD} and GND is indispensable to ensure the performance.</td></tr>
</table>

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C With respect to GND	–0.3 to 7.0	V
Input Voltage *1	V_I		–0.3 to V_{DD} + 0.3	
Operating Temperature	T_{op}	—	–25 to 70	°C
Storage Temperature	T_{STG}	—	–55 to 150	

*1 MCS, ME, SD, SIN, PRE, BR, TI, AI, CDT, CF, CT, $\overline{FT}$

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Condition		Min.	Typ.	Max.	Unit
Power Supply Voltage		V_{DD}	With respect to GND	*1	3.0	3.6	4.0	V
				*2	4.5	5	5.5	
		GND	—		—	0	—	
Operating Temperature		T_{op}	—		–25	25	70	°C
Crystal Resonant Frequency		$f_{X'TAL}$	MCS = "1"		7.3721	7.3728	7.3735	MHz
			MCS = "0"		3.6860	3.6864	3.6868	
Data Speed		T_S	MCS = "1", BR = "1"		—	2400	—	bit/sec
			BR = "0"		—	1200	—	
C1		—	—		—	2.2	—	µF
C2		—	—		—	0.1	—	
C3		—	—		—	0.047	—	
C4		—	$R_{LX} \geq 40$ kΩ		—	0.047	—	
C5		—	—		—	0.047	—	
C6		—	—		—	0.1	—	
Crystal	Oscillation Frequency	—	—		—	7.3728	—	MHz
	Frequency Deviation	—	25 ±5°C		–100	—	+100	ppm
	Temperature Characteristics	—	At –30°C to +70°C		–100	—	+100	
	Equivalent Series Resistance	—	—		—	—	50	Ω
	Load Capacitance	—	—		—	16	—	pF
Crystal	Oscillation Frequency	—	—		—	3.6864	—	MHz
	Frequency Deviation	—	25 ±5°C		–100	—	+100	ppm
	Temperature Characteristics	—	At –30°C to +70°C		–100	—	+100	
	Equivalent Series Resistance	—	—		—	—	100	Ω
	Load Capacitance	—	—		—	16	—	pF

*1 MSM6882-3
*2 MSM6882-5

ELECTRICAL CHARACTERISTICS

DC Characteristics

(MSM6882-3: V_{DD} = 3 V to 4 V, Ta = –25°C to 70°C)
(MSM6882-5: V_{DD} = 5 V ±0.5 V, Ta = –25°C to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current *1	I_{DD}	Normal Operating Mode	—	4	8	mA
		$\overline{FT}$ = "1"	—	5.5	11	
	I_{DDS}	Power Down Mode	—	3.5	7	
		$\overline{FT}$ = "0"	—	5.0	10	
Input Leakage Current *2	I_{IL}	V_{IN} = 0 V	–10	—	10	µA
	I_{IH}	V_{IN} = V_{DD}	–10	—	10	
Input Voltage *2	V_{IL}	*1	0	—	0.6	V
					0.8	
	V_{IH}	*1	1.8	—	V_{DD}	
			2.2			
Output Voltage *1 *3	V_{OL1}	I_{OL} = 10 µA/1.6 mA	0	—	0.3	
					0.4	
	V_{OH1}	I_{OH} = 10 µA/400 µA	0.8V_{DD}	—	V_{DD}	

*1 Upper is specified for the MSM6882-3, lower for the MSM6882-5
*2 MCS, ME, SD, SIN, PRE, BR, CF, CT, $\overline{FT}$
*3 ST, RD, RT

Digital Interface Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Data Set-up Time	t_S	See Fig.1	300	—	—	ns
Input Data Hold Time	t_H		300	—	—	ns
Output Data Delay Time	t_D	See Fig.2	–300	—	300	ns

Analog Interface Characteristics

Transmit signal output (AO)

(MSM6882-3: V_{DD} = 3 V to 4 V, Ta = –25°C to 70°C)
(MSM6882-5: V_{DD} = 5 V ±0.5 V, Ta = –25°C to 70°C)

Parameter		Symbol	Condition			Min.	Typ.	Max.	Unit
Carrier Frequency	1200 bps	f_{M1}	$\overline{FT}$ = "1"	BR = "0"	SD = "1"	1199	1200	1201	Hz
		f_{S1}			SD = "0"	1799	1800	1801	
	2400 bps	f_{M2}	ME = "1"	BR = "1"	SD = "1"	1199	1200	1201	
		f_{S2}			SD = "0"	2399	2400	2401	
Carrier Level	*1	V_{OX}	$R_L \geq 40$ kΩ		$\overline{FT}$ = "1"	–7	–3	–1	dBm
					ME = "1"	–3	0	2	*2
Output Amplitude	*1	V_{OPP}	$C_L \leq 40$ pF		$\overline{FT}$ = "1"	1.4	2.0	—	V_{p-p}
					ME = "0"	2.2	3.0	—	
Output Resistance		R_{OX}	—			—	50	—	Ω
Output Load Resistance		R_{LX}	—			40	—	—	kΩ
Output Load Capacitance		C_{LX}	—			—	—	40	pF
Output DC Voltage		V_{OSX}	—			$0.48V_{DD}$	$0.50V_{DD}$	$0.52V_{DD}$	V

Voice signal input (TI)

Parameter		Symbol	Condition		Min.	Typ.	Max.	Unit
Voltage Gain		GT	V_{AO}/V_{TI}	$\overline{FT}$ = "1" ME = "0"	–2	0	+2	dB
Input Signal Level	*1	V_{TI}	—		—	—	–4	dBm
							0	*2
Input Resistance		R_{TI}	$f_{TI} \leq 4$ kHz		40	100	300	kΩ

Built-in signal ground (SG)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DC Voltage	V_{SG}	Without DC Load	$0.48V_{DD}$	$0.50V_{DD}$	$0.52V_{DD}$	V

Receive signal input (AI)

Parameter		Symbol	Condition			Min.	Typ.	Max.	Unit
Input Resistance		R_{AI}	$f_{AI} \leq 4$ kHz			40	100	300	kΩ
Receive Signal Level		V_{IR1}	—		BR = "0"	–30	—	0	dBm
		V_{IR2}			BR = "1"	–24	—	0	*2
Bit Error Rate	1200 bps	BER	S/N at AI SIN = "1"	S/N	7 dB	—	2×10^{-3}	—	
					11 dB	—	2×10^{-5}	—	
	2400 bps				10 dB	—	2×10^{-3}	—	
					14 dB	—	2×10^{-5}	—	

*1 Upper is specified for the MSM6882-3, lower for the MSM6882-5
*2 0 dBm = 0.775 Vrms

Re-generated receive data timing clock output (RT)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
Data Bit Number for PLL' Lock-in	N_{PLL1}	CF = "1"	CT= "0"	*3	—	—	18	bit
	N_{PLL2}		CT= "1"		—	—	50	

*3 Data bit number to lock-in within 22.5 degree

TIMING DIAGRAM

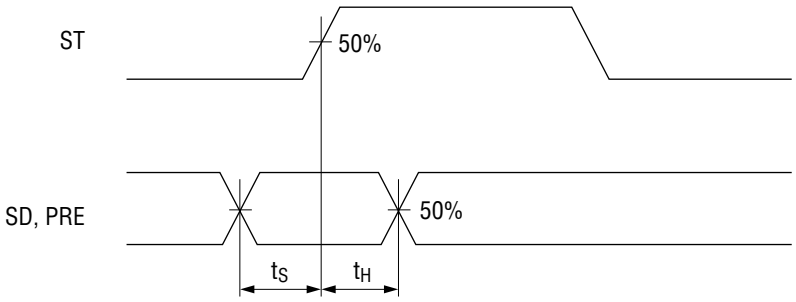


Figure 1 Input Data Timing

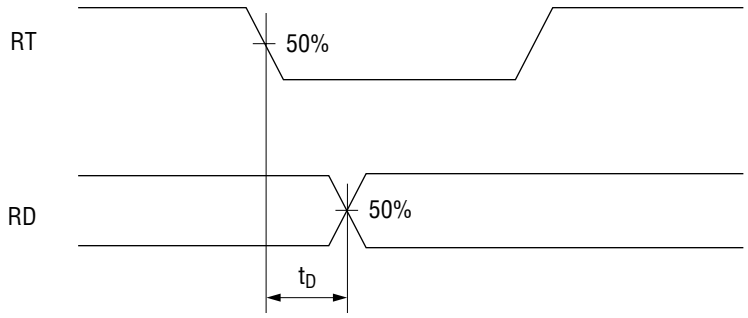
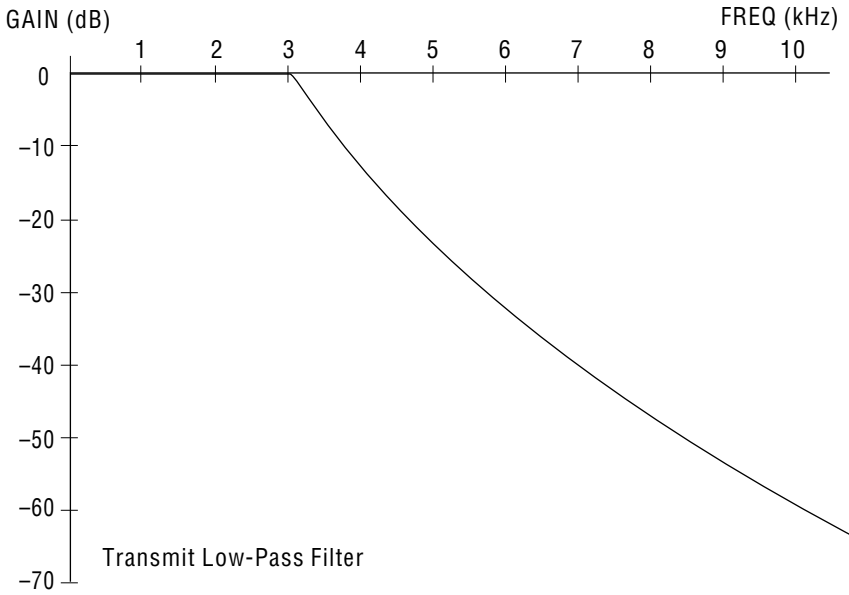
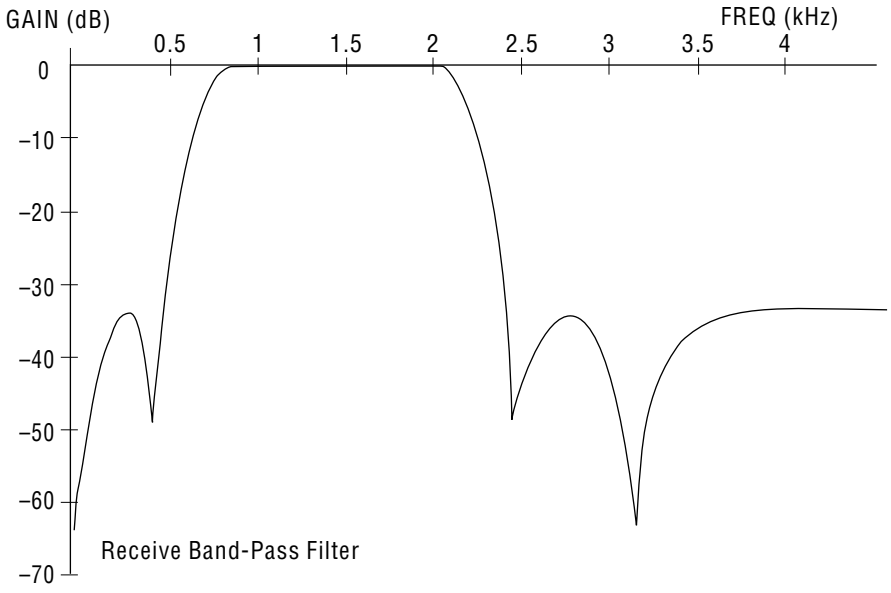


Figure 2 Output Data Timing

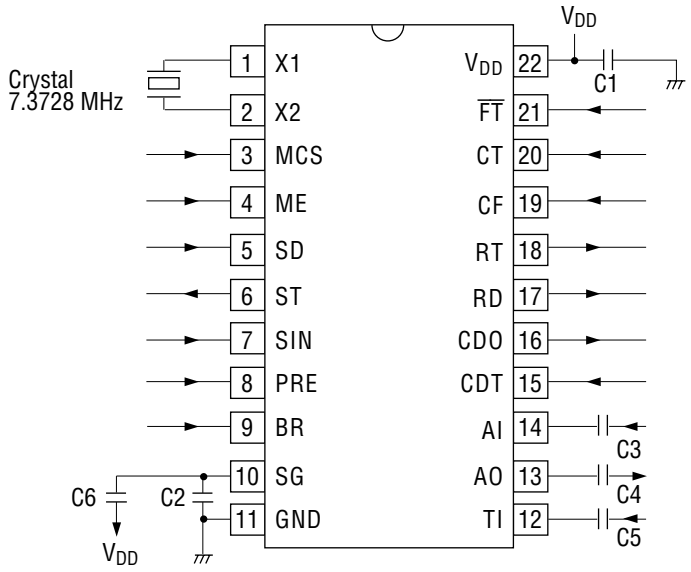
BUILT-IN FILTER FREQUENCY CHARACTERISTICS





Note: When BR = "1", frequency converter circuit (MIXER) is prepared before the receive BPF. Therefore, 1200 Hz input signal is converted to 3600 Hz at BPF output for example.

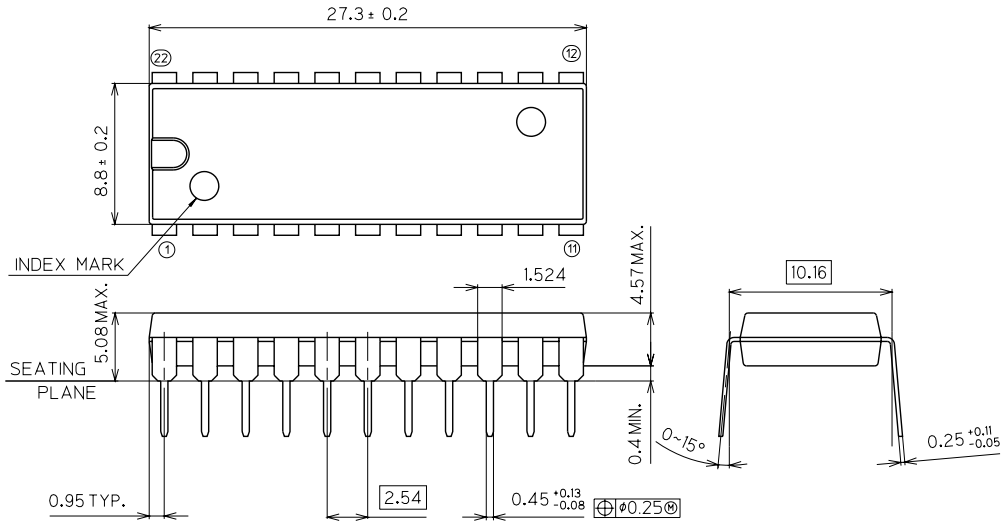
APPLICATION CIRCUIT



PACKAGE DIMENSIONS

(Unit : mm)

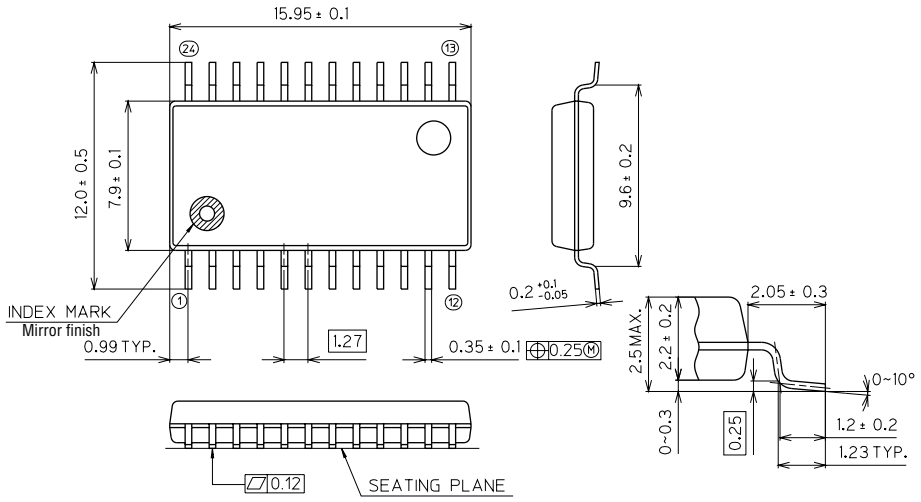
DIP22-P-400-2.54



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.90 TYP.

(Unit : mm)

SOP24-P-430-1.27-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.58 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).