CMOS LSI

SANYO No.※3886

LC78850, LC78850Q

Two-channel, 16- and 18-bit D/A Converters for Digital Audio

Preliminary

OVERVIEW

The LC78850 and LC78850Q are two-channel, 16- and 18-bit D/A converters with PWM outputs for use in digital audio equipment.

The LC78850 and LC78850Q feature 0.003% total harmonic distortion, 100 dB channel separation and a 100 dB signal-to-noise ratio.

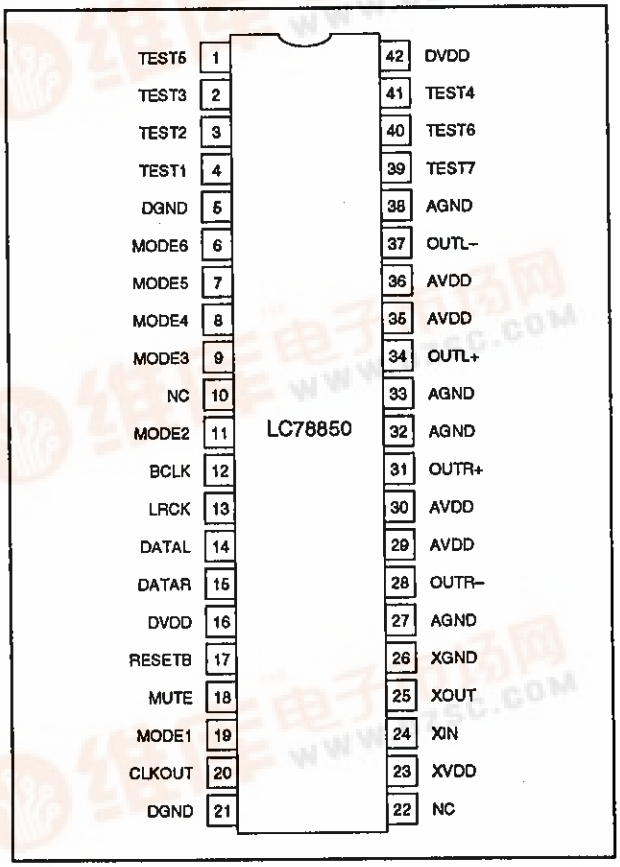
The LC78850 and LC78850Q input four-times and eight-times oversampled digital signals, perform digital signal processing on the data and, after lowpass filtering, output high-fidelity analog reproductions of the original waveforms. Input format options include 16- and 18-bit data lengths, msb- and lsb-first data, and 384fs and 512fs bit rates.

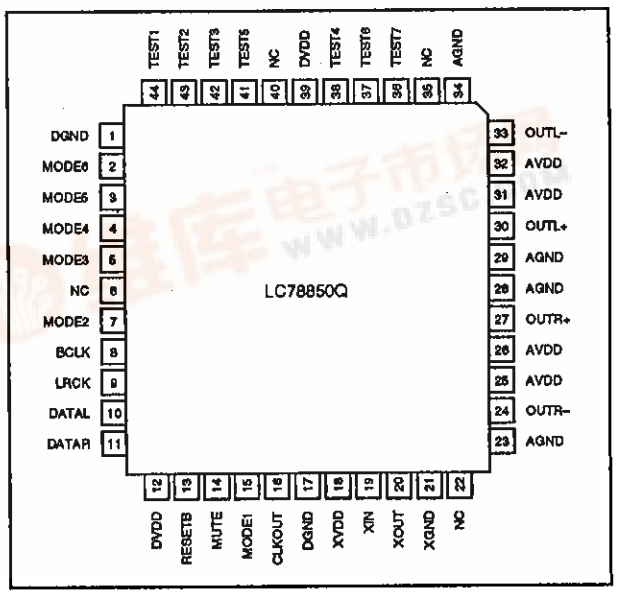
The LC78850 and LC78850Q operate from a 5 V supply and are available in 42-pin shrink DIPs and 44-pin QIPs, respectively.

FEATURES

- Two-channel, 16- and 18-bit D/A converters
- 0.003% total harmonic distortion
- 100 dB channel separation
- 100 dB signal-to-noise ratio
- Four- or eight-times oversampled serial data
- msb-first and lsb-first data formats
- 384fs and 512fs bit rates
- PWM outputs
- Silicon-gate CMOS process
- 5 V supply
- 42-pin shrink DIP (LC78850) and 44-pin QIP (LC78850Q)

PINOUT





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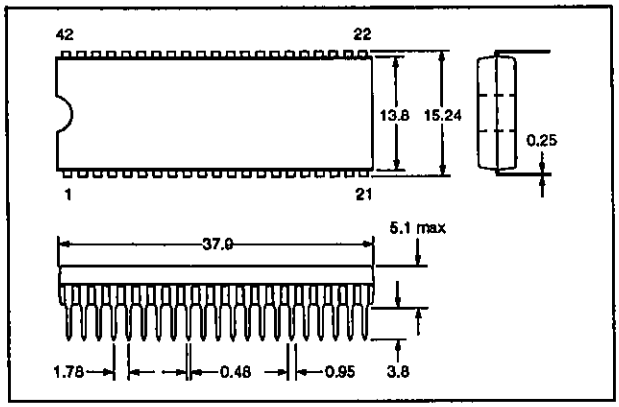
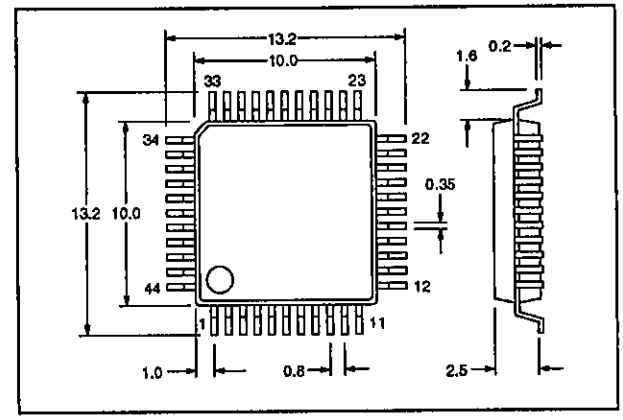
PACKAGE DIMENSIONS

Unit: mm

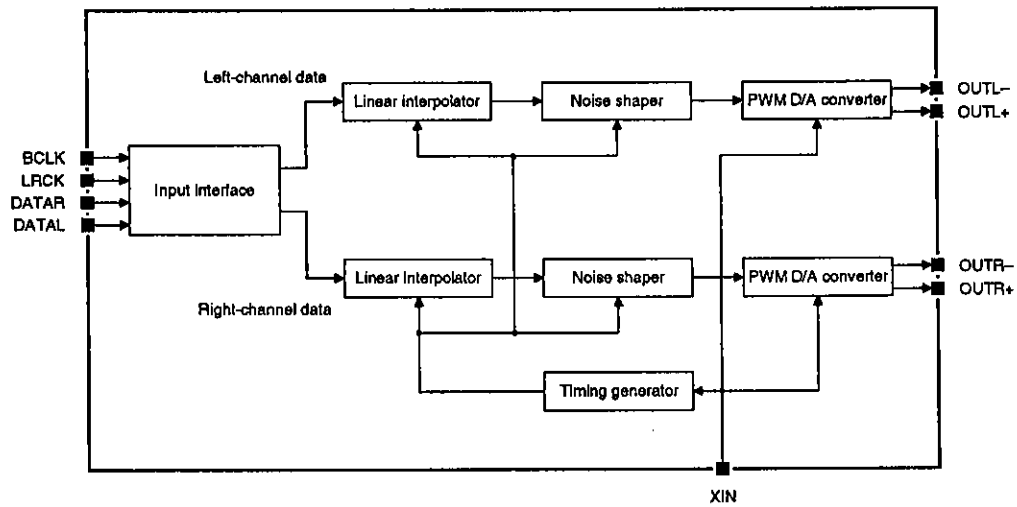
3025B-DIP42S (LC78850)



3148-QIP44MA (LC78850Q)



BLOCK DIAGRAM



PIN DESCRIPTION

Number		Name	Description
QIP	DIP		
1, 17	5, 21	DGND	Digital ground
2	6	MODE6	LRCK rising-edge/falling-edge select input
3	7	MODE5	I^2S format select input
4	8	MODE4	Serial data msb-first/lsb-first select input
5	9	MODE3	Data length select input
6, 22, 35, 40	10, 22	NC	No connection
7	11	MODE2	Sampling rate select input
8	12	BCLK	Serial data bit-clock input
9	13	LRCK	Serial data left-channel/right-channel clock input
10	14	DATAL	Left-channel serial data input

Number		Name	Description
QIP	DIP		
11	15	DATAR	Right-channel serial data input
12, 39	16, 42	DVDD	5 V digital supply
13	17	RESETB	Active-LOW reset input
14	18	MUTE	Mute input
15	19	MODE1	System clock frequency select input
16	20	CLKOUT	System clock output
18	23	XVDD	5 V oscillator amplifier supply
19	24	XIN	Crystal oscillator or external clock connection
20	25	XOUT	Crystal oscillator connection
21	26	XGND	Oscillator amplifier ground
23, 28, 29, 34	27, 32, 33, 38	AGND	Analog ground
24	28	OUTR–	Right-channel, negative PWM output
25, 26, 31, 32	29, 30, 35, 36	AVDD	5 V analog supply
27	31	OUTR+	Right-channel, positive PWM output
30	34	OUTL+	Left-channel, positive PWM output
33	37	OUTL–	Left-channel, negative PWM output
36	39	TEST7	Test inputs
37	40	TEST6	
38	41	TEST4	Test input and right-channel mute output
41	1	TEST5	Test output
42	2	TEST3	Test input
43	3	TEST2	Test input and left-channel mute output
44	4	TEST1	Test input

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7	V
Input voltage range	V_I	–0.3 to V_{DD} + 0.3	V
Output voltage range	V_O	–0.3 to V_{DD} + 0.3	V
Operating temperature range	Topr	–30 to 75	°C
Storage temperature range	T_{stg}	–40 to 125	°C

Recommended Operating Conditions

T_a = 25 °C

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	5	V
Supply voltage range	V_{DD}	4.5 to 5.5	V

DC Electrical Characteristics

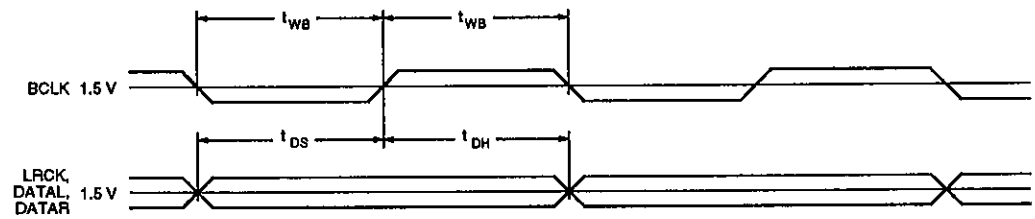
V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –30 to 75 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Power dissipation	P_D	V_{DD} = 5 V, f_{max} = 16.9344 MHz	–	240	–	mW
XIN LOW-level input voltage	V_{IL1}		–	–	0.3V_{DD}	V
LOW-level input voltage for all other inputs	V_{IL2}		–	–	0.8	V
XIN HIGH-level input voltage	V_{IH1}		0.7V_{DD}	–	–	V
HIGH-level input voltage for all other inputs	V_{IH2}		2.2	–	–	V
LOW-level output voltage	V_{OL}	I_{OL} = 1 µA	–	–	0.1	V
HIGH-level output voltage	V_{OH}	I_{OH} = –1 µA	V_{DD} – 0.1	–	–	V

AC Electrical Characteristics

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –30 to 75 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Oscillator frequency	f_{max}		–	16.9344	25	MHz
BCLK frequency	f_{BCK}		–	–	12.5	MHz
BCLK pulsewidth	t_{WB}		30	–	–	ns
Data setup time	t_{DS}		15	–	–	ns
Data hold time	t_{DH}		15	–	–	ns



Analog Characteristics

V_{DD} = 5 V, T_a = 25 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Total harmonic distortion	THD	f = 1 kHz, 0 dB output	–	0.003	–	%
Signal-to-noise ratio	S/N	JIS* A-weighted filter	–	100	–	dB
Crosstalk	CT	f = 1 kHz, 0 dB output	–	100	–	dB
Full-scale output voltage	V_O		–	1.7	–	V_{rms}

* Japanese Industrial Standard

FUNCTIONAL DESCRIPTION

MODE1

Set MODE1 HIGH for a 512fs system clock, and LOW, for a 384fs clock.

MODE2

Set MODE2 HIGH for eight-times oversampled (8fs) input data, and LOW, for four-times oversampled (4fs) data.

MODE3

Set MODE3 HIGH for 18-bit input data, and LOW, for 16-bit data.

MODE4

Set MODE4 HIGH for msb-first data, and LOW, for lsb-first data.

MODE5

Set MODE5 HIGH for I²S format input data, and LOW, for standard format data.

MODE6

For eight-times oversampled data, set MODE6 HIGH if LRCK goes HIGH at the end of each sample, and LOW, if LRCK goes LOW.

For four-times oversampled data, set MODE6 HIGH if LRCK goes LOW at the end of left-channel samples and HIGH at the end of right-channel samples. Set MODE6 LOW, however, if LRCK goes HIGH at the end of left-channel samples and LOW at the end of right-channel samples.

TEST1 to TEST7

During normal operation, the test inputs should be tied to ground and the test output left open.

When TEST1 is LOW and TEST7 is HIGH, muting is ON, the left- and right-channel outputs are held at $0.5V_{DD}$ and mute signals to external circuitry are output on TEST2 and TEST4. TEST2 is the left-channel mute output, and TEST4 is the right-channel.

MUTE

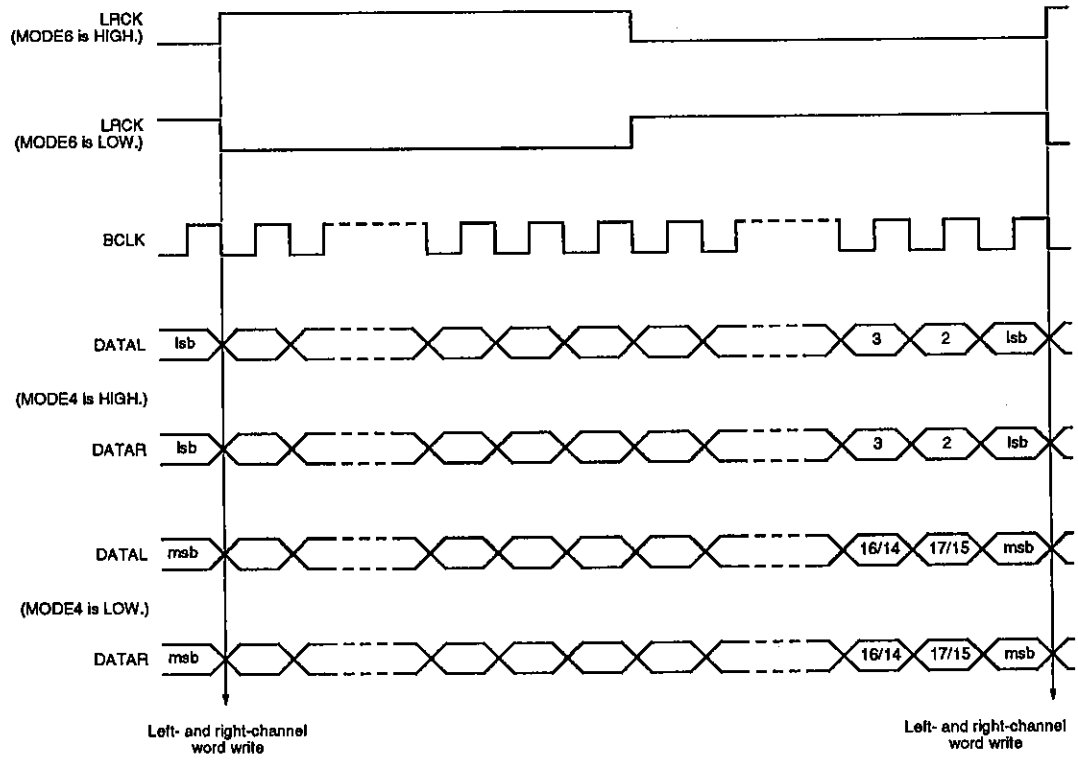
When MUTE is HIGH, muting is ON and the left- and right-channel outputs are held at $0.5V_{DD}$.

In normal mode (TEST1 and TEST7 are LOW), muting turns ON when the input data is zero for 2^{16} consecutive samples (approximately 0.37 s for four-times oversampled data when fs = 44.1 kHz).

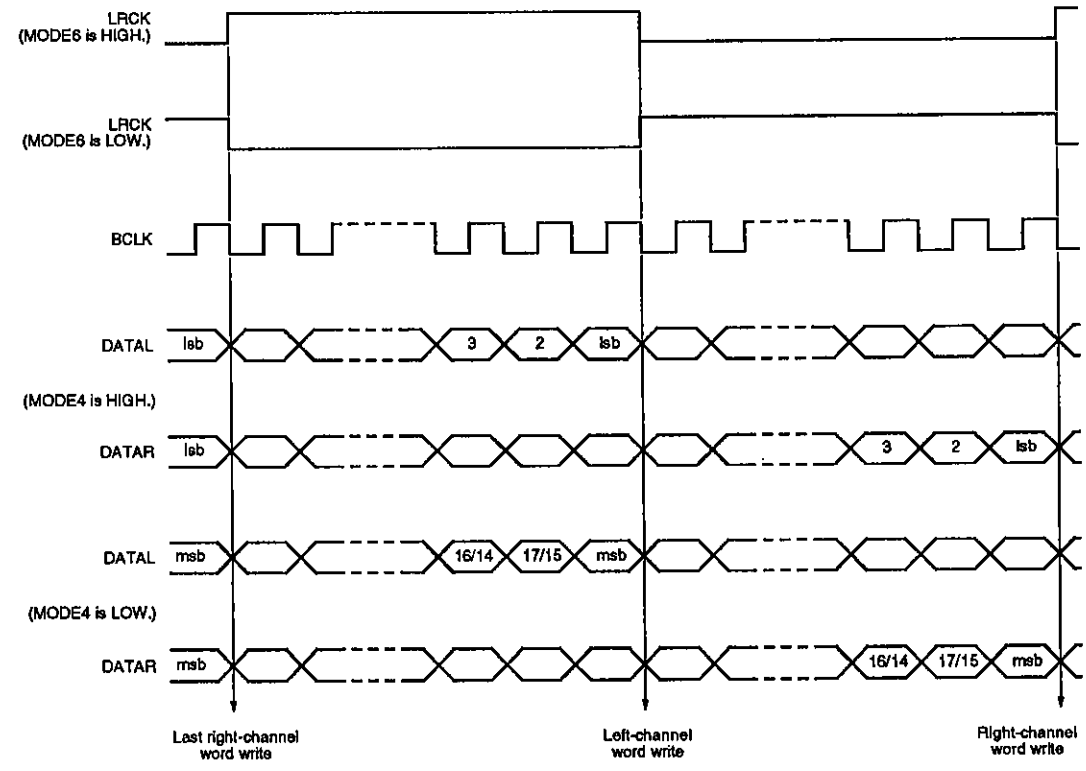
OPERATING INFORMATION

Input Waveforms

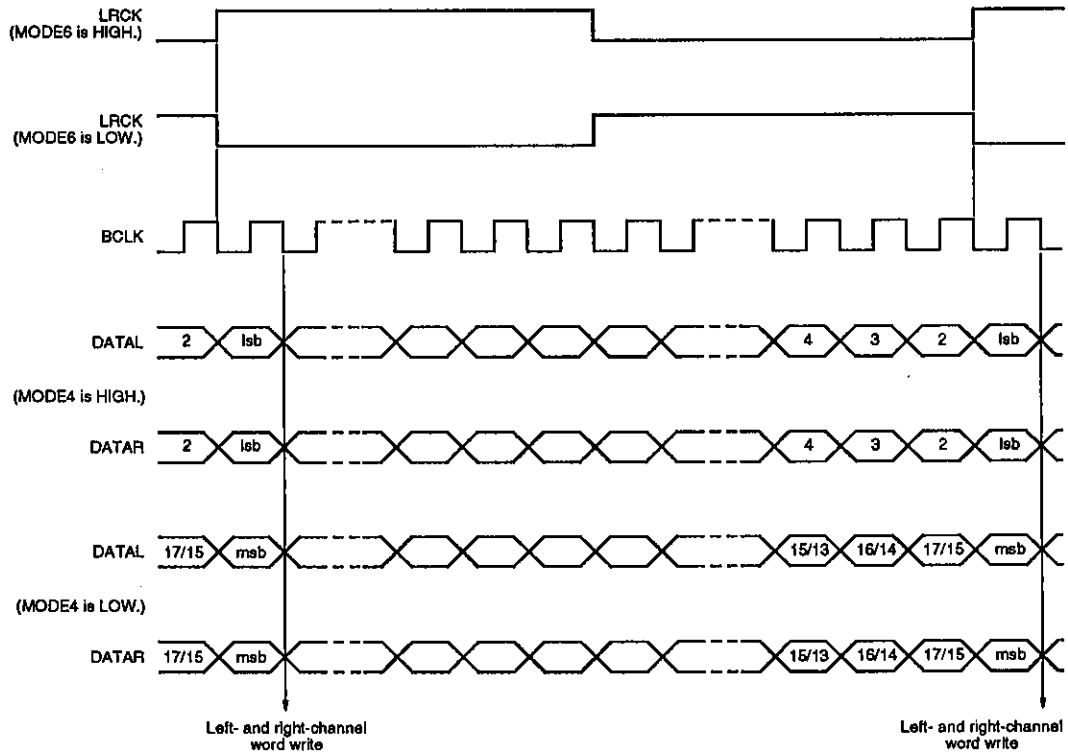
Standard format, eight-times oversampled data



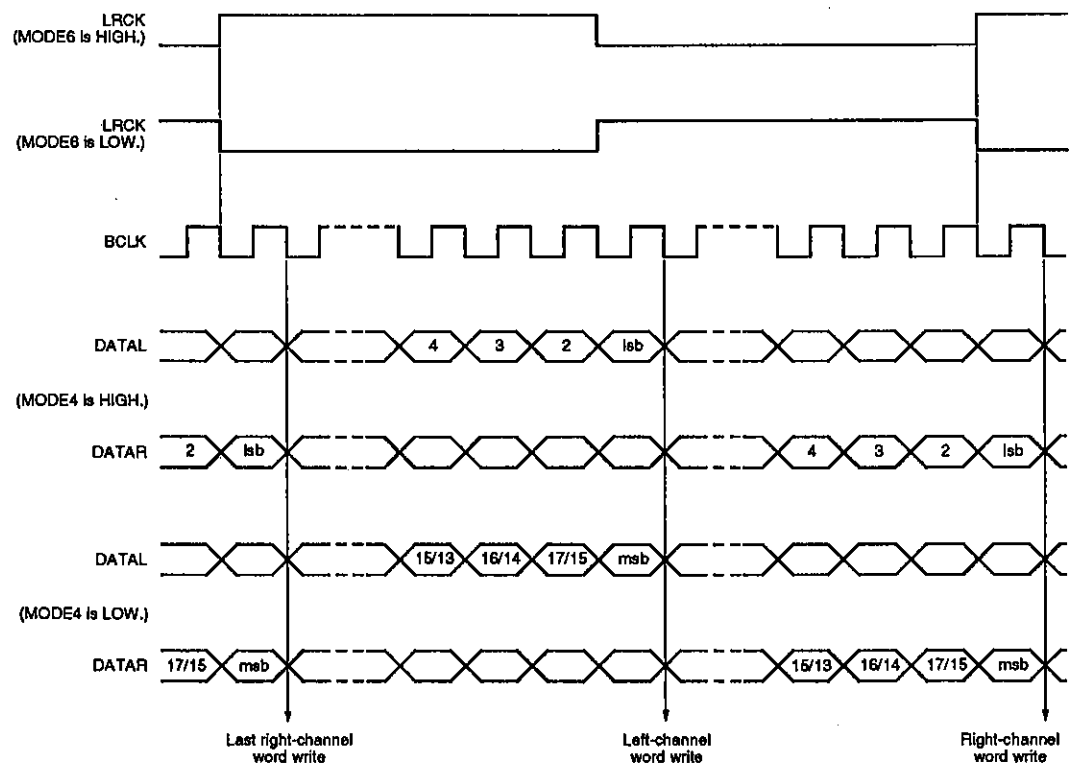
Standard format, four-times oversampled data



I²S format, eight-times oversampled data



I²S format, four-times oversampled data



TYPICAL APPLICATION