DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD8862

(2700 + 2700) PIXELS × 3 COLOR CCD LINEAR IMAGE SENSOR

DESCRIPTION

The μPD8862 is a color CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal and has the function of color separation.

The μPD8862 has 3 rows of (2700 + 2700) staggered pixels, and each row has a dual-sided readout-type charge transfer register. And it has reset feed-through level clamp circuits and voltage amplifiers. Therefore, it is suitable for 600 dpi/A4 color image scanners, color facsimiles and so on.

FEATURES

- Valid photocell : (2700 + 2700) staggered pixels × 3
- Photocell pitch : 5.25 μm
- Line spacing : 63 μm (12 lines) Red line - Green line, Green line - Blue line
  10.5 μm (2 lines) Odd line - Even line (for each color)
- Color filter : Primary colors (red, green and blue), pigment filter (with light resistance 10^7 lx•hour)
- Resolution : 24 dot/mm A4 (210 × 297 mm) size (shorter side)
  600 dpi US letter (8.5” × 11”) size (shorter side)
- Drive clock level : CMOS output under 5 V operation
- Data rate : 6 MHz Max.
- Power supply : +12 V
- On-chip circuits : Reset feed-through level clamp circuits
  Voltage amplifiers

ORDERING INFORMATION

Part Number	Package
μPD8862CY	CCD linear image sensor 22-pin plastic DIP (10.16 mm (400))

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

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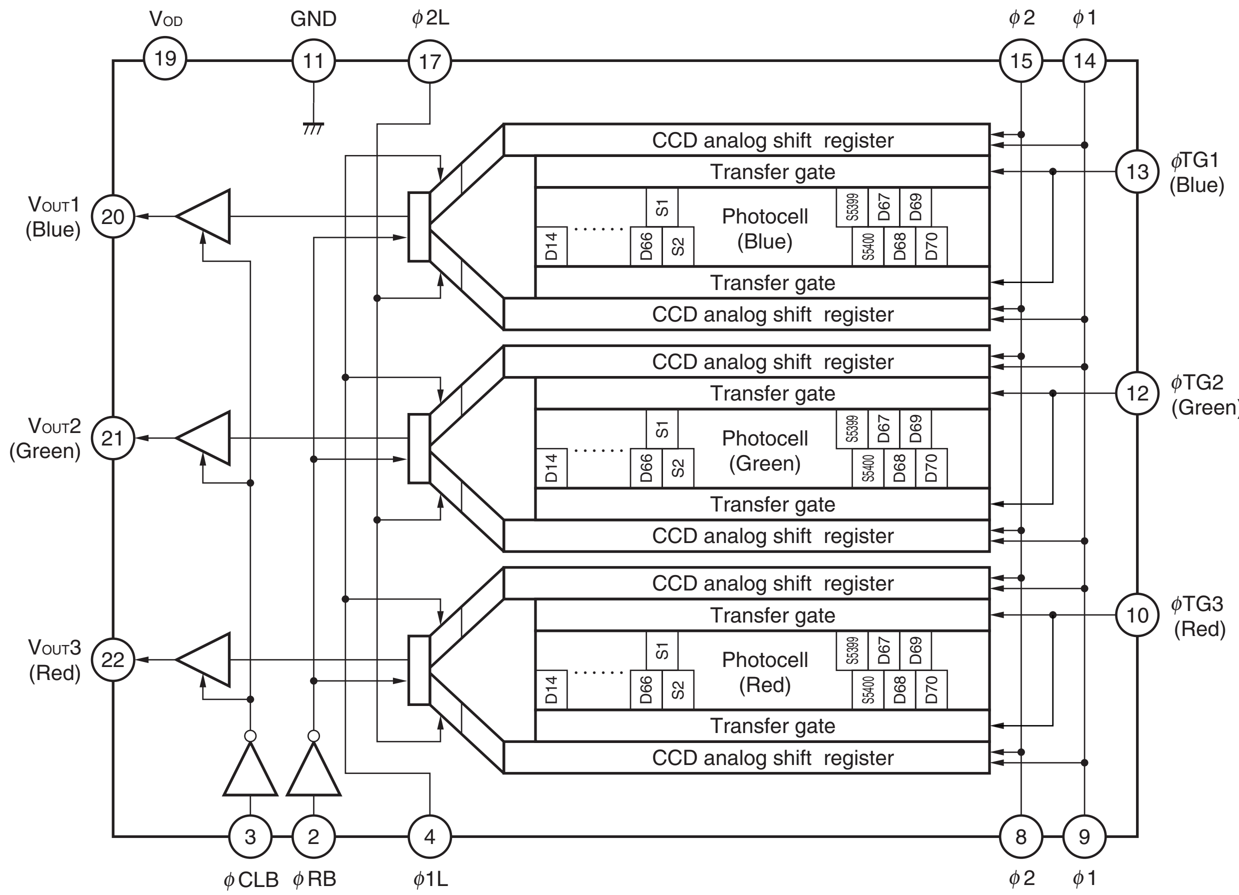
The mark ★ shows major revised points.

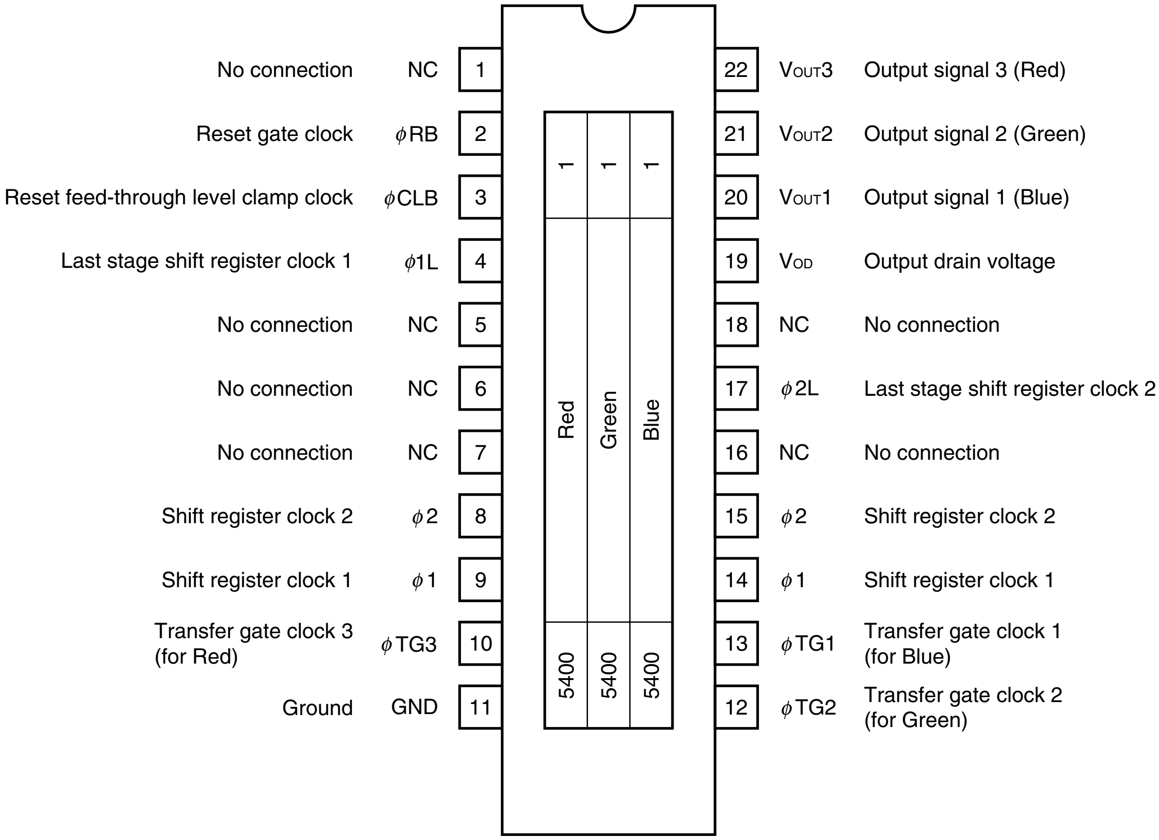
BLOCK DIAGRAM



PIN CONFIGURATION (Top View)

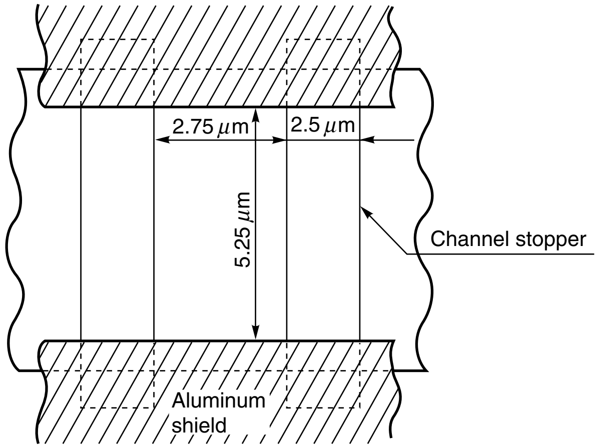
CCD linear image sensor 22-pin plastic DIP (10.16 mm (400))

• μPD8862CY

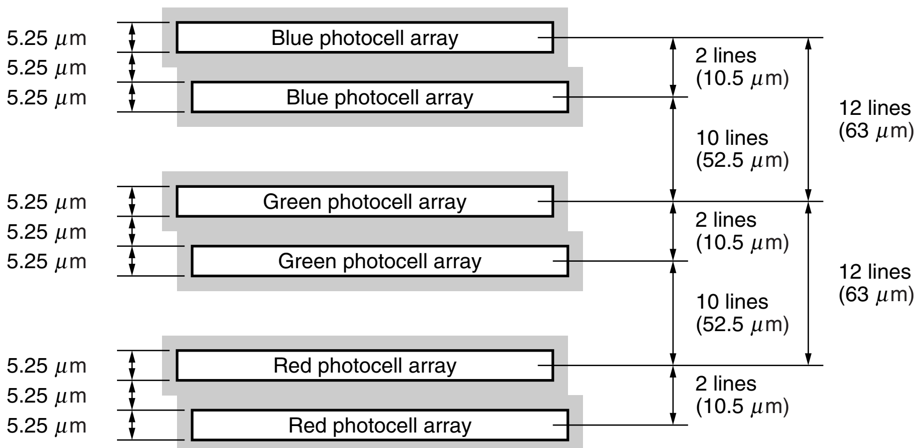


Caution Connect the No connection pins (NC) to GND.

PHOTOCELL STRUCTURE DIAGRAM



PHOTOCELL ARRAY STRUCTURE DIAGRAM (Line spacing)



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V_{OD}	–0.3 to +15	V
Shift register clock voltage	$V_{\phi 1}$, $V_{\phi 2}$, $V_{\phi 1L}$, $V_{\phi 2L}$	–0.3 to +8	V
Reset gate clock voltage	$V_{\phi RB}$	–0.3 to +8	V
Reset feed-through level clamp clock voltage	$V_{\phi CLB}$	–0.3 to +8	V
Transfer gate clock voltage	$V_{\phi TG1}$ to $V_{\phi TG3}$	–0.3 to +8	V
Operating ambient temperature[Note]	T_A	0 to +60	°C
Storage temperature	T_{stg}	–40 to +70	°C

Note Use at the condition without dew condensation.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

RECOMMENDED OPERATING CONDITIONS (T_A = +25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output drain voltage	V_{OD}	11.4	12.0	12.6	V
Shift register clock high level	$V_{\phi 1\_H}$, $V_{\phi 2\_H}$, $V_{\phi 1LH}$, $V_{\phi 2LH}$	4.75	5.0	5.5	V
Shift register clock low level	$V_{\phi 1\_L}$, $V_{\phi 2\_L}$, $V_{\phi 1LL}$, $V_{\phi 2LL}$	–0.3	0	+0.25	V
Reset gate clock high level	$V_{\phi RBH}$	4.5	5.0	5.5	V
Reset gate clock low level	$V_{\phi RBL}$	–0.3	0	+0.5	V
Reset feed-through level clamp clock high level	$V_{\phi CLBH}$	4.5	5.0	5.5	V
Reset feed-through level clamp clock low level	$V_{\phi CLBL}$	–0.3	0	+0.5	V
Transfer gate clock high level	$V_{\phi TG1H}$ to $V_{\phi TG3H}$	4.75	$V_{\phi 1\_H}$[Note]	$V_{\phi 1\_H}$[Note]	V
Transfer gate clock low level	$V_{\phi TG1L}$ to $V_{\phi TG3L}$	–0.3	0	+0.15	V
Data rate	$f_{\phi RB}$	–	2.0	6.0	MHz

Note When Transfer gate clock high level ($V_{\phi TG1H}$ to $V_{\phi TG3H}$) is higher than Shift register clock high level ($V_{\phi 1\_H}$), Image lag can increase.

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, V_{OD} = 12 V, data rate ($f_{\phi RB}$) = 2 MHz, storage time = 5.5 ms, input signal clock = 5 V_{p-p},
light source : 3200 K halogen lamp + C-500S (infrared cut filter, t = 1 mm) + HA-50 (heat absorbing filter, t = 3 mm))

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Saturation voltage		V_{sat}		2.0	2.5	–	V
Saturation exposure	Red	SER		–	0.421	–	lx•s
	Green	SEG		–	0.477	–	lx•s
	Blue	SEB		–	0.740	–	lx•s
Photo response non-uniformity		PRNU	V_{OUT} = 1.0 V	–	6	20	%
Average dark signal		ADS	Light shielding	–	0.2	2.0	mV
Dark signal non-uniformity		DSNU	Light shielding	–	1.5	5.0	mV
Power consumption		P_W		–	360	540	mW
Output impedance		Z_O		–	0.35	1	kΩ
Response	Red	R_R		4.15	5.94	7.73	V/lx•s
	Green	R_G		3.66	5.24	6.82	V/lx•s
	Blue	R_B		2.36	3.38	4.39	V/lx•s
Image lag		IL	V_{OUT} = 1.0 V	–	3.0	7.0	%
Offset level Note 1		V_{OS}		4.5	6.0	7.5	V
Output fall delay time Note 2		t_d	V_{OUT} = 1.0 V, t1', t2' = 5 ns	–	25	–	ns
Total transfer efficiency		TTE	V_{OUT} = 1.0 V, data rate = 6 MHz	92	98	–	%
Register imbalance		RI	V_{OUT} = 1.0 V	–	1.0	4.0	%
Response peak	Red			–	630	–	nm
	Green			–	540	–	nm
	Blue			–	460	–	nm
Dynamic range		DR1	V_{sat}/DSNU	–	1666	–	times
		DR2	V_{sat}/σCDS	–	2500	–	times
Reset feed-through noise Note 1		RFTN	Light shielding	–2000	+300	+1000	mV
Random noise (CDS)		σCDS	Light shielding	–	1.0	–	mV

Notes 1. Refer to **TIMING CHART 2, 3**.

2. When each fall time of ϕ1L and ϕ2L (t1', t2') is the Typ. value (refer to **TIMING CHART 2, 3**).

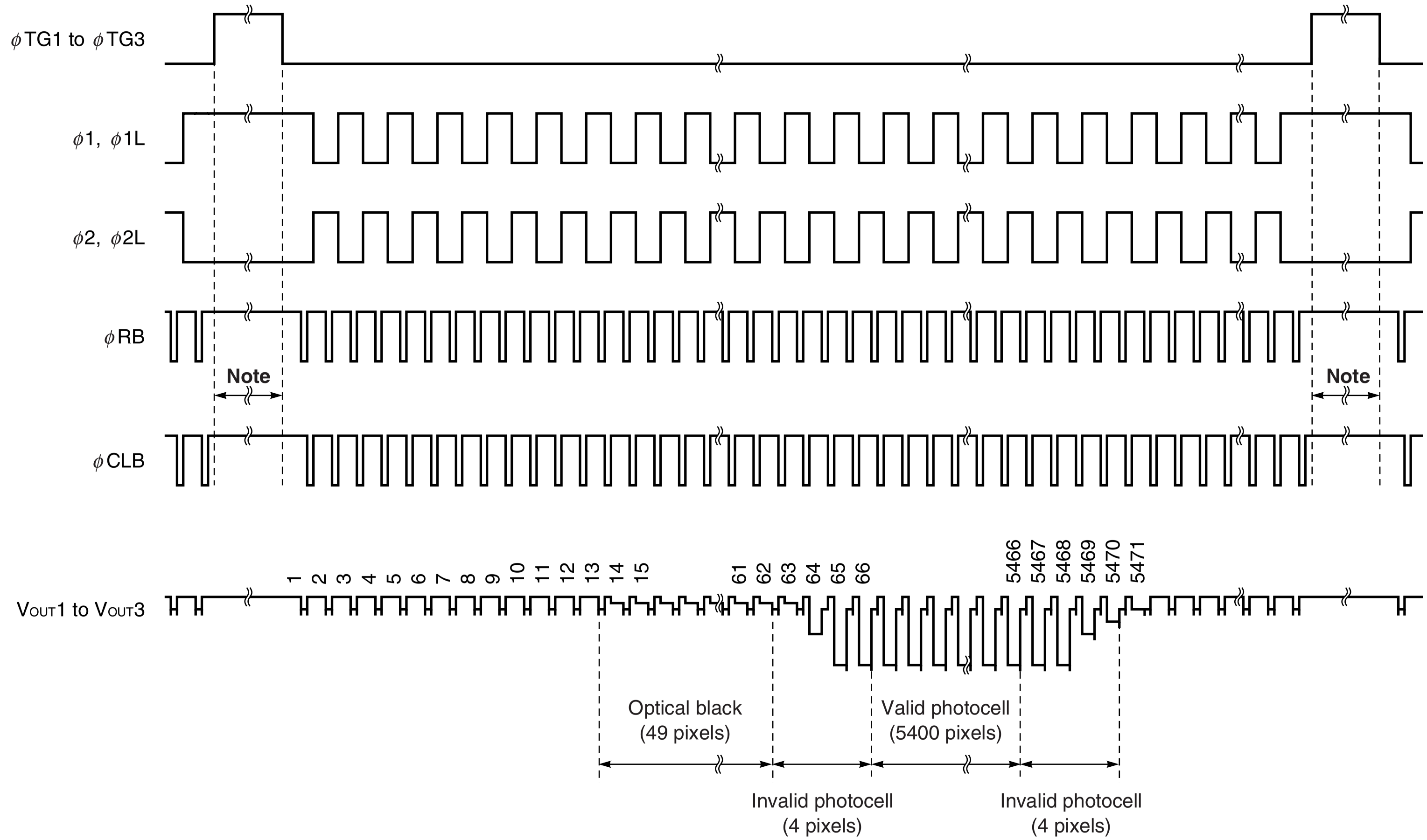
INPUT PIN CAPACITANCE (T_A = +25°C, V_{OD} = 12 V)

Parameter	Symbol	Pin name	Pin No.	Min.	Typ.	Max.	Unit
Shift register clock pin capacitance 1	$C_{\phi 1}$	ϕ1	9	–	250	–	pF
			14	–	250	–	pF
★	ϕ1 total capacitance			–	500	–	pF
Shift register clock pin capacitance 2	$C_{\phi 2}$	ϕ2	8	–	250	–	pF
			15	–	250	–	pF
★	ϕ2 total capacitance			–	500	–	pF
Last stage shift register clock pin capacitance	$C_{\phi L}$	ϕ1L	4	–	10	–	pF
		ϕ2L	17	–	10	–	pF
Reset gate clock pin capacitance	$C_{\phi RB}$	ϕRB	2	–	10	–	pF
Reset feed-through level clamp clock pin capacitance	$C_{\phi CLB}$	ϕCLB	3	–	10	–	pF
Transfer gate clock pin capacitance	$C_{\phi TG}$	ϕTG1	13	–	100	–	pF
		ϕTG2	12	–	100	–	pF
		ϕTG3	10	–	100	–	pF

Remarks 1. Pins 9 and 14 (ϕ1), 8 and 15 (ϕ2) are each connected inside of the device.

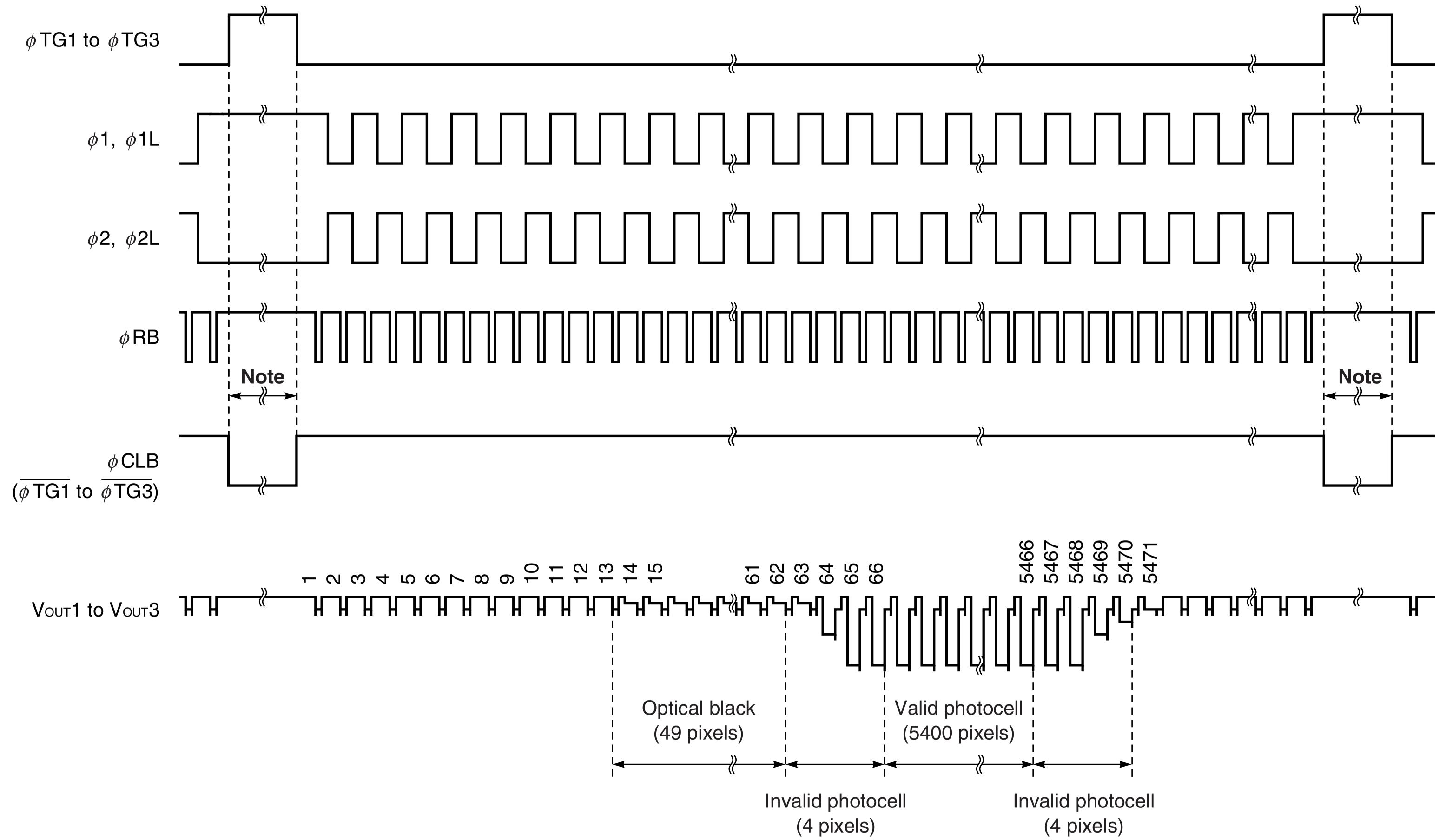
★ **2.** $C_{\phi 1}$ and $C_{\phi 2}$ show the equivalent capacity of the real drive including the capacity of between ϕ1 and ϕ2.

TIMING CHART 1-1 (Bit clamp mode, for each color)



Note Set the φRB and φCLB to high level during this period.

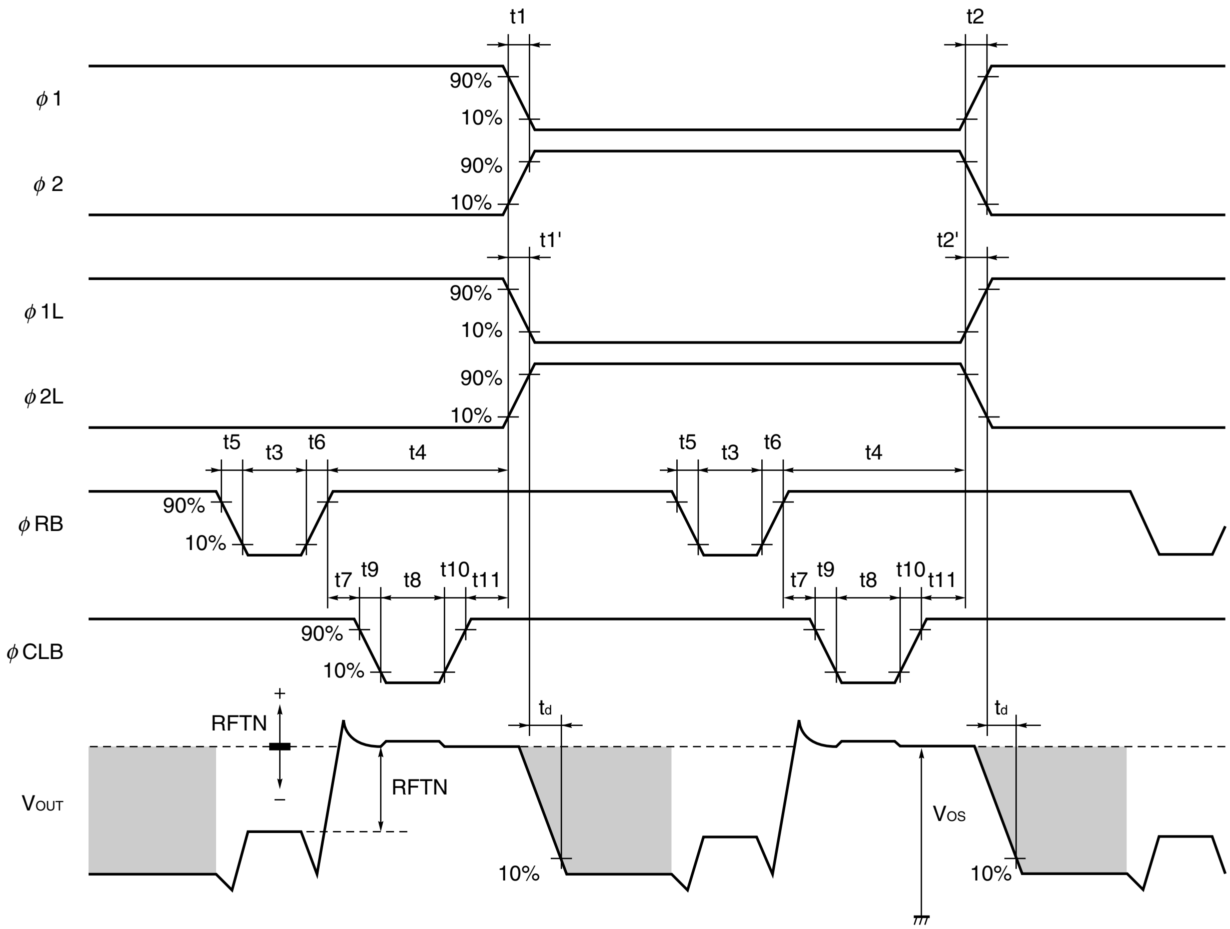
TIMING CHART 1-2 (Line clamp mode, for each color)



Note Set the φRB to high level during this period.

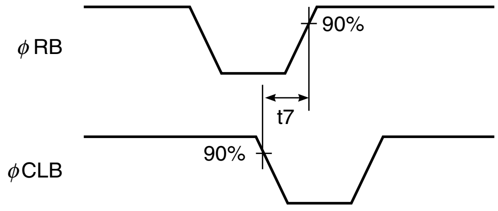
Remark Inverse pulse of the φTG1 to φTG3 can be used as φCLB.

TIMING CHART 2 (Bit clamp mode, for each color)

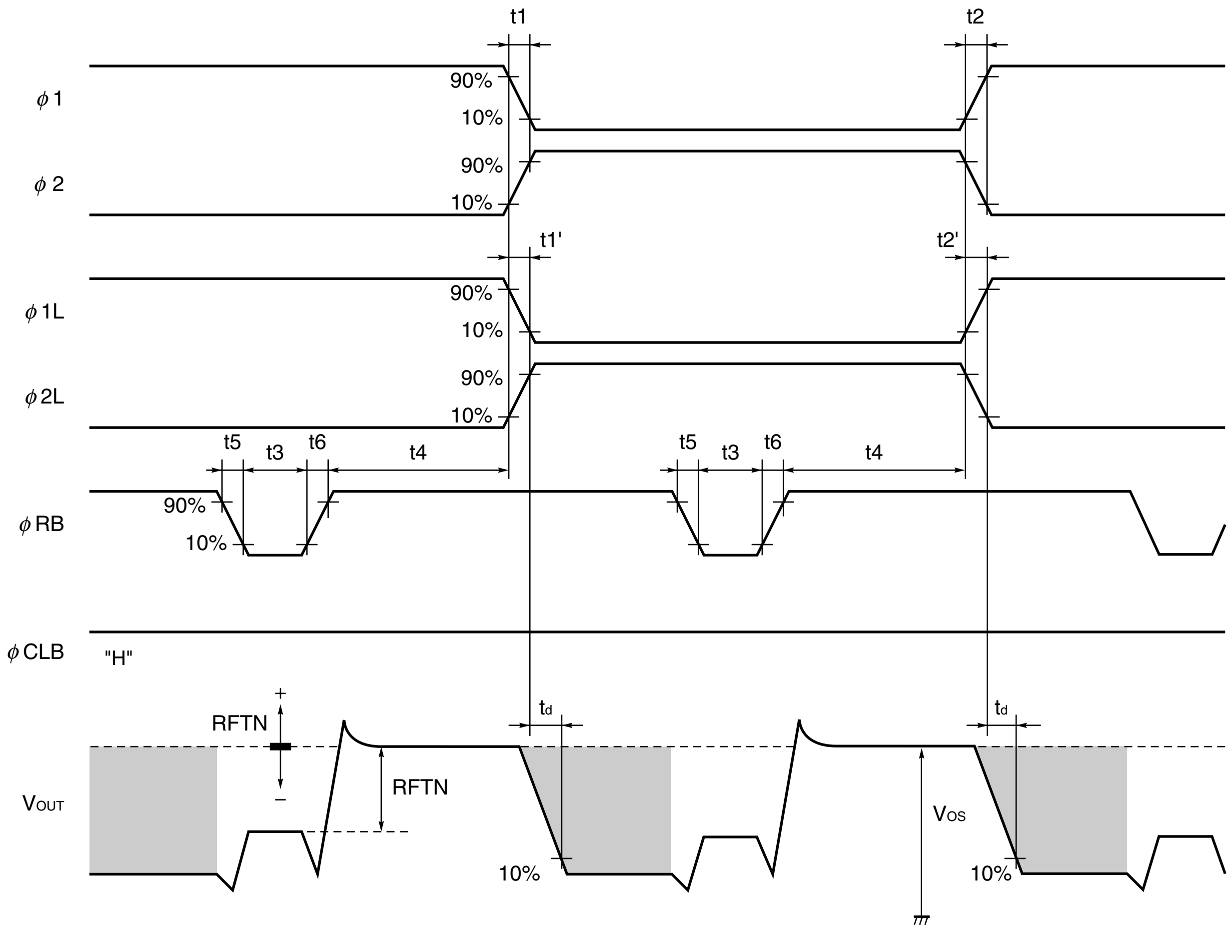


Symbol	Min.	Typ.	Max.	Unit
t1, t2	0	25	–	ns
t1', t2'	0	5	–	ns
t3	20	100	–	ns
t4	30	150	–	ns
t5, t6	0	25	–	ns
t7	–5 Note	25	–	ns
t8	20	100	–	ns
t9, t10	0	25	–	ns
t11	5	25	–	ns

Note Min. of t7 shows that the φRB and φCLB overlap each other.

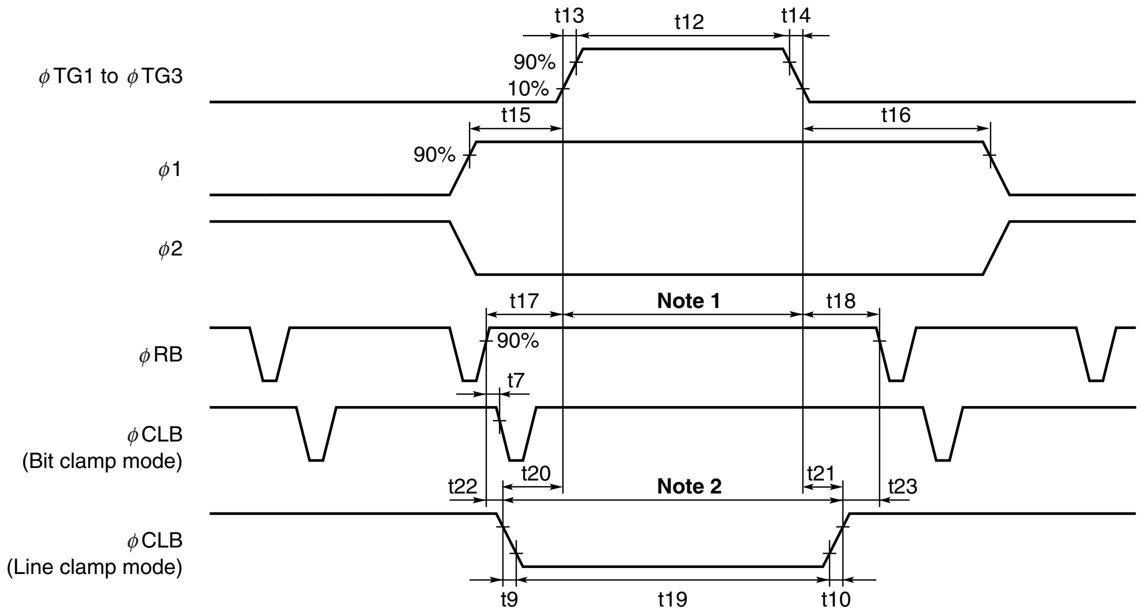


TIMING CHART 3 (Line clamp mode, for each color)



Symbol	Min.	Typ.	Max.	Unit
t1, t2	0	25	–	ns
t1', t2'	0	5	–	ns
t3	20	100	–	ns
t4	30	150	–	ns
t5, t6	0	25	–	ns

φTG1 to φTG3, φ1, φ2 TIMING CHART

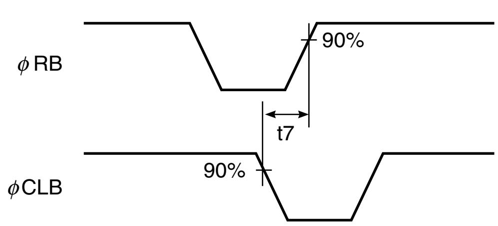


Symbol	Min.	Typ.	Max.	Unit
t7	–5 Note 3	25	–	ns
t9, t10	0	25	–	ns
t12	5000	10000	50000	ns
t13, t14	0	50	–	ns
t15, t16	900	1000	–	ns
t17, t18	200	400	–	ns
t19	t12	t12	50000	ns
t20, t21	0	50	–	ns
t22, t23	0	350	–	ns

Notes 1. Set the φRB and φCLB to high level during this period.

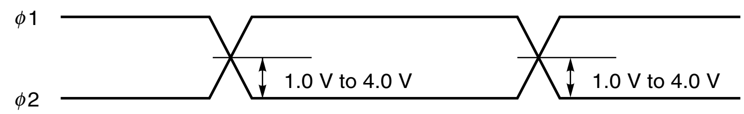
2. Set the φRB to high level during this period.

3. Min. of t7 shows that the φRB and φCLB overlap each other.

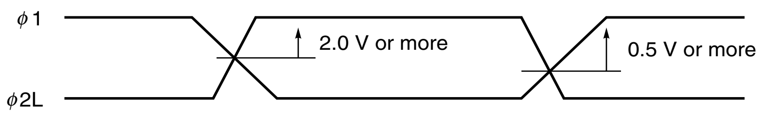


Remark Inverse pulse of the φTG1 to φTG3 can be used as φCLB.

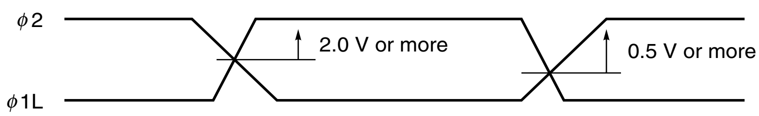
ϕ1, ϕ2 cross points



ϕ1, ϕ2L cross points



ϕ2, ϕ1L cross points



Remark Adjust cross points (ϕ1, ϕ2), (ϕ1, ϕ2L) and (ϕ2, ϕ1L) with input resistance of each pin.

DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage : **V_{sat}**

   Output signal voltage at which the response linearity is lost.

2. Saturation exposure : **SE**

   Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.

3. Photo response non-uniformity : **PRNU**

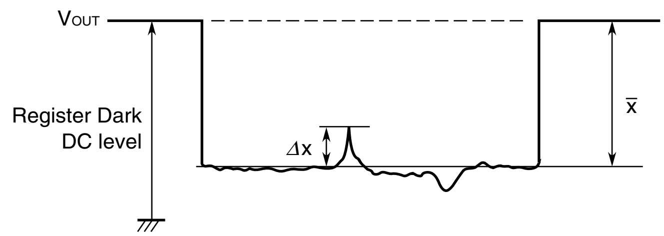
   The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$\text{PRNU (\%)} = \frac{\Delta x}{\overline{x}} \times 100$$

Δx : maximum of $|x_j - \overline{x}|$

$$\overline{x} = \frac{\sum_{j=1}^{5400} x_j}{5400}$$

x_j : Output voltage of valid pixel number j



4. Average dark signal : **ADS**

   Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

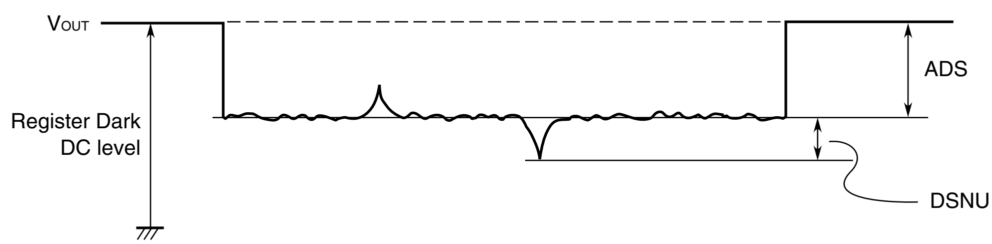
$$\text{ADS (mV)} = \frac{\sum_{j=1}^{5400} d_j}{5400}$$

d_j : Dark signal of valid pixel number j

5. Dark signal non-uniformity : **DSNU**
   Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

   DSNU (mV) : maximum of $|d_j - ADS|_{j = 1 \text{ to } 5400}$

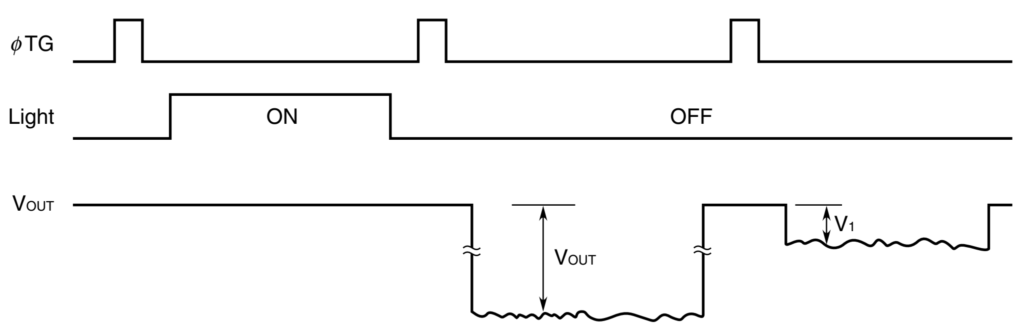
   d_j : Dark signal of valid pixel number j



6. Output impedance : **Zo**
   Impedance of the output pins viewed from outside.

7. Response : **R**
   Output voltage divided by exposure (lx•s).
   Note that the response varies with a light source (spectral characteristic).

8. Image lag : **IL**
   The rate between the last output voltage and the next one after read out the data of a line.



$$IL\ (\%) = \frac{V_1}{V_{OUT}} \times 100$$

9. Register imbalance: **RI**

The rate of the difference between the averages of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels.

$$RI\ (\%) = \frac{\frac{2}{n}\left|\sum_{j=1}^{\frac{n}{2}}(V_{2j-1} - V_{2j})\right|}{\frac{1}{n}\sum_{j=1}^{n}V_j} \times 100$$

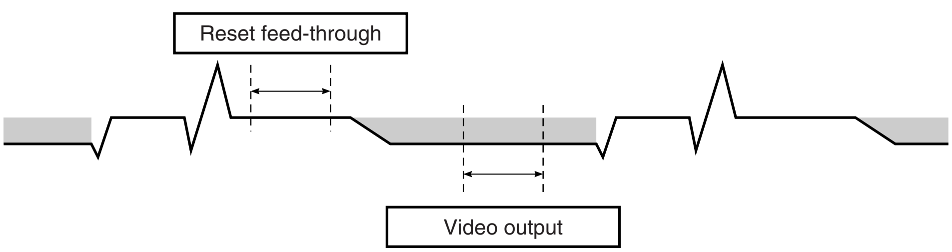
n : Number of valid pixels
V_j : Output voltage of each pixel

10. Random noise (CDS) : **σCDS**

Random noise σCDS is defined as the standard deviation of a valid pixel output signal with 100 times (=100 lines) data sampling at dark (light shielding). σCDS is calculated by the following procedure.

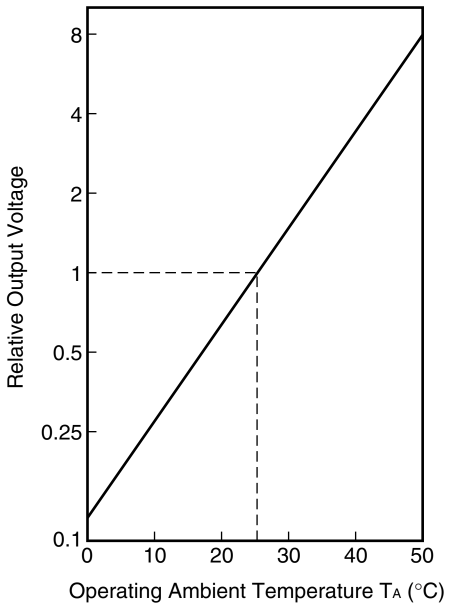
1. One valid photocell in one reading is fixed as measurement point.
2. The output level is measured during the reset feed-through period which is averaged over 100 ns to get "VD_i".
3. The output level is measured during the video output time averaged over 100 ns to get "VO_i".
4. The correlated double sampling output is defined by $VCDS_i = VD_i - VO_i$
5. Repeat the above procedure (1 to 4) for 100 times (= 100 lines).
6. Calculate the standard deviation σCDS using the following equation.

$$\sigma CDS\ (mV) = \sqrt{\frac{\sum_{i=1}^{100}(VCDS_i - \overline{V})^2}{100}}\ ,\quad \overline{V} = \frac{1}{100}\sum_{i=1}^{100} VCDS_i$$

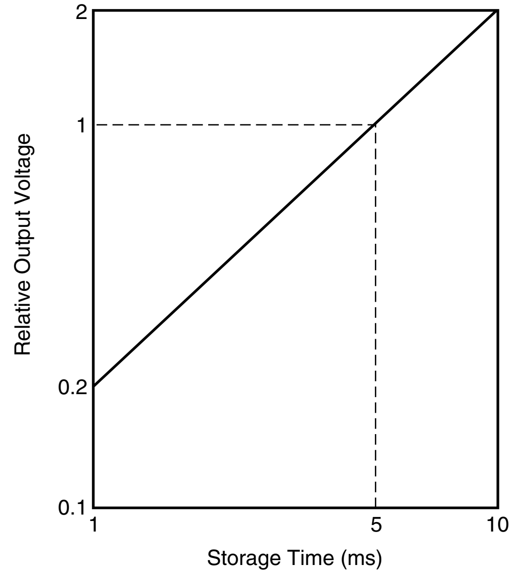


STANDARD CHARACTERISTIC CURVES (Reference Value)

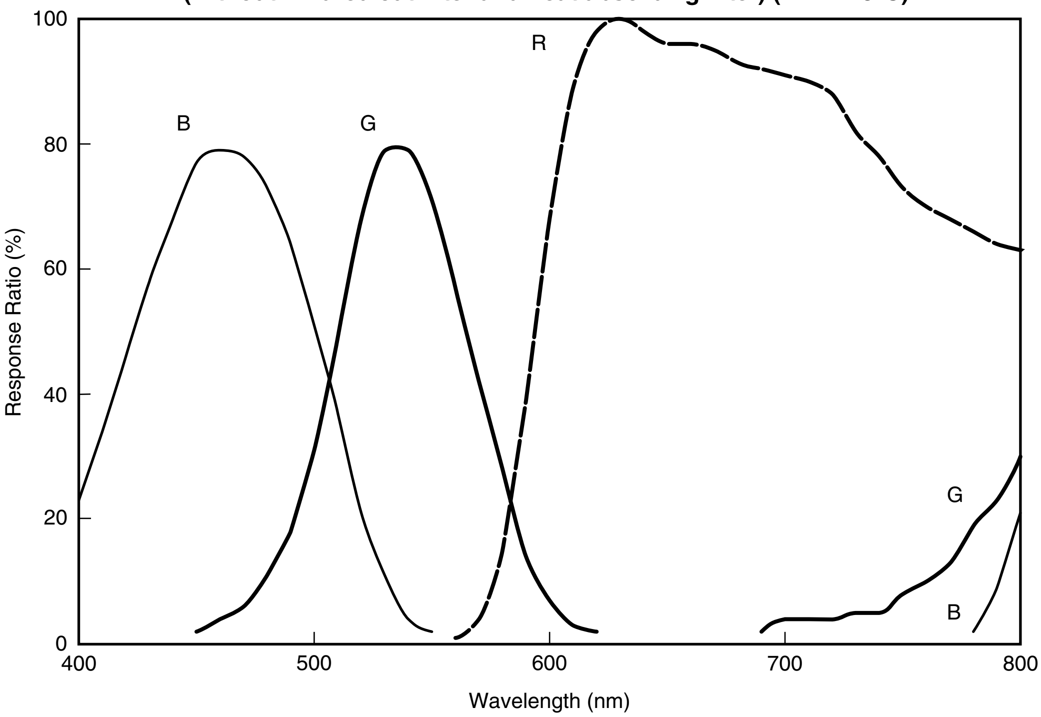
DARK OUTPUT TEMPERATURE CHARACTERISTIC



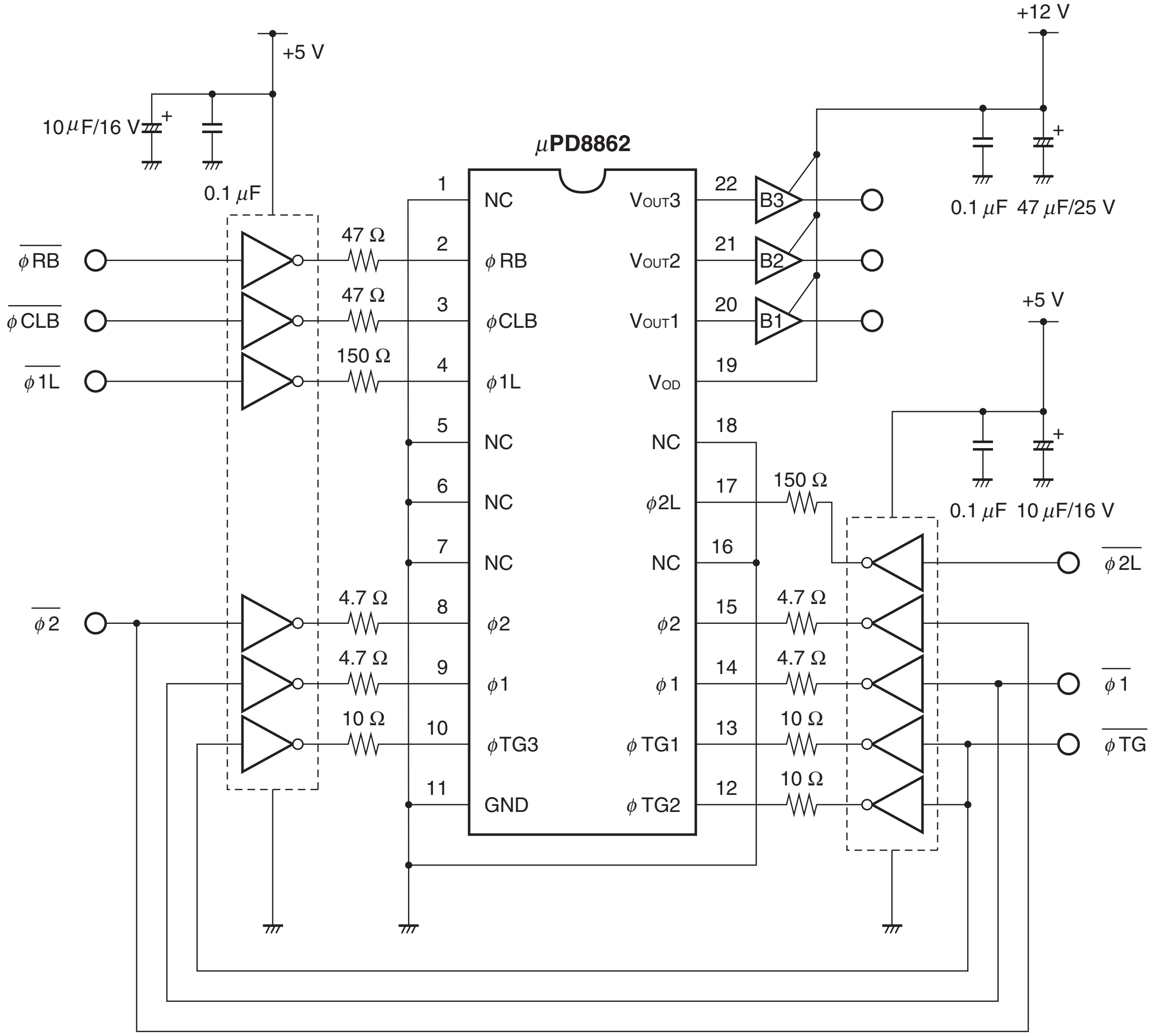
STORAGE TIME OUTPUT VOLTAGE CHARACTERISTIC (TA = +25°C)



TOTAL SPECTRAL RESPONSE CHARACTERISTICS (without infrared cut filter and heat absorbing filter) (TA = +25°C)



APPLICATION CIRCUIT EXAMPLE

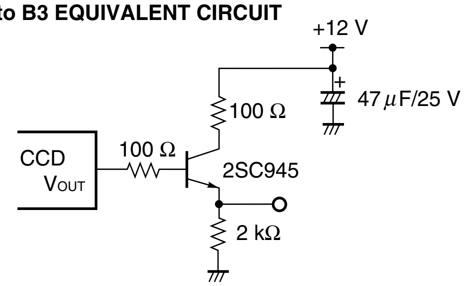


Caution Connect the No connection pins (NC) to GND.

Remarks 1. The inverters shown in the above application circuit example are the 74HC04 (data rate < 2 MHz) or the 74AC04 (2 ≤ data rate < 6 MHz).

2. Inverters B1 to B3 in the above application circuit example are shown in the figure below.

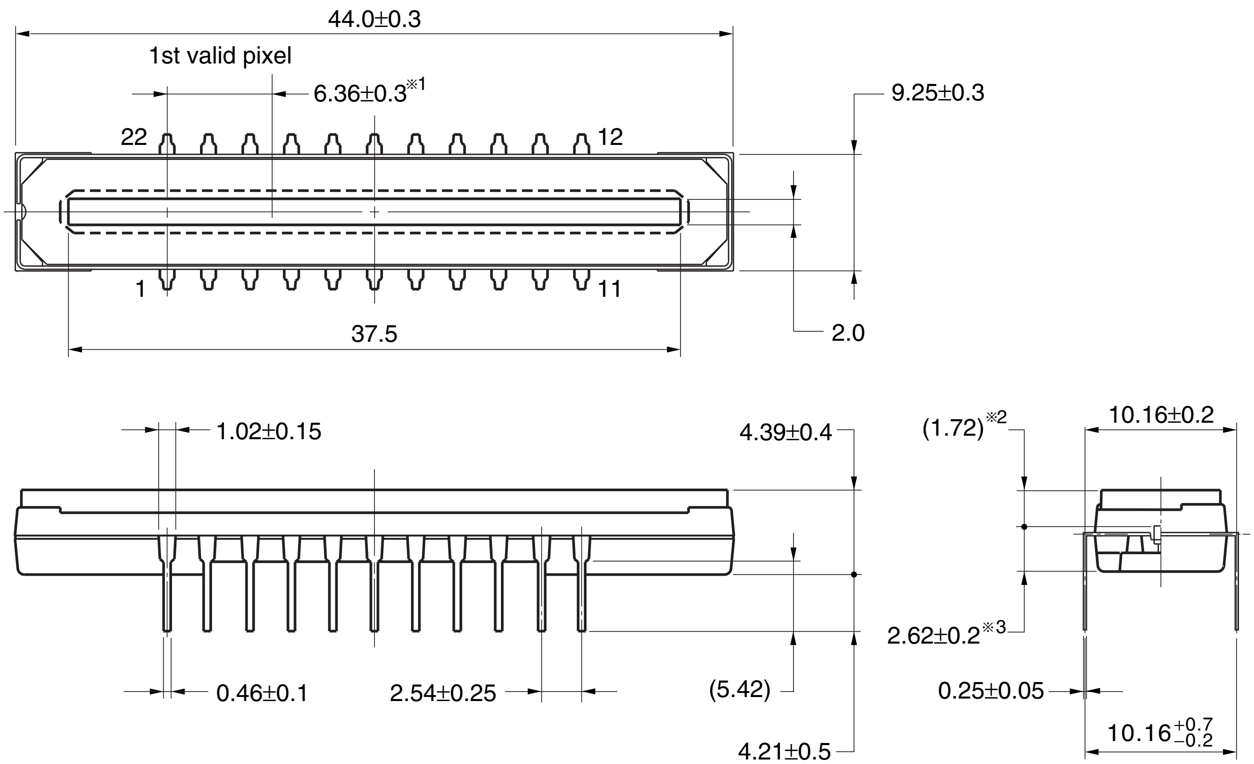
B1 to B3 EQUIVALENT CIRCUIT



★ **PACKAGE DRAWING**

μPD8862CY
CCD LINEAR IMAGE SENSOR 22-PIN PLASTIC DIP (10.16 mm (400))

(Unit : mm)



Name	Dimensions	Refractive index
Plastic cap	42.9×8.35×0.7	1.5

※1 1st valid pixel ←→ The center of the pin1
※2 The surface of the CCD chip ←→ The top of the cap
※3 The bottom of the package ←→ The surface of the CCD chip

22C-1CCD-PKG12-2

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

Type of Through-hole Device

μPD8862CY : CCD linear image sensor 22-pin plastic DIP (10.16 mm (400))

Process	Conditions
Partial heating method	Pin temperature : 300 °C or below, Heat time : 3 seconds or less (per pin)

Cautions 1. During assembly care should be taken to prevent solder or flux from contacting the plastic cap. The optical characteristics could be degraded by such contact.

2. Soldering by the solder flow method may have deleterious effects on prevention of plastic cap soiling and heat resistance. So the method cannot be guaranteed.

NOTES ON HANDLING THE PACKAGES

① DUST AND DIRT PROTECTING

The optical characteristics of the CCD will be degraded if the cap is scratched during cleaning. Don’t either touch plastic cap surface by hand or have any object come in contact with plastic cap surface. Should dirt stick to a plastic cap surface, blow it off with an air blower. For dirt stuck through electricity ionized air is recommended. And if the plastic cap surface is grease stained, clean with our recommended solvents.

○ CLEANING THE PLASTIC CAP

Care should be taken when cleaning the surface to prevent scratches.

We recommend cleaning the cap with a soft cloth moistened with one of the recommended solvents below. Excessive pressure should not be applied to the cap during cleaning. If the cap requires multiple cleanings it is recommended that a clean surface or cloth be used.

○ RECOMMENDED SOLVENTS

The following are the recommended solvents for cleaning the CCD plastic cap.

Use of solvents other than these could result in optical or physical degradation in the plastic cap. Please consult your sales office when considering an alternative solvent.

Solvents	Symbol
Ethyl Alcohol	EtOH
Methyl Alcohol	MeOH
Isopropyl Alcohol	IPA
N-methyl Pyrrolidone	NMP

② MOUNTING OF THE PACKAGE

The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board. Don't have any object come in contact with plastic cap. You should not reform the lead frame. We recommended to use a IC-inserter when you assemble to PCB.

Also, be care that the any of the following can cause the package to crack or dust to be generated.

1. Applying heat to the external leads for an extended period of time with soldering iron.
2. Applying repetitive bending stress to the external leads.
3. Rapid cooling or heating

③ OPERATE AND STORAGE ENVIRONMENTS

Operate in clean environments. CCD image sensors are precise optical equipment that should not be subject to mechanical shocks. Exposure to high temperatures or humidity will affect the characteristics. So avoid storage or usage in such conditions.

Keep in a case to protect from dust and dirt. Dew condensation may occur on CCD image sensors when the devices are transported from a low-temperature environment to a high-temperature environment. Avoid such rapid temperature changes.

For more details, refer to our document "Review of Quality and Reliability Handbook" (C12769E)

④ ELECTROSTATIC BREAKDOWN

CCD image sensor is protected against static electricity, but destruction due to static electricity is sometimes detected. Before handling be sure to take the following protective measures.

1. Ground the tools such as soldering iron, radio cutting pliers of or pincer.
2. Install a conductive mat or on the floor or working table to prevent the generation of static electricity.
3. Either handle bare handed or use non-chargeable gloves, clothes or material.
4. Ionized air is recommended for discharge when handling CCD image sensor.
5. For the shipment of mounted substrates, use box treated for prevention of static charges.
6. Anyone who is handling CCD image sensors, mounting them on PCBs or testing or inspecting PCBs on which CCD image sensors have been mounted must wear anti-static bands such as wrist straps and ankle straps which are grounded via a series resistance connection of about 1 MΩ.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.