APOGEE TECHNOLOGY, INC.

DDX-2100

All-Digital High Efficiency Power Amplifier

FEATURES

- HIGH OUTPUT CAPABILITY
- **2 x 50W** into 8Ω or **1 x 100W** into 4Ω
- SINGLE SUPPLY (+9V to +36V)
- SMALL PACKAGE
- HIGH EFFICIENCY, >88%
- THERMAL OVERLOAD AND SHORT CIRCUIT PROTECTION

BENEFITS

- COMPLETE SURFACE MOUNT DESIGN
- POWER SUPPLY SAVINGS

APPLICATIONS

- DIGITAL POWERED SPEAKERS
- PC SOUND CARDS
- CAR AUDIO
- SURROUND SOUND SYSTEMS
- DIGITAL AUDIO COMPONENTS

GENERAL DESCRIPTION

The DDX-2100 power device is a monolithic dual channel H-Bridge that can provide up to 50 watts per channel of audio power at very high efficiency. The DDX-2100 power device contains a logic interface, integrated bridge drivers, high efficiency MOSFET output transistors and protection circuitry. The device may be used as a dual bridge or reconfigured as a single bridge with double the output current capability.

The benefits of the DDX amplification system are an all-digital design that eliminates the need for a digital to analog converter (DAC) and the high efficiency operation derived from the use of Apogee's patented damped ternary pulse width modulation (PWM). This approach provides an efficiency advantage over conventional Class-D designs and up to three times the efficiency of typical Class A/B amplifiers with music input signals.

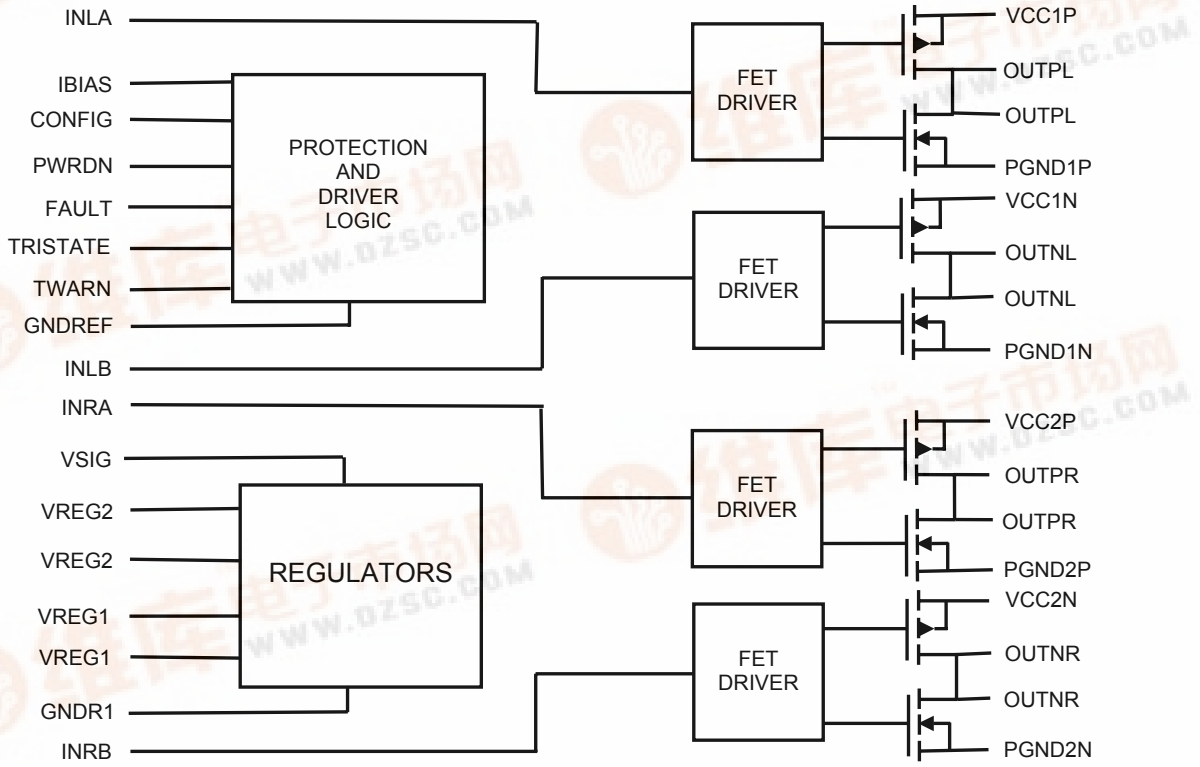


Figure 1. Block Diagram

Absolute Maximum Ratings [Note 1]

SYMBOL	PARAMETER	VALUE	UNIT
VCC	Power supply voltage	40V	V
VL	Input logic reference	5.5V	V
Tj	Operating junction temperature range	-40 to +150	°C
Tstg	Storage temperature range	-40 to +150	°C

Recommended Operating Conditions [Note 2]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VCC	Power supply voltage	10.0		36.0	V
VL	Input logic reference	2.7	3.3	5.0	V
T_A	Ambient Temperature	0		70	°C

Thermal Data

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
θ_{JC}	Thermal resistance junction-case (thermal pad)			2.5	°C/W
T_{jSD}	Thermal shut-down junction temperature		150		°C
Twarn	Thermal warning temperature		130		°C
T_{hSD}	Thermal shut-down hysteresis		25		°C

Electrical Characteristics

Refer to circuit Figure 2. VCC = 36V, V_L = 3.3V, fsw = 384kHz, T_A = 25C, RL = 8Ω unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Po	Output power [Note 3]	THD+N <1%		50		Wrms
Po	Output power [Note 3]	THD+N <10%		75		Wrms
UVL	Undervoltage Lockout Threshold			7	9	V
I_{PD}	Vcc supply current in Powerdown			1	3	mA
I_{cc}tri	Supply current from Vcc in Tristate	TRISTATE = 0		25		mA
I_{cc}	Vcc supply current	2-Chan. switching at 384 KHz.		75		mA
I_{sc}	Output Short-circuit Protection limit	Speaker outputs.	3.5	5.0	6.5	A
THD+N	Total Harmonic Distortion+Noise [Note 3]	Po=1 Wrms Po=50 Wrms		.07 .50		% %
SNR	Signal to Noise Ratio [Note 3]	A-Weighted		90		dB
η	Efficiency	Po=2 x 50 W		88		%
RdsON	Power MOSFET output resistance	Id=1A		200	270	mΩ
RdsON matching		Id=1A	95			%
t_{on}	Turn-on delay time	Resistive load			100	ns
t_{off}	Turn-off delay time	Resistive load			100	ns
t_r	Rise time	Resistive load			25	ns
t_f	Fall Time	Resistive load			25	ns
V_{IL}	Low logic input voltage on PWRDN, TRISTATE pins	V_L = 2.7V V_L = 3.3V V_L = 5.0V	0.7 0.8 0.85			V
V_{IH}	High logic input voltage on PWRDN, TRISTATE pins	V_L = 2.7V V_L = 3.3V V_L = 5.0V			1.5 1.7 1.85	V
V_{IL}, PWM Inputs	Low logic input voltage on INLA, INLB, INRA, INRB pins	V_L = 2.7V V_L = 3.3V V_L = 5.0V	1.05 1.35 2.2			V
V_{IH}, PWM Inputs	High logic input voltage on INLA, INLB, INRA, INRB pins	V_L = 2.7V V_L = 3.3V V_L = 5.0V			1.65 1.95 2.8	V
I_{fault}	Output Sink Current, FAULT, TWARN pins	Fault Active		1		mA
$P_w$min	Minimum output pulse width	No load	70		150	ns

Electrical Characteristics (continued)

Note 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Note 2: Performance not guaranteed beyond recommended operating conditions.
Note 3: Characteristics are for the DDX-2100 power device driven by DDX-2000 processor.

Logic Truth Table

TRISTATE	INxA	INxB	OUTPx	OUTNx	OUTPUT MODE
0	X	X	OFF	OFF	Hi-Z
1	0	0	GND	GND	DAMPED
1	0	1	GND	VCC	NEGATIVE
1	1	0	VCC	GND	POSITIVE
1	1	1	VCC	VCC	Not Used

DDX-2100 Pin Function Description

PWM Inputs

Pin Name	Pin No.	Description
INLA	29	Left A logic input signal
INLB	30	Left B logic input signal
INRA	31	Right A logic input signal
INRB	32	Right B logic input signal

Control/Miscellaneous

Pin Name	Pin No.	Description
PWRDN	25	Power Down (0=Shutdown, 1= Normal).
TRI-STATE	26	Tri-State (0=All MOSFETS Hi-Z, 1=Normal).
FAULT [Note 4]	27	Fault output indicator; Overcurrent Overtemperature (0=Fault, 1=Normal).
TWARN [Note 4]	28	Thermal warning output (0=Warning T_J >= 130°C, 1=Normal).
CONFIG [Note 5]	24	Configuration (0=Normal, 1=Parallel operation for mono).
NC	18	Do not connect.

Power Outputs [Note 6]

Pin Name	Pin No.	Description
OUTPL	16, 17	Left output, positive reference
OUTNL	10, 11	Left output, negative reference
OUTPR	8, 9	Right output, positive reference
OUTNR	2, 3	Right output, negative reference

Note 4: FAULT and TWARN outputs are open-drain
Note 5: Connect CONFIG Pin 24 to VREG1 Pins 21,22 to implement single bridge operation for high current.
Note 6: DDX outputs are bridged. The outputs OUTPx produce signals in phase with the input.

Power Supplies

Pin Name	Pin No.	Description
VCC [1P, 1N, 2P, 2N]	4, 7, 12, 15	Power
PGND [1P, 1N, 2P, 2N]	5, 6, 13, 14	Power grounds
VREG1	21, 22	Internal regulator voltage requires bypass capacitor.
VREG2	33, 34	Internal regulator voltage requires bypass capacitor.
VSIG	35, 36	Signal Positive supply.
VL	23	Logic reference voltage.
GNDREF	19	Logic reference ground.
GNDS	1	Substrate ground.
GNDR1	20	Internal regulator ground.

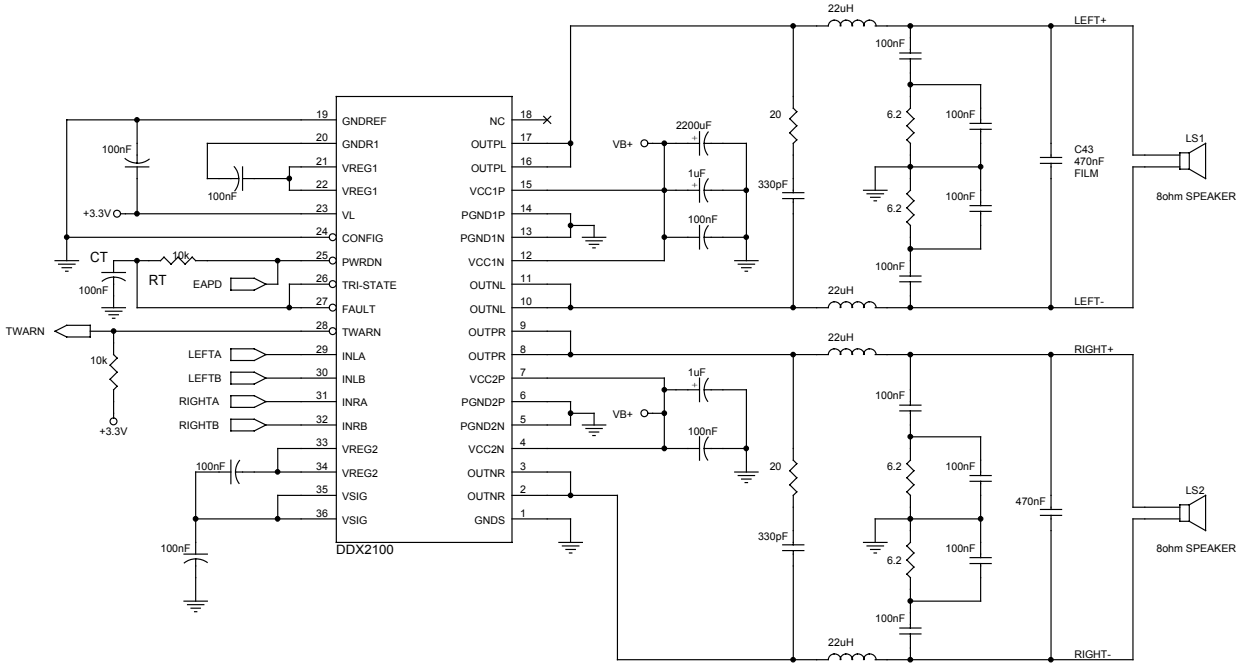


Figure 2. Stereo Audio Application Circuit

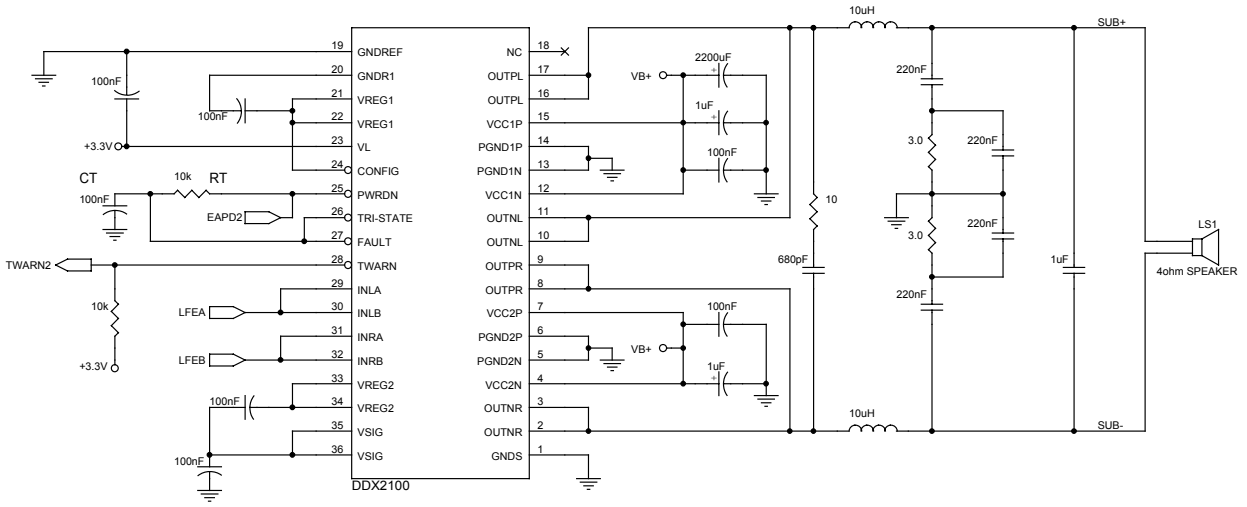


Figure 3. Mono Audio Application Circuit

DDX-2100 POWER DEVICE

The DDX-2100 Power Device is a dual channel H-Bridge that can deliver over 50 watts per channel of audio output power at very high efficiency. It converts DDX controlled PWM signals to power at the load. The DDX-2100 includes a logic interface, integrated bridge drivers, high efficiency MOSFET outputs, thermal and short circuit protection circuitry. Two logic level signals per channel are used to control high-speed MOSFET switches to connect the speaker load to the input supply or to ground in a bridge configuration, according to Apogee's patented damped ternary PWM. The DDX-2100 includes over-current, thermal and under-voltage lockout with automatic recovery. A thermal warning status is also provided.

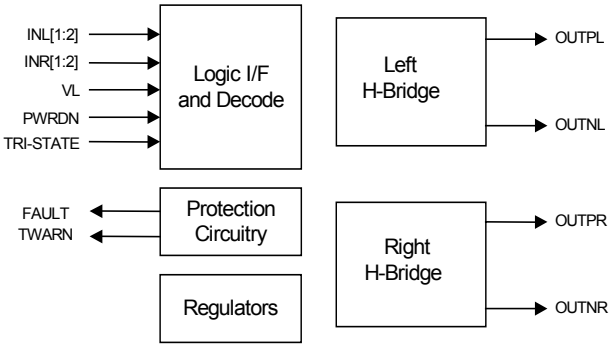


Figure 4. DDX-2100 Block Diagram

Logic Interface and Decode

The DDX-2100 power outputs are controlled using two logic level timing signals. In order to provide a proper logic interface, the VL input must operate at the same voltage as the DDX controller logic supply.

Protection Circuitry

The DDX-2100 includes protection circuitry for over-current and thermal overload conditions. A thermal warning pin TWARN is activated low (open-drain MOSFET) when the IC temperature exceeds 130°C, in advance of the thermal shutdown protection. When a fault condition is detected (logical OR of over-current and thermal), an internal fault signal acts to immediately disable the output power MOSFETs, placing both H-bridges in a high impedance state. At the same time an open-drain MOSFET connected to the FAULT pin is switched on. There are two possible modes subsequent to activating a fault. The first is a SHUTDOWN mode. With FAULT (pull-up resistor) and TRI-STATE pins independent, an activated fault will disable the device, signaling low at the FAULT output. The device may subsequently be reset to normal operation by toggling the TRI-STATE pin from High to Low to High using an external logic signal. The second is an AUTOMATIC recovery mode. This is depicted in the application circuit, Figure 2. The FAULT and TRI-STATE pins are shorted together and connected to a time constant circuit comprising RT and CT. An activated FAULT will force a reset on the TRI-STATE pin causing normal operation to resume following a delay determined by the time constant of the circuit. If the fault condition is still presented, the circuit operation will continue repeating until such time as the fault condition is removed. An increase in the time constant of the circuit will produce a longer recovery interval. Care must be taken in the overall system design so as not to exceed the protection thresholds under normal operation.

Power Outputs

The DDX-2100 power and output pins are duplicated to provide a low impedance path for the devices bridged outputs. All duplicate power, ground and output pins must be connected for proper operation. The PWRDN or TRI-STATE pins should be used to set all MOSFETS to the Hi-Z state during power-up until the logic power supply, VL, is settled.

Parallel Output/High Current Operation

The DDX-2100 outputs can be connected in parallel to increase the output current to a load. In this configuration the device can provide over 100W into 4Ω (see Figure 3). This mode is enabled with the CONFIG pin connected to VREG1 and the inputs combined INLA = INLB, INRA = INRB and outputs combined OUTLA = OUTLB, OUTRA = OUTRB.

ADDITIONAL INFORMATION

Output Filter

A passive two-pole low pass filter is used on the DDX-2100 power outputs to reconstruct an analog signal. System performance can be significantly affected by the output filter design and choice of components. A filter design for 8Ω loads is shown in Figure 2, and for 4Ω loads in Figure 3.

Power Dissipation/Heat Sink Requirements

The power dissipation of the device will depend primarily on the supply voltage, load impedance, and output modulation level.

The DDX-2100 surface mount package includes an exposed thermal pad on the top of the device to provide a direct thermal path from the integrated circuit to the heatsink. This pad should be fastened to a low thermal impedance path at circuit ground potential for proper operation.. For continuous duty rated applications, careful consideration must be made to the overall thermal design.

For additional thermal design considerations, see http://www.apogeeddx.com/DDX_Themal_Considerations.PDF

Typical Performance Characteristics at Vcc=36V

Figure 5: Efficiency

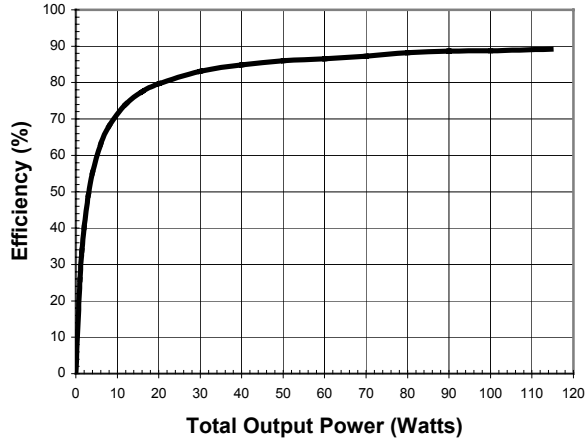
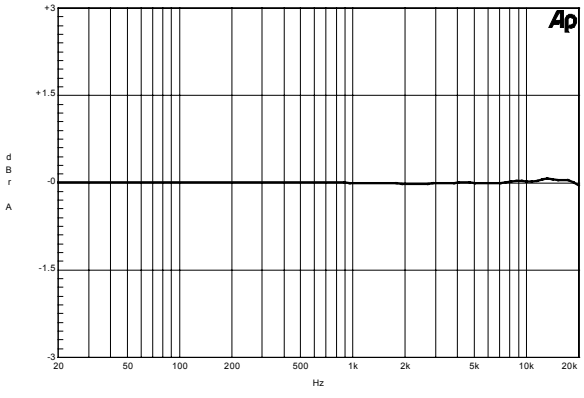


Figure 6: Frequency Response



Typical Performance Characteristics at Vcc=36V, 8Ω Load, Stereo Mode

Figure 7: THD+N vs. Frequency

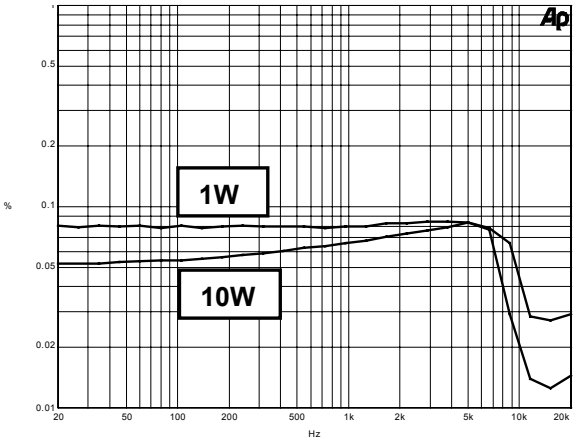
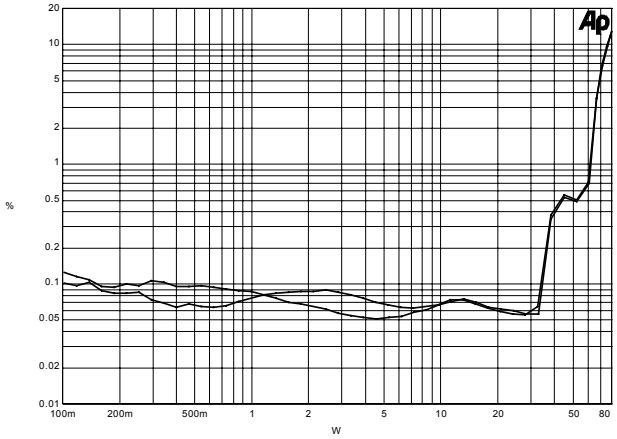


Figure 8: THD+N vs. Output Power @ 1kHz



Typical Performance Characteristics at Vcc=36V, 4Ω Load, Mono Mode

Figure 9: THD+N vs. Frequency

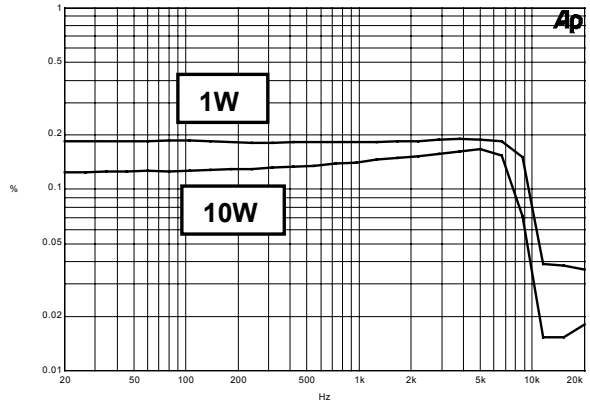
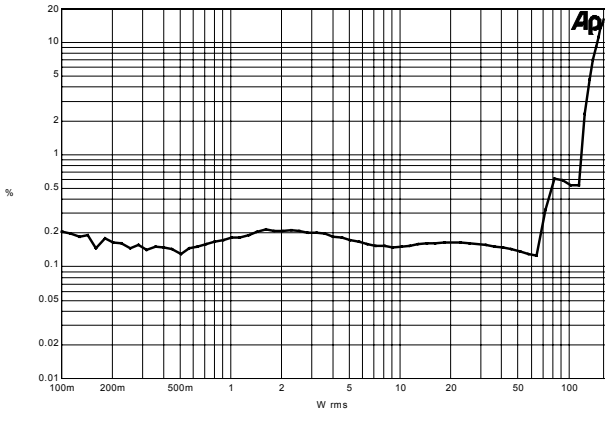


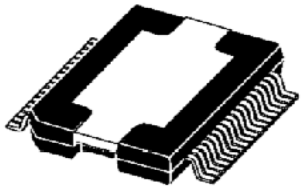
Figure 10: THD+N vs. Output Power @ 1kHz



PHYSICAL DIMENSIONS (Dimensions shown in mm)

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.25		3.5	0.128		0.138
A2		3.15			0.124	
A4	0.8		1	0.031		0.039
A5		0.2			0.008	
a1	0		0.1	0		0.004
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D	15.8		16	0.622		0.630
D1	9.4		9.8	0.37		0.38
D2		1			0.039	
E	13.9		14.5	0.547		0.57
E1	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
E4	2.9		3.2	0.114		1.259
e		0.65			0.026	
e3		11.05			0.435	
G	0		0.1	0		0.004
H	15.5		15.9	0.61		0.625
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	10° (max)					
s	8° (max)					

OUTLINE AND MECHANICAL DATA



PowerSO-36 (SLUG UP)