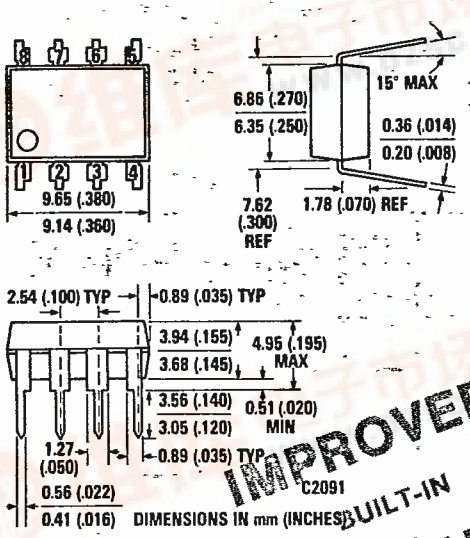
GENERAL INSTRUMENT

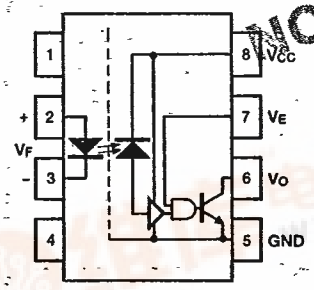
VERY HIGH-SPEED LOGIC GATE OPTOCOUPLERS

6N137
10 MBit/s LOGIC GATE MCL2601 (HCPL-2601)

PACKAGE DIMENSIONS



IMPROVED!
BUILT-IN
NOISE SHIELD



Equivalent Circuit

TRUTH TABLE
(Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H

A 0.1μF bypass capacitor must be connected between pins 8 and 5. (See note 1)

DESCRIPTION

The 6N137 and MCL/HCPL-2601 single-channel optocouplers consists of a 700 nm GaAsP LED, optically coupled to a very high speed integrated photodetector logic gate with a strobable output. This output features an open collector, thereby permitting wired-OR outputs. The coupled parameters are guaranteed over the temperature range of 0-70° C. A maximum input signal of 5 mA will provide a minimum output sink current of 13 mA (fan-out of 8).

An internal noise shield provides superior common mode rejection of typically 10 kV/μs. The MCL/HCPL-2601 has a minimum CMR of 1 kV/μs.

An improved package allows superior insulation, permitting a 480 V working voltage compared to industry standard 220 V.

FEATURES

- Very high speed — 10 MBit/s
- Superior CMR — 10 k V/μs
- Superior insulation — 2500 V RMS 1 min.
- Double working voltage — 480 V
- Fan-out of 8 over 0-70° C
- Logic gate output
- Strobable output
- Wired-OR — open collector
- U.L. recognized (File #E50151)

APPLICATIONS

- Ground loop elimination
- LSTTL to TTL, LSTTL or 5-volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer-peripheral interface

ABSOLUTE MAXIMUM RATING

Storage temperature ..... -55° C to + 125° C
Operating temperature ..... 0° C to + 70° C
Lead solder temperature ..... 260° C for 10 s
DC/average forward input current ..... 20 mA
Enable input voltage, (V_E)
(Not to exceed V_{CC} by more than 500 mV) ... 5.5 V
Reverse input voltage ..... 5.0 V
Reverse supply voltage ($-V_{CC}$) ..... -500 mV
Supply voltage, (V_{CC}) .... 7.0 V/1 minute maximum
Output current, (I_O) ..... 25 mA
Output voltage , (V_O) ..... 7.0 V
Collector output power dissipation ..... 40 mW

RECOMMENDED OPERATING CONDITIONS

	SYMBOL	MIN.	MAX.	UNITS
Input current, low level	I_{FL}	0	250	μA
Input current, high level	I_{FH}	*6.3	15	mA
Supply voltage, output	V_{CC}	4.5	5.5	V
Enable voltage low level	V_{EL}	0	0.8	V
Enable voltage high level	V_{EH}	2.0	V_{CC}	V
Operating temperature	T_A	0	70	°C
Fan out (TTL load)	N		8	

**6.3 mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0 mA or less.*

ELECTRICAL CHARACTERISTICS (T_A = 0° C to 70° C Unless Otherwise Specified)

			6N137			MCL(HCPL)-2601			
PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.**	MAX.	MIN.	TYP.*	MAX.	UNITS
High level output current	I_{OH}	V_{CC} = 5.5 V, V_O = 5.5 V I_F = 250 μA, V_E = 2.0 V		.02	250*		.02	250	μA
Low level output voltage	V_{OL}	V_{CC} = 5.5 V, I_F = 5 mA V_E = 2.0 V, I_{OL} = 13 mA		.34	0.6*		.34	0.6	V
High level supply current	I_{CCH}	V_{CC} = 5.5 V, I_F = 0 mA V_E = 0.5 V		10	15*		10	15	mA
Low level supply current	I_{CCL}	V_{CC} = 5.5 V, I_F = 10 mA V_E = 0.5 V		15	18*		15	18	mA
Low level enable current	I_{EL}	V_{CC} = 5.5 V, V_E = 0.5 V		-1.5	-2.0*		-1.5	-2.0	mA
High level enable current	I_{EH}	V_{CC} = 5.5 V, V_E = 2.0 V		-1.0			-1.0		mA
High level enable voltage	V_{EH}	V_{CC} = 5.5 V, I_F = 10 mA	2.0			2.0			V
Low level enable voltage	V_{EL}	Note: 11			0.8			0.8	V
Input forward voltage	V_F	I_F = 10 mA, T_A = 25° C		1.55	1.75*		1.55	1.75	V
Input reverse breakdown voltage	B_{VR}	I_R = 10 μA, T_A = 25° C	5.0*			5.0			V
Input capacitance	C_{IN}	V_F = 0, f= 1 MHz		60			60		pF
Input diode temperature coefficient	$\Delta V_F/\Delta T_A$	I_F = 10 mA		-1.4			-1.4		mV/°C
Input-output Insulation leakage current	I_{I-O}	Relative humidity = 45% T_A = 25° C, t = 5 s V_{I-O} = 3000 VDC Note: 10			1.0*			1.0	μA
Withstand insulation test voltage	V_{ISO}	RH < 50 % T_A = 25° C t = 1 min.	2500			2500			V_{RMS}
Resistance (Input to output)	R_{I-O}	V_{I-O} = 500 V, Note: 10		10^{12}			10^{12}		Ω
Capacitance (Input to output)	C_{I-O}	f = 1 MHz, Note: 10		0.6			0.6		pF

SWITCHING CHARACTERISTICS (T_A = 25° C, V_{CC} = 5.0 V)

PARAMETER	SYM.	TEST CONDITIONS	6N137 MIN.	6N137 TYP.**	6N137 MAX.	MCL(HCPL)-2601 MIN.	MCL(HCPL)-2601 TYP.*	MCL(HCPL)-2601 MAX.	UNITS
Propagation delay time (For output high level)	T_{PLH}			48	75*		48	75	ns
Propagation delay time (For output low level)	T_{PHL}	R_L = 350 Ω C_L = 15 pF		48	75*		48	75	ns
Output rise time (10-90%)	t_r	I_F = 7.5 mA		30			30		ns
Output fall time (90-10%)	t_f	Notes 2, 3, 4 & 5, Figure 10		14			14		ns
Enable propagation delay time (For output high level)	t_{ELH}	I_F = 7.5 mA V_{EH} = 3.0 V V_{EL} = 0 V		25			25		ns
Enable propagation delay time (For output low level)	t_{EHL}	R_L = 350 Ω, C_L = 15 pf Notes 6 & 7, Figure 11		14			14		ns
Common mode transient immunity (At output high level)	CM_H	V_{CM} = 50 V (Peak) I_F = 0 mA, V_{OH} (Min.) = 2.0 V R_L = 350 Ω, Note 9 Figure 16, 15		10,000		1000	10,000		V/μs
Common mode transient immunity (At output low level)	CM_L	V_{CM} = 50 V (Peak) I_f = 7.5 mA, V_{OL} (Max.) = 0.8 V R_L = 350 Ω Note 8, Figure 16, 15		-10,000		-1000	-10,000		V/μs

JEDEC Registered Data

***All typical values are at V_{CC} = 5 V, T_A = 25° C.*

TYPICAL CHARACTERISTIC CURVES (T_A = 25° C Unless Otherwise Specified)

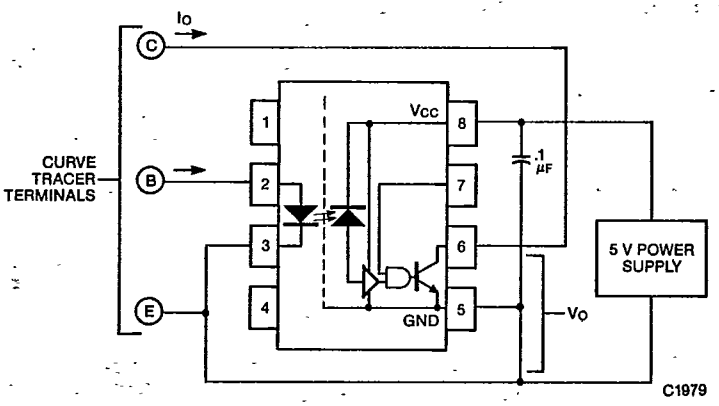


Fig. 1. Curve Tracer Connection to Obtain Collector Characteristics

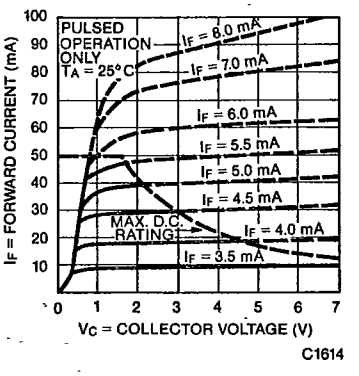


Fig. 2. Optocoupler Collector Characteristics

TYPICAL CHARACTERISTIC CURVES (T_A = 25°C Unless Otherwise Specified)

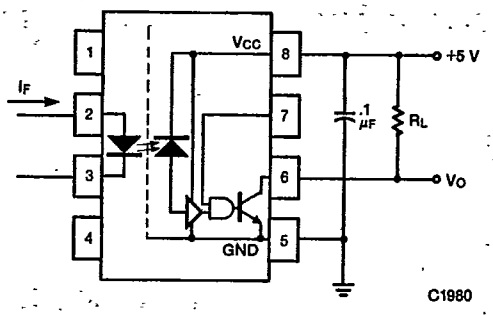


Fig. 3. Input-Output Schematic

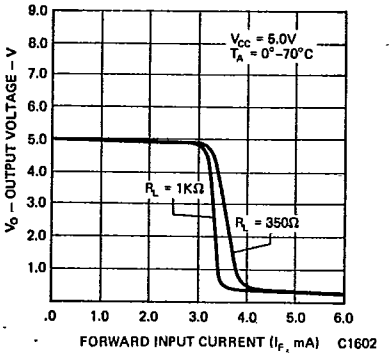


Fig. 4. Output Voltage vs. Forward Input Current

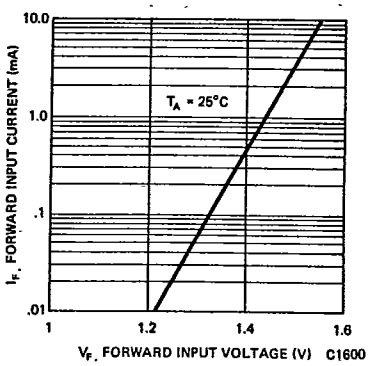


Fig. 5. Forward Input Current vs. Forward Input Voltage

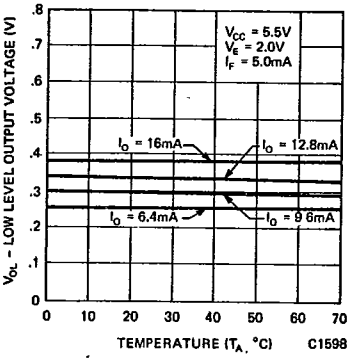


Fig. 6. Low Level Output Voltage vs. Temperature

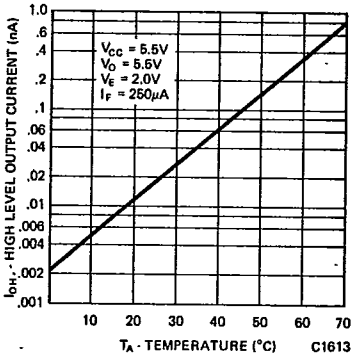


Fig. 7. High Level Output Current vs. Temperature

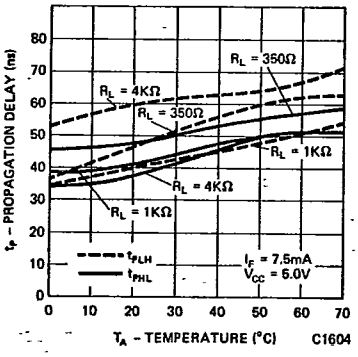


Fig. 8. Propagation Delay vs. Temperature

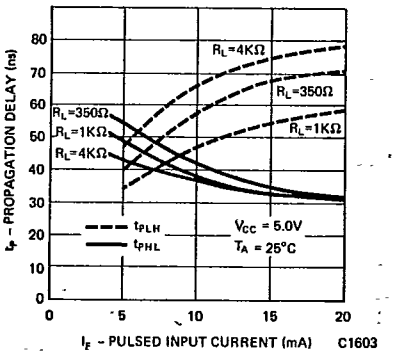


Fig. 9. Propagation Delay vs. Pulse Input Current

TYPICAL CHARACTERISTIC CURVES (T_A = 25° C Unless Otherwise Specified)

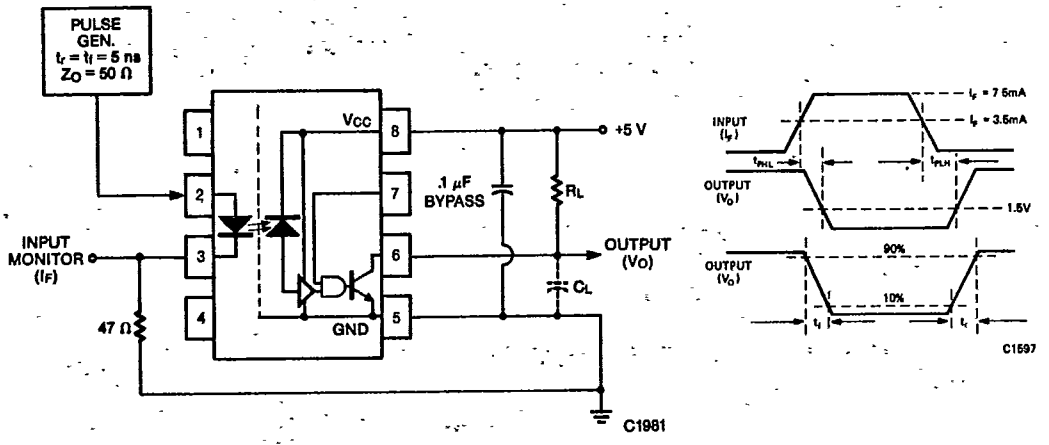


Fig. 10. Test Circuit and Waveforms for t_{PLH}, t_r, and t_f

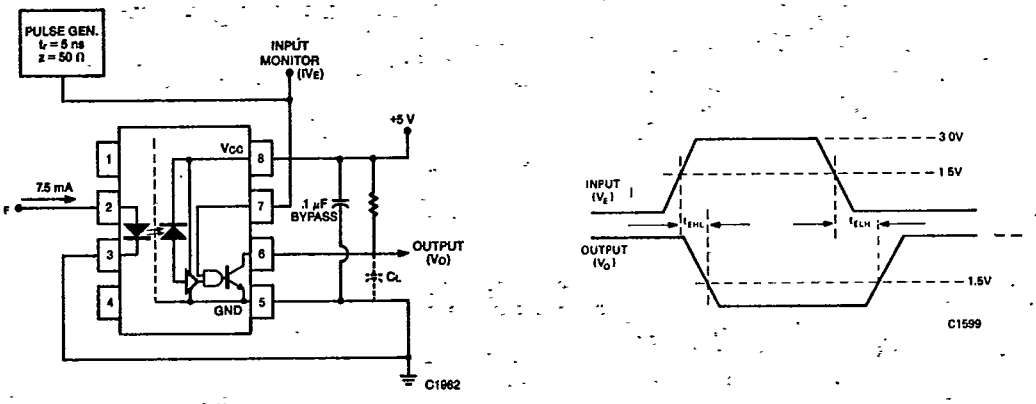


Fig. 11. Test Circuit t_{EHL} and t_{ELH}

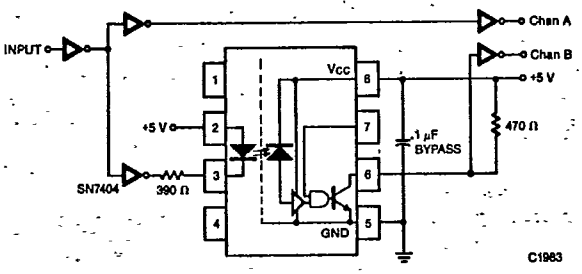


Fig. 12. Response Delay Between TTL Gates

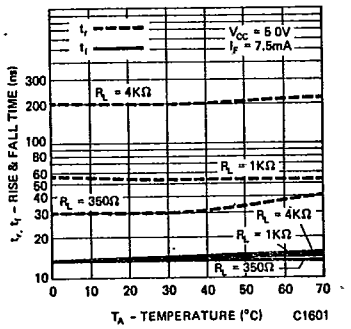


Fig. 13. Rise and Fall Time vs. Temperature

TYPICAL CHARACTERISTIC CURVES (T_A = 25°C Unless Otherwise Specified)

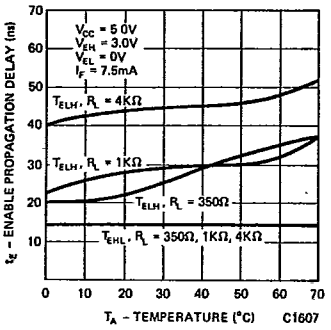


Fig. 14. *Enable Propagation Delay vs. Temperature*

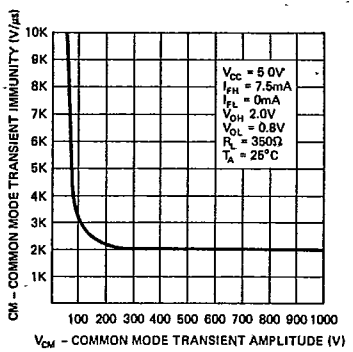


Fig. 15. *Relative Common Mode Transient Immunity vs. Common Mode Transient Amplitude*

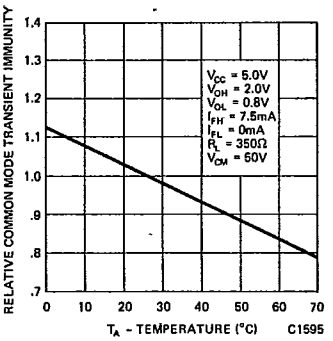


Fig. 16. *Relative Common Mode Transient Immunity vs. Temperature*

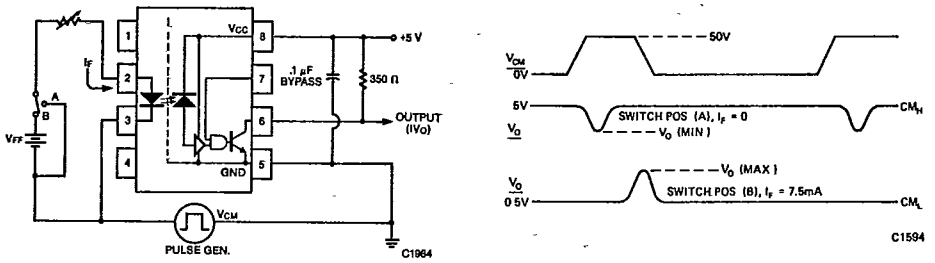


Fig. 17. *Test Circuit Common Mode Transient Immunity*

NOTES

1. *The V_{CC} supply voltage to each 6N137 isolator must be bypassed by a 0.1 μF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins of each device.*
2. *t_{PHL} - Propagation delay is measured from the 3.75 mA level on the LOW to HIGH transition of the input current pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.*
3. *t_{PHL} - Propagation delay is measured from the 3.75 mA level on the LOW to HIGH transition of the input current pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.*
4. *t_f - Fall time is measured from the 10% to the 90% levels of the HIGH to LOW transition on the output pulse.*
5. *t_r - Rise time is measured from the 90% to the 10% levels of the LOW to HIGH transition on the output pulse.*
6. *t_{EHL} - Enable input propagation delay is measured from the 1.5 V level on the LOW to HIGH transition of the input voltage pulse to the 1.5 V level on the HIGH to LOW of the output voltage pulse.*
7. *t_{ELH} - Enable input propagation delay is measured from the 1.5 V level on the HIGH to LOW transition of the input voltage pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.*
8. *CM_L - The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state (i.e., V_{OUT} < 0.8 V). Measured in volts per microsecond (V/μs).*
9. *CM_H - The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high state (i.e., V_{OUT}> 2.0 V). Measured in volts microsecond (V/μs).*
10. *- Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together, and Pins 5, 6, 7 and 8 shorted together. The 2500 V_{AC}/1 minute capability guarantees 3000 V_{DC}/5 sec. as registered with JEDEC and is validated by a factory 3.1 K V_{AC}/1 second.*
11. *Enable Input - No pull up resistor required as the device has an internal pull up resistor.*
12. *- DC current transfer ratio is defined as the ratio of the output collector current to the forward bias input current times 100%.*