VT1621 and VT1621M TV Encoder

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VIA TECHNOLOGIES, INC.

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REVISION HISTORY

Document Release	Date	Revision	Initials
1.0	6/17/02	Initial Public Release	EY

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VT1621 and VT1621M
TV Encoder

PRODUCT FEATURES

- **TV output supporting inputs up to 800x600 graphics resolutions**
- **Supports digital RGB (15/16 or 24-bit) or YCrCb (CCIR601 or CCIR656) 16 bit 4:2:2 input video data in both interlaced or non-interlaced formats**
- **Supports NTSC(M and J) or PAL (B, D, G, H, I, M, N and Nc) TV output standards**
- **Supports Macrovision 7.1 anti-copy protection (VT1621M only)**
- **Underflow check and coring function for reducing the input noise**
- **Composite, S-Video and SCART output support**
- **Flicker filtering to enhance to TV image quality**
- **Dot crawl control circuit to still this phenomenon**
- **Master or slave video timing operation**
- **New Algorithm for text sharpness**
- **High Quality 3 x 9-bit Video DAC**
- **Serial bus programming interface**
- **Programmable power management**
- **Automatic detection of TV presence**
- **Buffered crystal clock output pin**
- **ProScale™ engine support for underscan and overscan mode**
- **44-pin TQFP package**

OVERVIEW

The VT1621 and VT1621M are television encoders that accept various RGB or YCrCb pixel data streams from a VGA controller or MPEG decoder and generates high quality flicker-free composite and Y/C (S-video) signals. Both of these chips contain the same functionality and register. The only variation is that the VT1621 is Macrovision disabled and the VT1621M is Macrovision enabled. Both of these chips can accept any digital input format from 512x384 to 800x600. The input data is also compliant with CCIR656 and CCIR601.

These two TV Encoder chips use VIA's ProScale technology to provide the most advanced vertical and horizontal scaling for the display of non-interlaced data on interlaced TV. This ProScale technology also converts the lines of input video stream data to an appropriate number of output lines for producing a full-screen high quality TV image.

Worldwide video standards are supported, including NTSC-M (North America, Taiwan) NTSC-J (Japan), PAL-B, D, G, H, I (Europe, Asia), PAL-M (Brazil), PAL-N (Uruguay, Paraguay) and PAL-Nc (Argentina). The VT1621M can output a video with the Macrovision 7.1 anticopy included video signal. The Macrovision anti-copy process provides a means to deter any unauthorized copying of copy protected analog video signals onto a videocassette. All features are software programmable through a serial bus interface that provides read/write access to all registers.

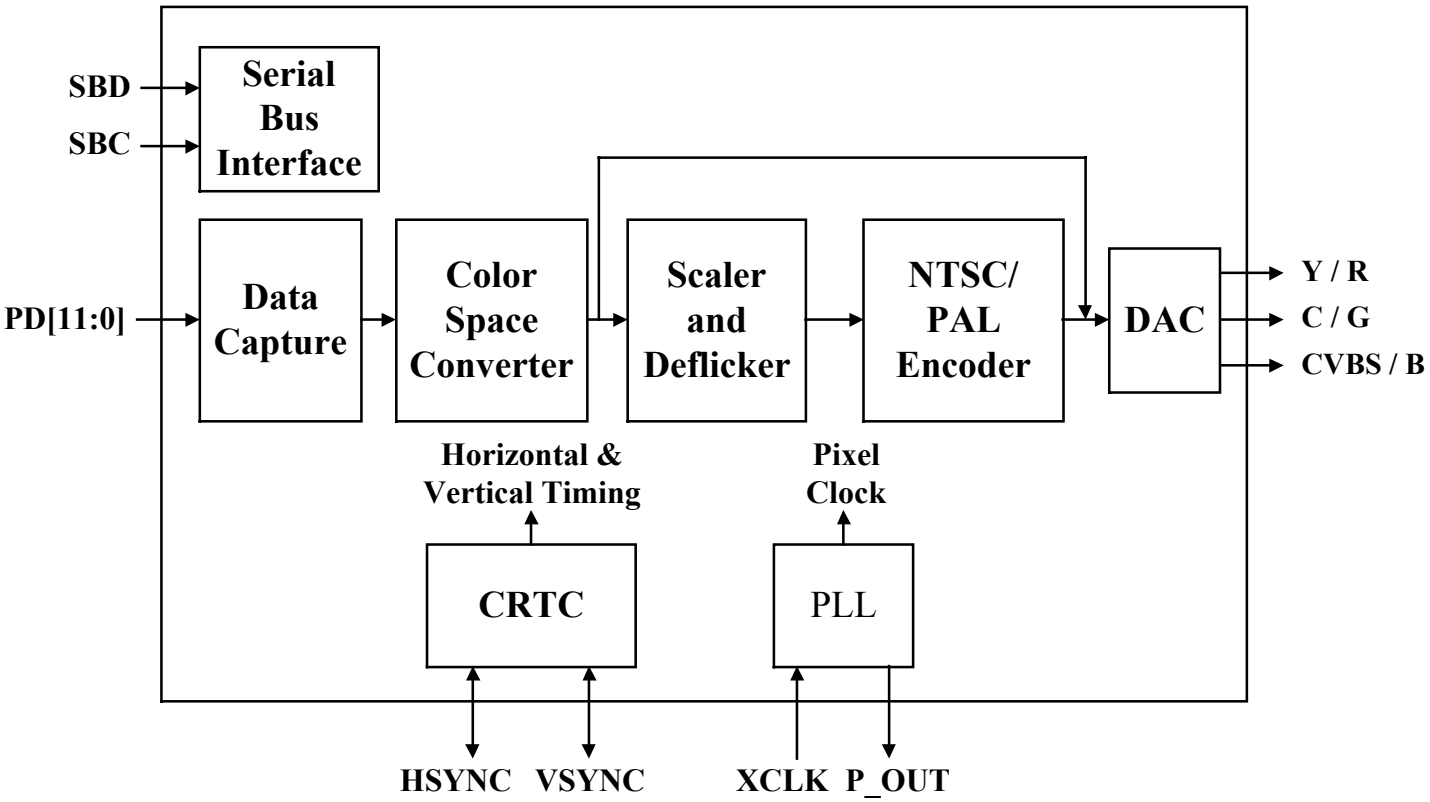


Figure 1. Functional Block Diagram

PINOUTS

Pin Diagram

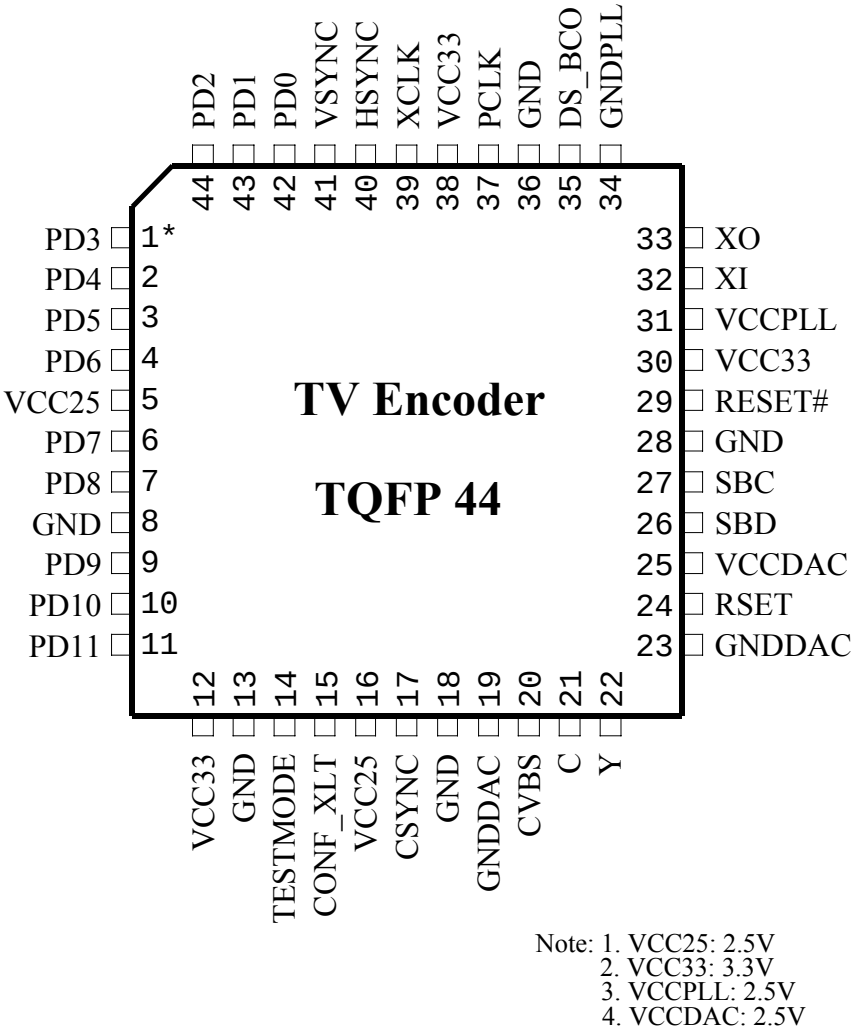


Figure 2. Pin Diagram (Top View)

Pin List

Table 1. Pin List (Alphabetical Order)

Pin		Pin Name	Pin		Pin Name
21	O	C	6	IO	PD7
15	I	CONF_XLT	7	IO	PD8
17	IO	CSYNC	9	IO	PD9
20	O	CVBS	10	IO	PD10
35	IO	DS_BCO	11	IO	PD11
8	**P**	**GND**	29	I	RESET#
13	**P**	**GND**	24	I	RSET
18	**P**	**GND**	27	I	SBC
28	**P**	**GND**	26	IO	SBD
36	**P**	**GND**	14	I	TESTMODE
19	**P**	**GNDDAC**	**5**	**P**	**VCC25**
23	**P**	**GNDDAC**	**16**	**P**	**VCC25**
34	**P**	**GNDPLL**	**12**	**P**	**VCC33**
40	IO	HSYNC	**30**	**P**	**VCC33**
37	IO	PCLK	**38**	**P**	**VCC33**
42	IO	PD0	**25**	**P**	**VCCDAC**
43	IO	PD1	**31**	**P**	**VCCPLL**
44	IO	PD2	41	IO	VSYNC
1	IO	PD3	39	I	XCLK
2	IO	PD4	32	I	XI
3	IO	PD5	33	I	XO
4	IO	PD6	22	O	Y

Pin Descriptions

Table 2. Pin Descriptions

SIGNALS			
Signal Name	**Pin #**	**Type**	**Description**
PD[11-0]	11, 10, 9, 7, 6, 4, 3, 2, 1, 44, 43, 42	IO	Input for pixel data. These inputs can accept 8 or 12 bit multiplexed RGB or YCbCr format. Output for testing only.
HSYNC	40	IO	When Rx1[2]=0, this pin can accept a horizontal sync input. When Rx1[2]=1, the device will output a horizontal sync pulse through this pin.
VSYNC	41	IO	When Rx1[3]=0, this pin can accept a vertical sync input. When Rx1[3]=1, the device will output a vertical sync pulse through this pin.
XCLK	39	I	Reference clock for PDs. It can operate on 1X, 2X or 3X pixel clock.
PCLK	37	IO	Pixel clock output. This pin can provide and operate on 1X, 2X or 3X pixel clock to VGA. Input for testing only.
DS_BCO	35	IO	Input for display enable. The rising edge of this signal identifies the first active pixel of data for each active line. Output for providing a 14.31818 MHz clock to other devices.
Y	22	O	Luminance output for general TV system.
C	21	O	Chrominance output for general TV system.
CVBS	20	O	Composite video output for general TV system.
CSYNC	17	IO	Composite sync. Input for testing only.
SBD	26	IO	Serial bus data pin.
SBC	27	I	Serial bus clock pin.
TESTMODE	14	I	Test mode enable. Pull down for regular operation.
CONF_XLT	15	I	Selects internal or external oscillator. When pulled low, a crystal must be attached to pins 32 and 33. If pulled high, a stable 14.31818MHz external clock source must be supplied to pin 32, XI.
RESET#	29	I	When this pin is low, the device is held in the power-on reset condition.
XI	32	I	A 14.31818 MHz crystal is attached between XI and XO. An oscillator can also be connected to this pin.
XO	33	I	A 14.31818 MHz crystal is attached between XI and XO. If an external oscillator is attached with XI, this pin should be connected to ground.
RSET	24	I	An external resistor, typically 4.87kΩ, attached between this pin and ground sets the FS (full scale) range of the DACs.

Power and Ground			
Signal Name	**Pin #**	**Type**	**Description**
VCC33	**38, 30, 12**	**P**	**I/O Power. 3.3V**
GND	**13, 36**	**P**	**I/O Ground**
VCC25	**5, 16,**	**P**	**Digital Power. 2.5V**
GND	**8, 18, 28**	**P**	**Digital Ground**
VCCPLL	**31**	**P**	**PLL Power. 2.5V**
GNDPLL	**34**	**P**	**PLL Ground**
VCCDAC	**25**	**P**	**DAC Power. 2.5V**
GNDDAC	**23, 19**	**P**	**DAC Ground**

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers that apply to the VT1621 and VT1621M TV Encoder. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details).

Detailed register descriptions are provided in the following section of this document. All offset and default values are shown in hexadecimal unless otherwise indicated.

Table 3. Register Summary

Offset	TV Encoder Registers	Default	Acc
00	Input Frame Format	00	RW
01	Input Sync Format	00	RW
02	Scaling / Chroma Filter	00	RW
03	Luma Filter	00	RW
04	Output Mode	00	RW
05	Control 1	00	RW
06	Control 2	00	RW
07	Start Active Video	00	RW
08	Start Horizontal Position	00	RW
09	Start Vertical Position	00	RW
0A	Cr Amplitude Factor	00	RW
0B	Black Level	00	RW
0C	Luma Amplitude Factor	00	RW
0D	Cb Amplitude Factor	00	RW
0E	Power Management	00	RW
0F	Status	00	RO
10	Special Effect 0	00	RW
11	Special Effect 1	00	RW
12	PLL P2 Value	00	RW
13	PLL D Value	**05**	RW
14	PLL N Value	**21**	RW
15	PLL Overflow	**04**	RW
16	Sub-carrier Value 0	00	RW
17	Sub-carrier Value 1	00	RW
18	Sub-carrier Value 2	00	RW
19	Sub-carrier Value 3	00	RW
1A	- reserved -	00	–
1B	Version ID	02	RO
1C	Overflow	00	RW
1D	Test 0	00	RW
1E	Test 1	00	RW
1F	Test 2	00	RW
20	TV Sync Step	00	RW
21	TV Burst Envelope Step	00	RW
22	TV Sub-carrier Phase Adjustment	00	RW
23	TV Blank Level	00	RW
24	TV Signal Overflow	00	RW
25-49	- reserved -	00	–
4A	Input Aperture Threshold	00	RW
4B	Input Aperture Delta	00	RW
4C	Aperture Upper Threshold	00	RW
4D	Aperture Lower Threshold	00	RW
4E	Aperture Mode and Delta	00	RW
4F	Coring Function	00	RW
50	Y Delay Control	00	RW
51	UV Delay Control	00	RW
52	Burst Maximum Amplitude	00	RW
53-FF	- reserved -	00	–

Register Descriptions

Offset 00 – Input Frame Format ..... RW

7-5 Frame Resolution

000 512x384..... default
001 720x400
010 640x400
011 640x480
100 800x600
*101 720x576 (for PAL)
*101 720x480 (for NTSC)
*110 800x500 (for PAL)
*110 640x400 (for NTSC)
111 -reserved-
* interlaced input mode

4 RGB Pass through Mode

0 Disable..... default
1 Enable

3-0 Input Data Format

00xx -reserved-..... default = 0000b
0100 12-bit multiplexed RGB (24-bit color) input ("C" multiplex scheme)
0101 12-bit multiplexed RGB (24-bit color) input ("I" multiplex scheme)
0110 8-bit multiplexed RGB (24-bit color) input
0111 8-bit multiplexed RGB (16-bit color) input
1000 8-bit multiplexed RGB (15-bit color) input
1001 8-bit multiplexed YCrCb (Normal) input (Y, Cr and Cb multiplexed)
101x 8-bit multiplexed YCrCb (Cr and Cb shift 128) input (Y, Cr and Cb multiplexed)
110x 8-bit multiplexed YCrCb (Y shift 16) input (Y, Cr and Cb multiplexed)
111x 8-bit multiplexed YCrCb (Y shift 16 and Cr and Cb shift 128) input (Y, Cr and Cb multiplexed)

Offset 01 – Input Sync Format..... RW

7 Reserved .....always reads 0

6 Field Signal Polarity

0 Active Low ..... default
1 Active High

5 DS_BCO Pin Control

0 BCO Output ..... default
1 DS Input

4 Detect Embedded Sync

0 Don't detect..... default
1 Sync will be detected from the embedded codes on the pixel input stream

3 Vertical Sync Direction

0 Input ..... default
1 Output

2 Horizontal Sync Direction

0 Input ..... default
1 Output

1 Vertical Sync Polarity

0 Active Low ..... default
1 Active High

0 Horizontal Sync Polarity

0 Active Low ..... default
1 Active High

Offset 02 – Scaling / Chroma Filter Control ..... RW

7-6 Reserved ..... always reads 0

5-3 Scaling Ratio

000 1/1 ..... default
001 3/4
010 5/4
011 5/6
100 7/8
101 7/10

2 Reserved ..... always reads 0

1-0 Chroma Channel Deflicker Adjust

00 No Deflicker Filter ..... default
01 1:1:1 Deflicker Filter
1x 1:2:1 Deflicker Filter

Offset 03 – Luma Filter Control..... RW

7-2 Reserved ..... always reads 0

1-0 Luma Channel Deflicker Adjust

00 No Deflicker Filter ..... default
01 1:1:1 Deflicker Filter
1x 1:2:1 Deflicker Filter

Offset 04 – Output Mode ..... RW

7 Reserved ..... always reads 0

6 YCbCr to YUV Conversion

0 Disable..... default
1 Enable

5 Reserved ..... always reads 0

4 PAL_N Mode

0 Disable..... default
1 Enable (bits 1-0 must be 00b)

3 PAL_Nc Mode

0 Disable..... default
1 Enable (bits 1-0 must be 00b)

2 Reserved ..... always reads 0

1 Output Line Selection

0 625 ..... default
1 525

0 Output TV Standard

0 PAL ..... default
1 NTSC

Offset 05 – Control 1..... RW

7 Reserved ..... always reads 0

6 Master / Slave Clock Mode Select

0 Master Clock Mode ..... default
1 Slave Clock Mode

5 Reserved ..... always reads 0

4 FSCI Auto Adjust

0 Disable ..... default
1 FSCI Auto Adjust Enable, use 14.31818 MHz to calculate FSCI [31:0]

3 FSCI Auto Fine Tune

0 Disable ..... default
1 Enable

2 PCLK Clock Polarity

0 ..... default
1

1-0 PCLK Output Mode

00 1X ..... default
01 2X
1x 3X

Offset 06 – Control 2..... RW

7 Color Bar

0 Disable ..... default
1 Enable

6-5 XCLK Input Clock Mode

00 1X ..... default
01 2X
1x 3X

4 Edge Used to Latch Input Data

0 ..... default
1

3-0 Input Clock Adjust

0000 ..... default
…
1111

Offset 07 – Start Active Video ..... RW

7-0 Start Active Video Bits 7-0.....default = 00h
Sets the delay from the leading edge of horizontal sync to start of active video. See Rx1C[3] for bit-8.

Offset 08 –Start Horizontal Position ..... RW

7-0 Start Horizontal Position Bits 7-0 .....default = 00h
Used to shift the displayed TV image in a horizontal direction. See Rx1C[2] for bit-8.

Offset 09 – Start Vertical Position..... RW

7-0 Start Vertical Position Bits 7-0.....default = 00h
Used to shift the displayed TV image in a vertical direction. See Rx1C[1] for bit-8.

Offset 0A – Cr Amplitude Factor ..... RW

7-0 Cr Amplitude Factor ..... default = 00h

Offset 0B – Black Level ..... RW

7-0 Black Level ..... default = 00h

Offset 0C – Luma Amplitude Factor ..... RW

7-0 Luma Amplitude Factor ..... default = 0

Offset 0D – Cb Amplitude Factor ..... RW

7-0 Cb Amplitude Factor ..... default = 0

Offset 0E – Power Management ..... RW

7-4 Reserved ..... always reads 0

3 DAC Sense

0 Disable ..... default

1 Enable

2 Reserved ..... always reads 0

1 S-Video DAC Power State

0 On ..... default

1 Off

0 Composite DAC Power State

0 On ..... default

1 Off

Offset 0F – Status ..... RO

7 Macrovision Copy Protection

0 Disable ..... default

1 Enable

6 Reserved ..... always reads 0

5-3 MS_POS

0 ..... default

1

2 YT

0 ..... default

1

1 CT

0 ..... default

1

0 CVBST

0 ..... default

1

Offset 10 – Special Effect 0 ..... RW

7-0 Hue Adjust Bits 7-0 (see Rx11[7-5]).... default = 00h

Offset 11 – Special Effect 1 ..... RW

7-5 Hue Adjust Bits 10-8 (see Rx10)..... default = 000b
4 Reserved ..... always reads 0
3 Dot Crawl
0 Enable..... default
1 Disable
2-0 Reserved ..... always reads 0

Offset 12 – PLL P2 Value ..... RW

7-4 Reserved ..... always reads 0
3-0 Second Post Divider Control ..... default = 0

Offset 13 – PLL D Value (05h) ..... RW

7-5 Resister Selection Bits 2-0 (see Rx15[0]). default = 0
4-0 Pre-Divider Control ..... default = 00101b

Offset 14 – PLL N Value (21h) ..... RW

7-0 VCO Output Division Factor Bits 7-0
(see Rx15[1] for bit-8) ..... default = 21h

Offset 15 – PLL Overflow (04h) ..... RW

7-6 Reserved ..... always reads 0
5-2 First Post Divider Control ..... default = 0001b
1 VCO Output Division Factor Bit-8 (see Rx14)
..... default = 0
0 Resister Selection Bit-3 (see Rx13[7-5]).. default = 0

Offset 16 – Sub-Carrier Value 0 ..... RW

7-0 Sub-Carrier Value Bits 7:0 .....default = 00h

Offset 17 – Sub-Carrier Value 1 ..... RW

7-0 Sub-Carrier Value Bits 15:8 .....default = 00h

Offset 18 – Sub-Carrier Value 2 ..... RW

7-0 Sub-Carrier Value Bits 23:16 .....default = 00h

Offset 19 – Sub-Carrier Value 3 ..... RW

7-0 Sub-Carrier Value Bits 31:24 .....default = 00h

Offset 1B – Version ID..... RO

7-0 Version ID (VID) .....always reads 02h

Offset 1C – Overflow ..... RW

7-4 Reserved .....always reads 0
3 Start Active Video Bit-8 (see Rx7).....default=0
2 Start Horizontal Position Bit-8 (see Rx8) .default=0
1 Start Vertical Position Bit-8 (see Rx9) .....default=0
0 Reserved .....always reads 0

Offset 1D – Test 0 ..... RO

7 Software Reset: 0: Reset

6-4 Scaler and Deflicker Test

000 Normal ..... default
001 BIST_EN:1:BIST Enable
01x -reserved-
1x1 Scale Test Mode 0
(VSI, HSI, PDI[15:12], PDI[11:0])
11x Scale Test Mode 1
(VSI, HSI, PDI[15:12], PDO[11:0])

3-2 Encoder Test

(VSI, HSI, DSI, PDI[15:8], PDO[4:0])
00 Normal ..... default
01 Chrominance test
10 Luminance test
11 Composite test

1 Internal Register Parallel Testing (Read Mode) (PDO[7:0])

0 Disable ..... default
1 Enable

0 Internal Register Parallel Testing (Write Mode) (PDI[14:0])

0 Disable ..... default
1 Enable

Offset 1E – Test 1 ..... RW

7 Test TV Out

0 ..... default
1

6 Turn On Input Clock Mode

0 ..... default
1

5 CSYNC Output Enable

0 Output Mode ..... default
1

4 PD[15:12] Bus

0 Input Mode ..... default
1 Output Mode

3 PD[11:8] Bus

0 Input Mode ..... default
1 Output Mode

2 PD[7:4] Bus

0 Input Mode ..... default
1 Output Mode

1 PD[3:0] Bus

0 Input Mode ..... default
1 Output Mode

0 Test Input Pad

0 ..... default
1

Offset 1F – Test 2 ..... RW

7-6 Y DAC Control

00 Normal function ..... default
01 DAC off
10 Test DAC
11 Invert test DAC

5-4 C DAC Control

00 Normal function ..... default
01 DAC off
10 Test DAC
11 Invert test DAC

3-2 Composite DAC Control

00 Normal function ..... default
01 DAC off
10 Test DAC
11 Invert test DAC

1-0 Test I2C

0 ..... default
1

Offset 20 – TV Sync Step ..... RW

7-0 TV Sync Step ..... default = 00h
Step value to control the shape / slope of the sync. The msb is defined in TV signal overflow register Rx24[0].

Offset 21 – TV Burst Envelope Step ..... RW

7-0 TV Burst Envelope Step ..... default = 00h
Step value to control the shape / slope of the burst. The msb is defined in TV signal overflow register Rx24[1].

Offset 22 – TV Sub-Carrier Phase Adjustment ..... RW

7-0 TV Sub-Carrier Phase Adjustment .... default = 00h
Step value to control the shape / slope of the burst. The msbs are defined in TV signal overflow register Rx24[4-2].

Offset 23 –TV Blank Level..... RW

7-0 TV Blank Level..... default = 00h
Step value to control the base level of the blank signal. The msb is defined in TV signal overflow register Rx24[5].

Offset 24 – TV Signal Overflow ..... RW

7-6 Reserved ..... always reads 0
5 Bit[8] of TV Blank Level..... default = 0
4-2 Bit[10:8] of Sub-Carrier Phase Adjustment
..... default = 0
1 Bit[8] of TV Burst Envelope Step ..... default = 0
0 Bit[8] of TV Sync Step (Rx20)..... default = 0

Offset 4A – Input Aperture Threshold ..... RW

7-0 Input Data Threshold..... default = 00h

Offset 4B - Input Aperture Delta ..... RW

7-0 Input Data Adjustment Value ..... default = 00h

Offset 4C – Aperture Upper Threshold..... RW

7-0 Text Enhancement Upper Threshold.. default = 00h

Offset 4D – Aperture Lower Threshold..... RW

7-0 Text Enhancement Lower Threshold . default = 00h

Offset 4E – Aperture Mode ..... RW

7 Aperture Mode
0 Normal..... default
1 Inverse
6-0 Adjustment Delta..... default = 0

Offset 4F – Coring Function ..... RW

7 Coring Function
0 Disable ..... default
1 Enable
6-0 Coring Function Threshold .....default = 0

Offset 50 – Y Delay Control..... RW

7-3 Reserved .....always reads 0
2-0 Y Delay Depth.....default = 0

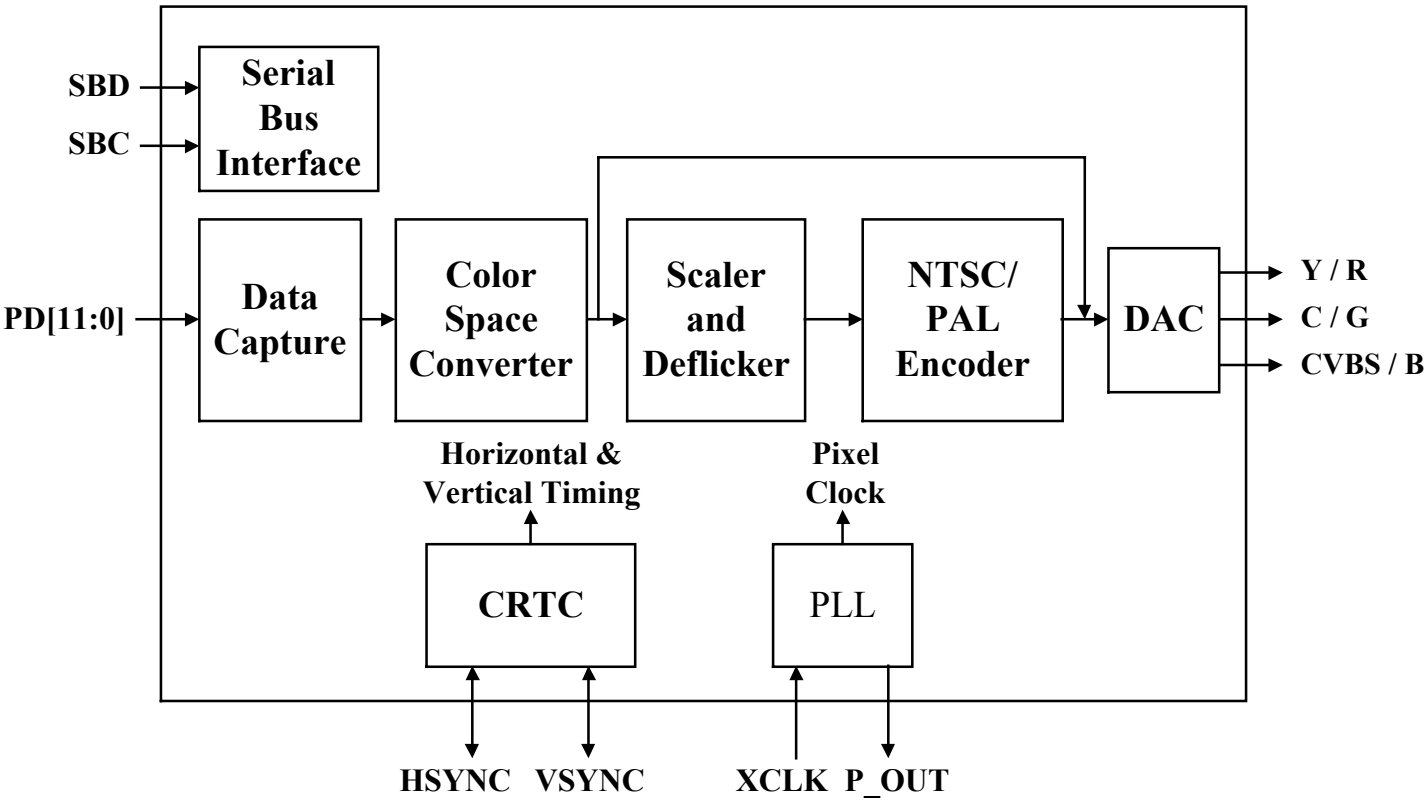
Offset 51 – UV Delay Control ..... RW

7 Burst Maximum Amplitude Bit-8 (see Rx52) .def=0
6-4 U Delay Depth.....default = 0
3 Y, Cb, Cr Underflow Check
0 Disable ..... default
1 Enable
2-0 V Delay Depth.....default = 0

Offset 52 – Burst Maximum Amplitude..... RW

7-0 Burst Maximum Value (see Rx51[7]).....default = 0

FUNCTIONAL DESCRIPTION



Architecture Description

Data Capture

The 8-bit or 12-bit multiplexed input data is captured by this module and is transferred to 24-bit data for one pixel.

Color Space Converter

The data from the Data Capture module is RGB or YCrCb format. This module converts both formats to YUV 422 format.

Scaler and Deflicker

This module converts the lines of input pixel data to the appropriate number of output lines for producing a full-screen image on the television receiver. The image can be scaled to 100% within the viewable area of the screen. The device can perform vertical filtering to reduce the effects of picture flicker due to the interlacing of the output image. Because this process trades off vertical resolution in order to reduce flicker, the amount of flicker filtering is programmable and allows the process to be optimized for the specific image. This module finally generates the YUV444 pixel data of the interlaced image to the encoder module.

Encoder

This module accepts the YUV444 pixel data and converts it to a standard baseband television signal that is compatible with worldwide standards including PAL (B, D, G, H, I, N, Nc, M) and NTSC (M, J). The Y data can be manipulated for contrast control and a setup level can be added for brightness control. The U, V data can be scaled to achieve color saturation control. Besides, U, V signals are modulated by the appropriate subcarrier sine/cosine waveforms and a phase offset may be added onto the color subcarrier during active video to allow hue adjustment. The resulting U and V signals are added together to make up the chrominance signal. The luma (Y) and chroma signals are added together to make up the composite video signal. Separated luma and chroma signals make up the S-video signal.

DAC

Both VT1621 and VT1621M contain three DACs. Each DAC is used to convert digital composite or luma / chroma data to analog signals and can be individually powered off if not required. The DAC module also has an auto-detection circuit, which provides a way to sense the connection of a TV to either S-video or composite Video outputs.

Serial bus Interface

Both VT1621 and VT1621M contain a standard serial bus control port through which the control registers can be written and read. The serial bus address is 40h.

CRTC

Normally the VGA controller supplies the horizontal and vertical sync signals. However, they could be generated either by the VT1621 or the VT1621M. This module generates the horizontal and vertical sync signals. In CCIR656 input mode, the embedded sync may also be used.

PLL

Both VT1621 and VT1621M contain a high accuracy, low-jitter phase-locked-loop to create outstanding quality video. Normal operation requires the encoding clock to be generated by the PLL. In master clock mode, the reference clock of the PLL is provided by OSC and the frequency is 14.31818 MHz. In slave clock mode, the reference clock is from the XCLK pin.

Master/Slave Clock Mode

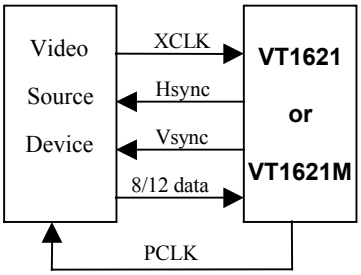
Both VT1621 and VT1621M can be configured either as master or slave clock mode. In master clock mode, the VT1621 and VT1621M provide the pixel clock signal to the video source and expect incoming data to be available when required. In slave clock mode, the VT1621 and VT1621M accept the external pixel clock from the video source.

Master mode

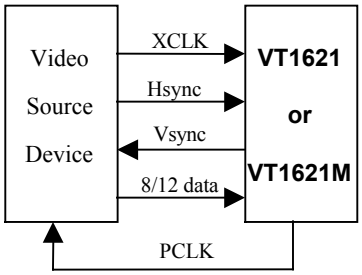
In master clock mode, the VT1621 and VT1621M work as a master and the video source device works as a slave. The VT1621 and VT1621M provide a clock signal through the PCLK pin to the video source device and the video source device will use this clock as a frequency reference. Then the video source will generate a clock signal into the XCLK pin. The VT1621 and VT1621M will use this clock signal to latch incoming data. The PCLK clock signal can also be used as the input clock signal connected directly to the XCLK pin. The HSYNC and VSYNC signals can be programmed to be either input or output to the TV Encoder. The master clock mode can be configured as mode 1 and mode 2 illustrated in Figure 3 and Figure 4.

Slave Mode

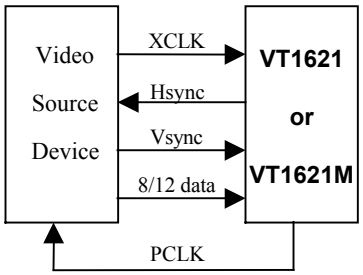
In slave clock mode, the VT1621 and VT1621M work as a slave and the video source device works as a master. The video source device will generate a clock signal input to the XCLK pin. Through the XCLK pin, the TV Encoder receives a clock from the video source device and uses this clock to latch incoming data. Moreover, this clock will be a reference clock of the VT1621 or the VT1621M for generating a pixel clock. The HSYNC and VSYNC signals can be programmed to be either input or output to the VT1621 and VT1621M. In slave clock mode, both VT1621 and VT1621M can be configured as illustrated in Figure 5.



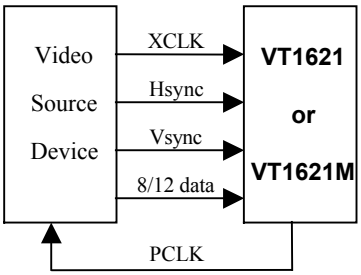
Configuration 1



Configuration 2

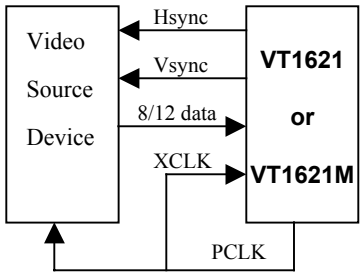


Configuration 3

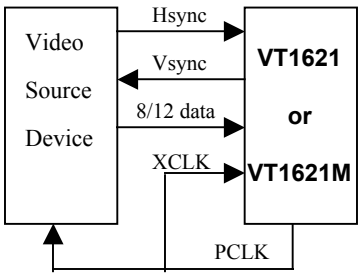


Configuration 4

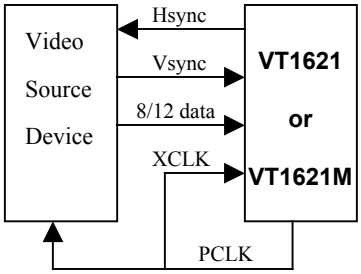
Figure 3. Master Clock Mode 1



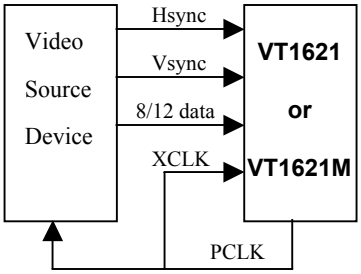
Configuration 5



Configuration 6

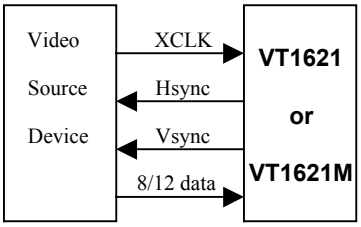


Configuration 7

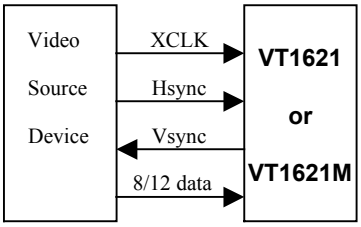


Configuration 8

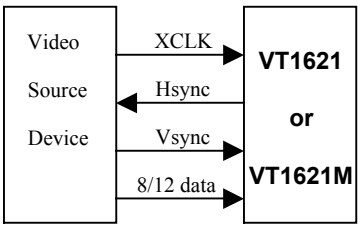
Figure 4. Master Clock Mode 2



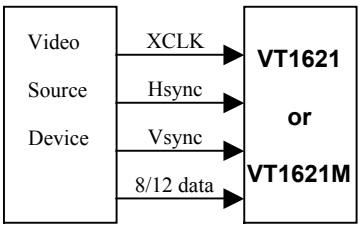
Configuration 1



Configuration 2



Configuration 3



Configuration 4

Figure 5. Slave Clock Mode

Digital Video Interface

The VT1621 and the VT1621M can both be configured with an 8-bit or 12-bit data bus. It accepts RGB 16-bit, RGB 15-bit, RGB 24-bit or YCrCb 16-bit (CCIR 656) data format.

- **8-bit multiplexed mode**
  - RGB 15-bit: 5-5-5 over two bytes
  - RGB 16-bit: 5-6-5 over two bytes
  - RGB 24-bit: 8-8-8 over three bytes
  - YCrCb 16-bit: Cb, Y0, Cr, Y1
- **12-bit multiplexed mode**
  - RGB 24-bit: 8-8-8 over two words

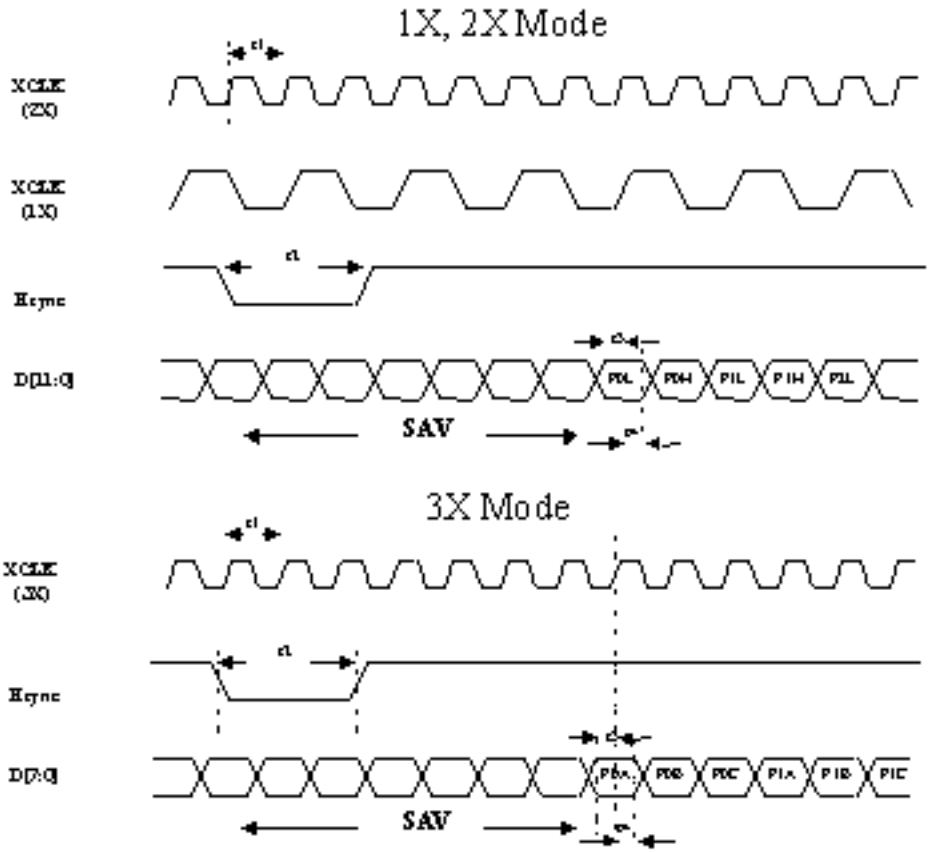


Figure 6. Input Interface Protocol

Each rising edge (or each rising and falling edge) of the XCLK signal will latch data from the video source device. The multiplexed input data formats are shown in Figure 6. The Pixel Data bus represents an 8 or 12-bit multiplexed data stream, which contains either RGB or YCrCb formatted data. In IDF settings 4, 5, 7, 8 and 9, the input data rate is 2X the pixel clock frequency and each pair of P# values (for example, P#A and P#B) will contain a complete pixel, encoded as shown in Table 4. When IDF = 6, the input data rate is 3X the pixel clock frequency and each triplet of P# values (for example, P#A, P#B and P#C) will contain a complete pixel, encoded as shown in Table 4. When the input is YCrCb, the color-difference data will be transmitted at half the data rate of the luminance data, with the sequence being set as Cb, Y, Cr, Y. When IDF = 9 (YCrCb 8-bit mode), the H and V sync signals can be embedded into the data stream. In this mode, the embedded sync will follow the CCIR656 convention and the first byte of the "video timing reference code" will be assumed to occur when a Cb sample would occur if the video stream is continuous.

Table 4. Input Data Format

IDF	4 24-bit RGB		5 24-bit RGB		6 24-bit RGB			7 16-bit RGB		8 15-bit RGB		9~ 16-bit YCrCb	
Pin	P#A	P#B	P#A	P#B	P#A	P#B	P#C	P#A	P#B	P#A	P#B	P#A	P#B
PD11	G3	R7	G4	R7									
PD10	G2	R6	G3	R6									
PD9	G1	R5	G2	R5									
PD8	G0	R4	B7	R4									
PD7	B7	R3	B6	R3	B7	G7	R7	G2	R4	G2	x	Cr/Cb7	Y7
PD6	B6	R2	B5	G7	B6	G6	R6	G1	R3	G1	R4	Cr/Cb6	Y6
PD5	B5	R1	B4	G6	B5	G5	R5	G0	R2	G0	R3	Cr/Cb5	Y5
PD4	B4	R0	B3	G5	B4	G4	R4	B4	R1	B4	R2	Cr/Cb4	Y4
PD3	B3	G7	G0	R2	B3	G3	R3	B3	R0	B3	R1	Cr/Cb3	Y3
PD2	B2	G6	B2	R1	B2	G2	R2	B2	G5	B2	R0	Cr/Cb2	Y2
PD1	B1	G5	B1	R0	B1	G1	R1	B1	G4	B1	G4	Cr/Cb1	Y1
PD0	B0	G4	B0	G1	B0	G0	R0	B0	G3	B0	G3	Cr/Cb0	Y0

# Denotes the pixel number

Video Standards

There are several bits in the Output Mode register at offset 04h (see Rx4[1-0] and Rx4[4-3]) that control the generation of popular video standards. These bits control NTSC and PAL video standard encoding parameters. Other registers may also need to be modified to meet every video parameter of the particular video standard to be output. Video timing diagrams are illustrated in Figure 7 through Figure 12 which summarize all the common video standards.

Composite and S-video outputs are supported in either NTSC or PAL format. Figure 13 through Figure 18 illustrate the composite and S-video output waveforms of color test pattern bars.

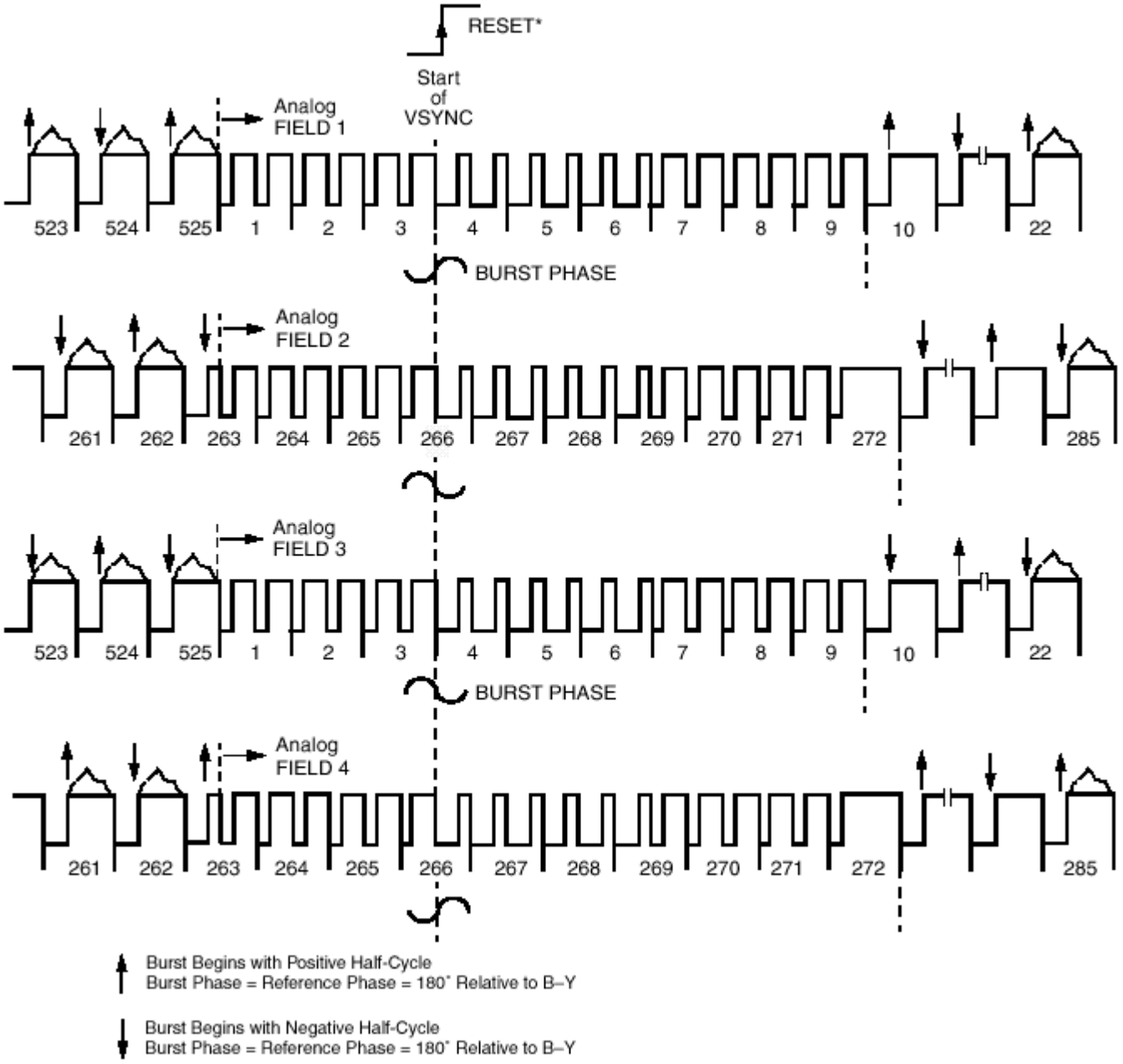


Figure 7. Interlaced 525-Line (NTSC) Video Timing

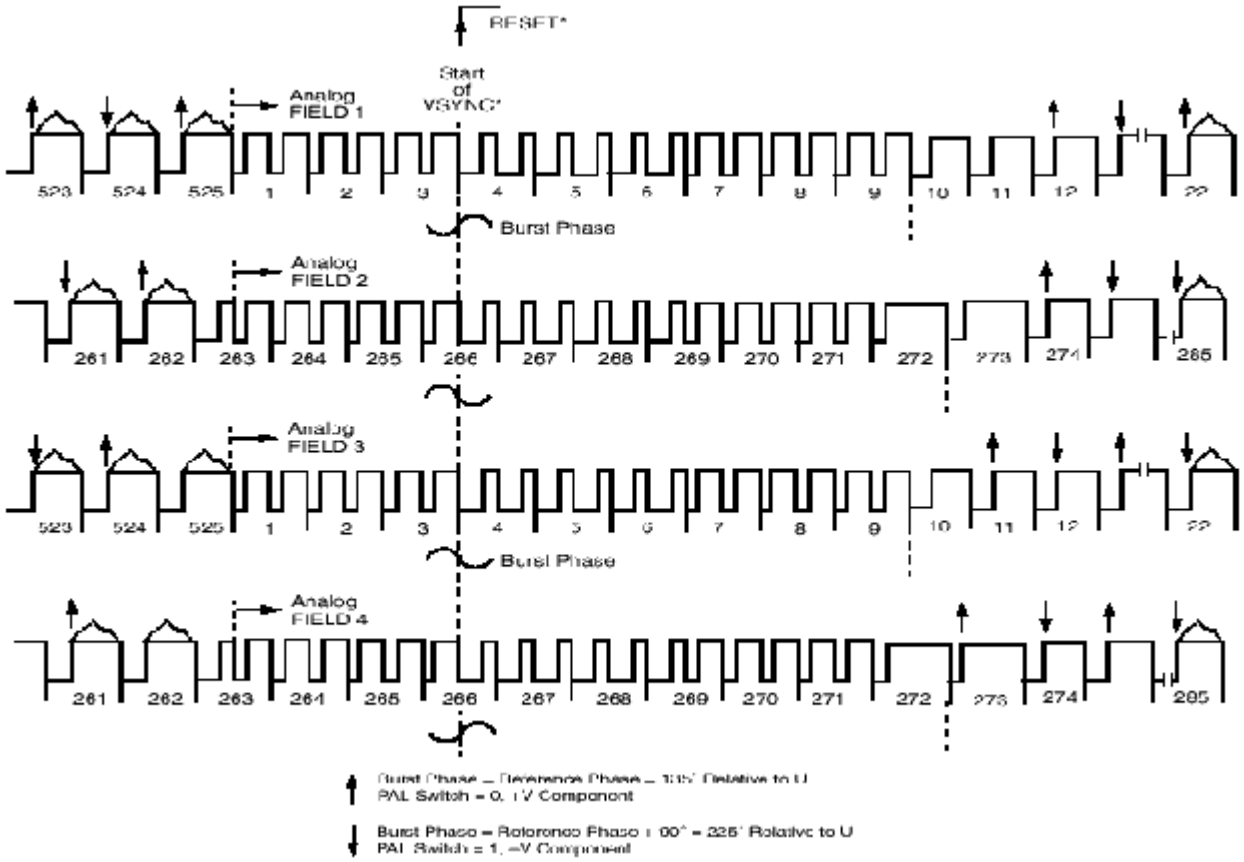


Figure 8. Interlaced 525-Line (PAL-M) Video Timing

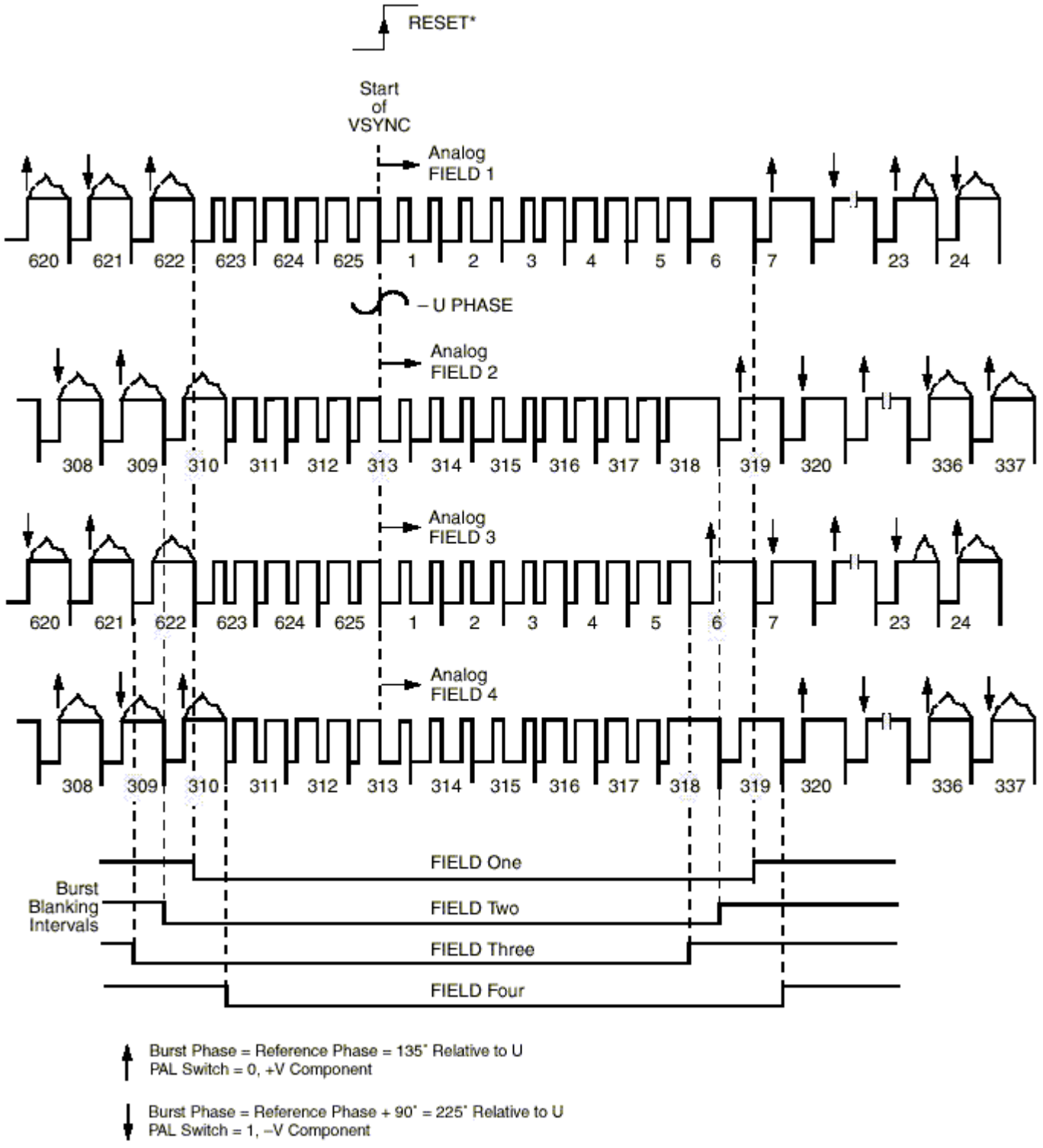


Figure 9. Interlaced 625-Line (PAL-B, D, G, H, I, Nc) Video Timing (Fields 1-4)

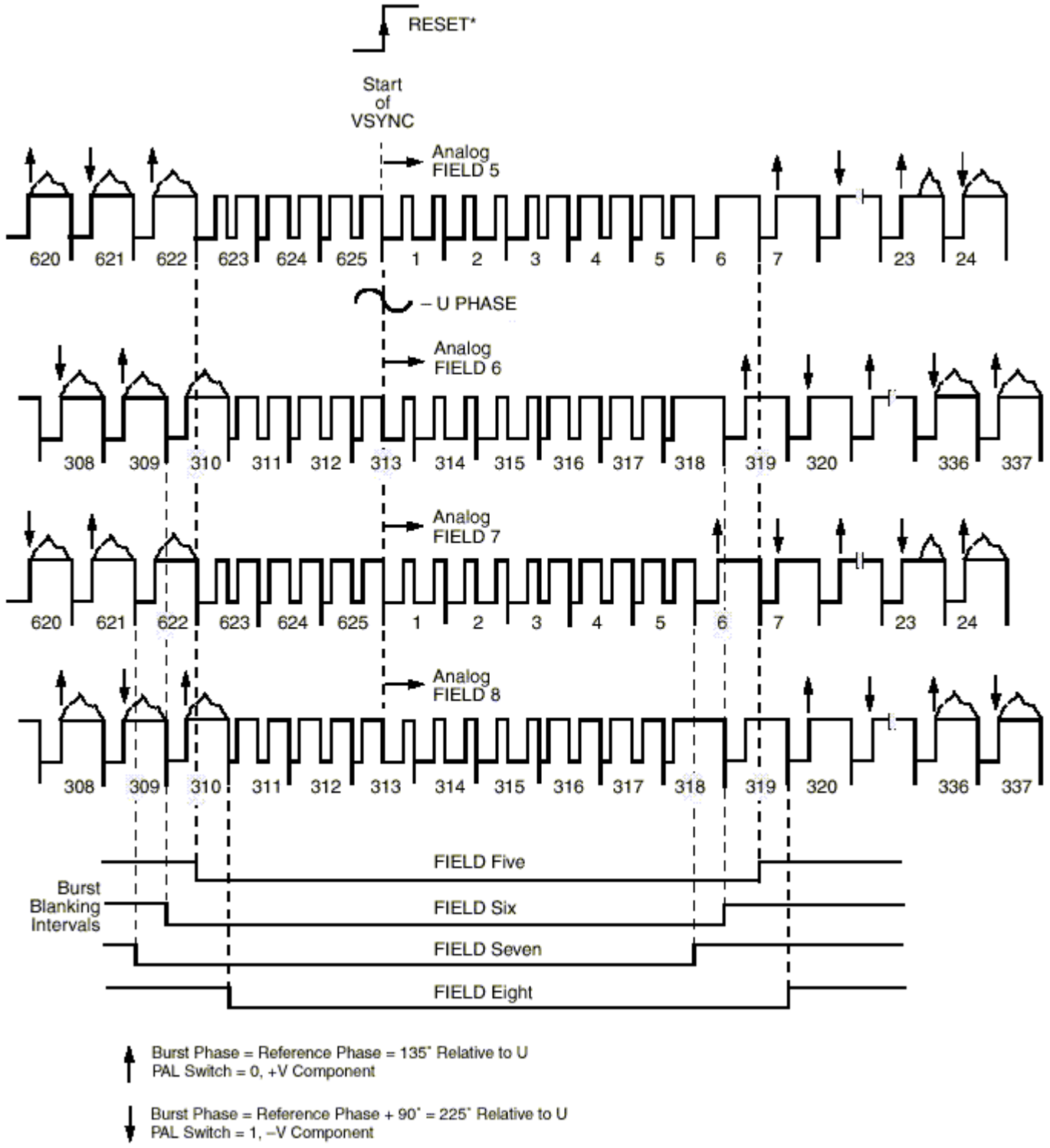


Figure 10. Interlaced 625-Line (PAL-B, D, G, H, I, Nc) Video Timing (Fields 5-8)

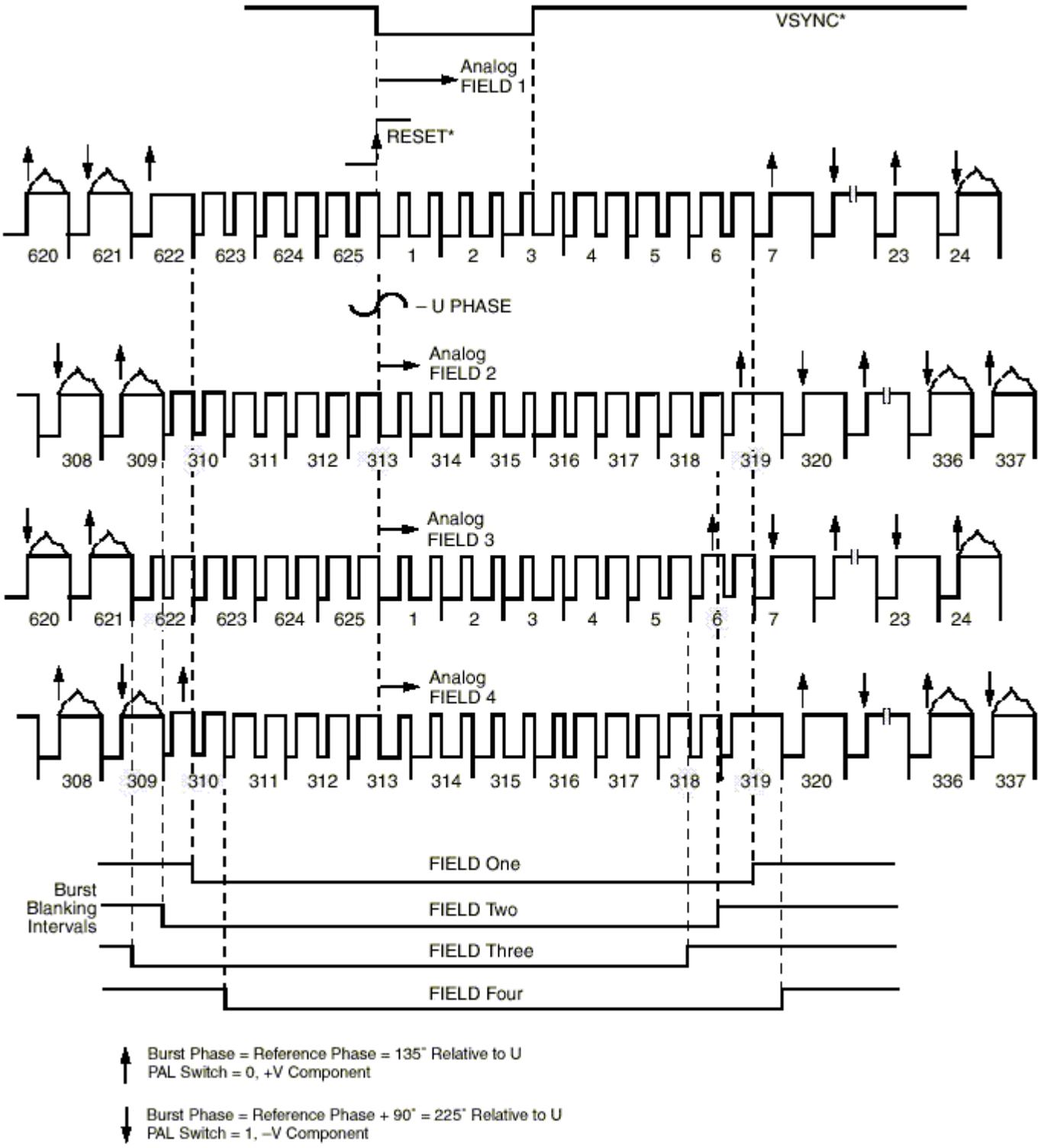


Figure 11. Interlaced 625-Line (PAL-N) Video Timing (Fields 1-4)

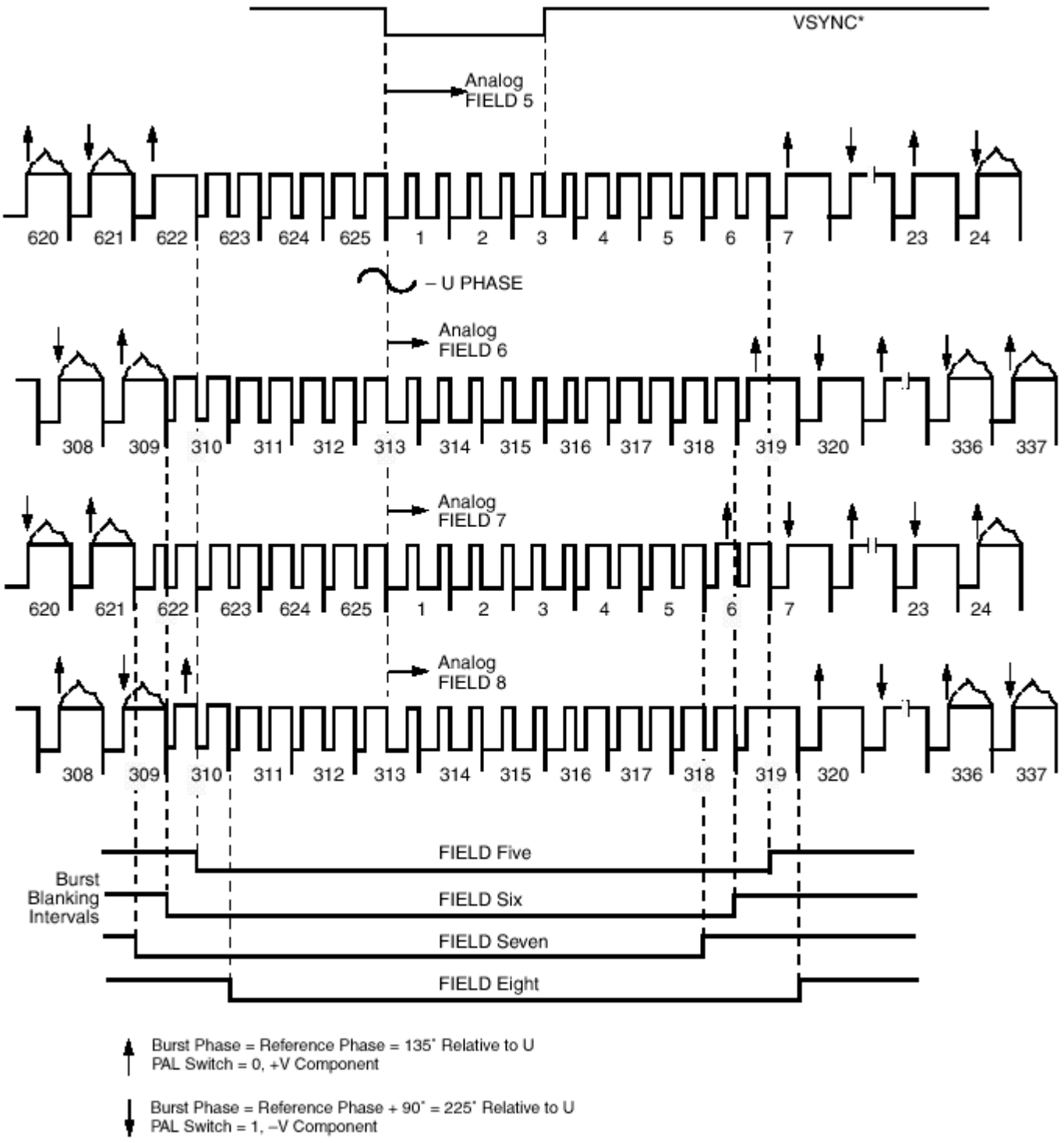


Figure 12. Interlaced 625-Line (PAL-N) Video Timing(Fields 5-8)

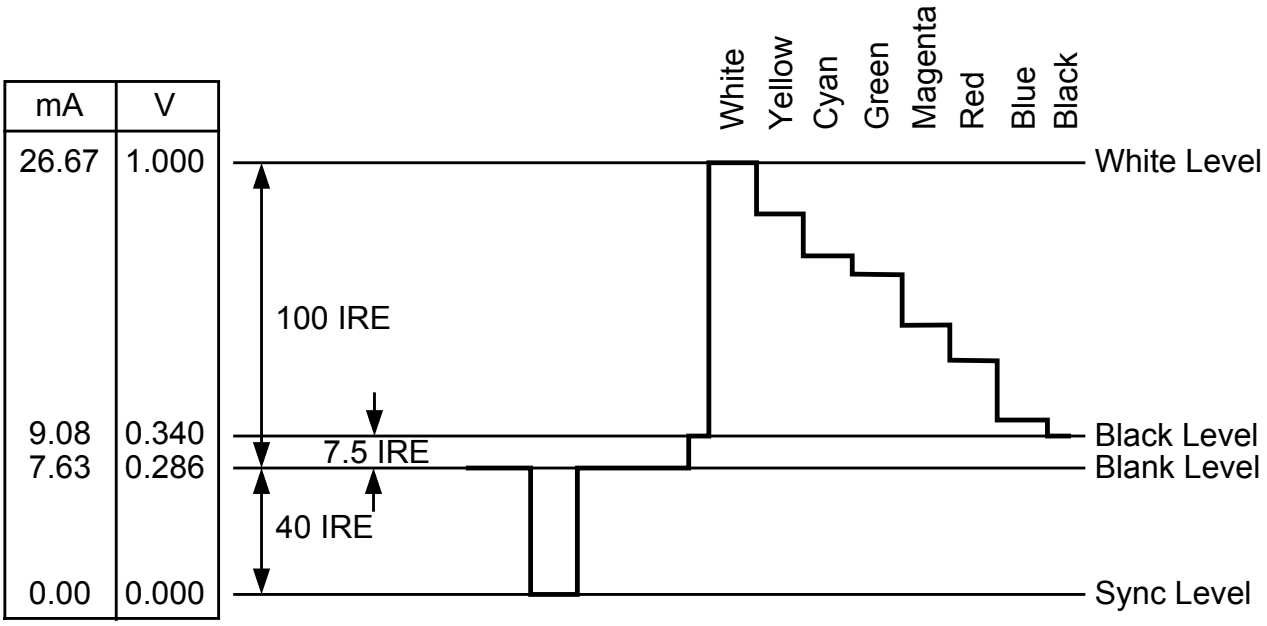


Figure 13. 525-Line (NTSC/PAL-M) Y (Luma) Video Test Pattern Waveform

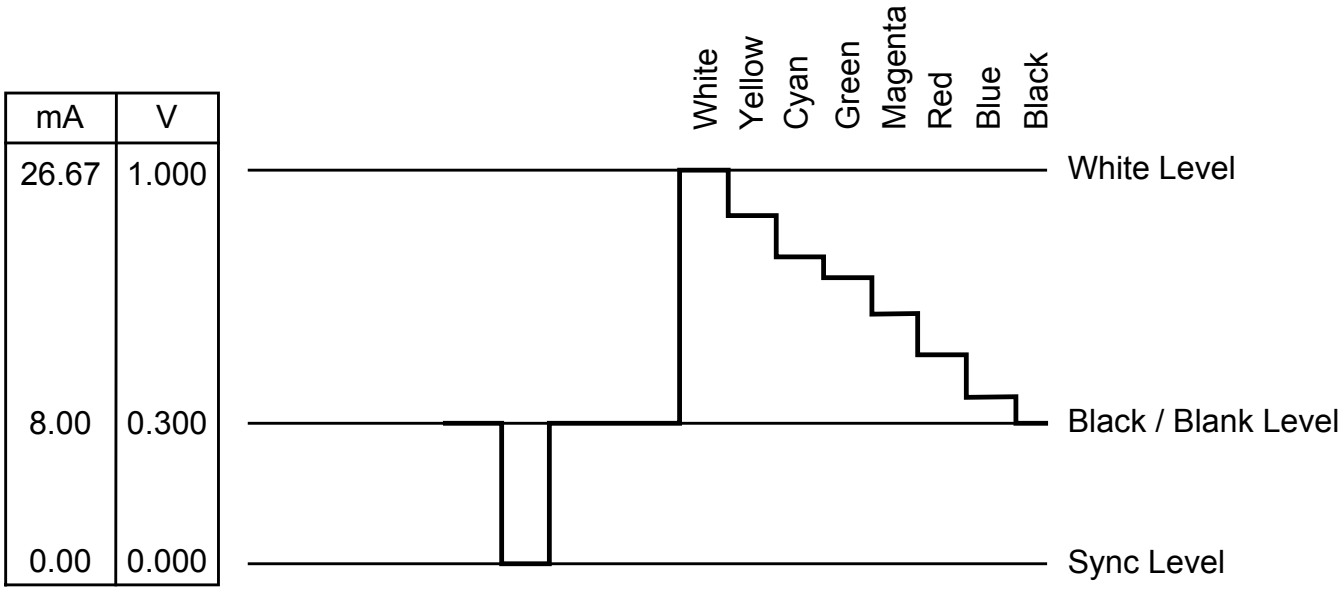


Figure 14. 625-Line (PAL-B, D, G, H, I, N, Nc) Y (Luma) Test Pattern Waveform

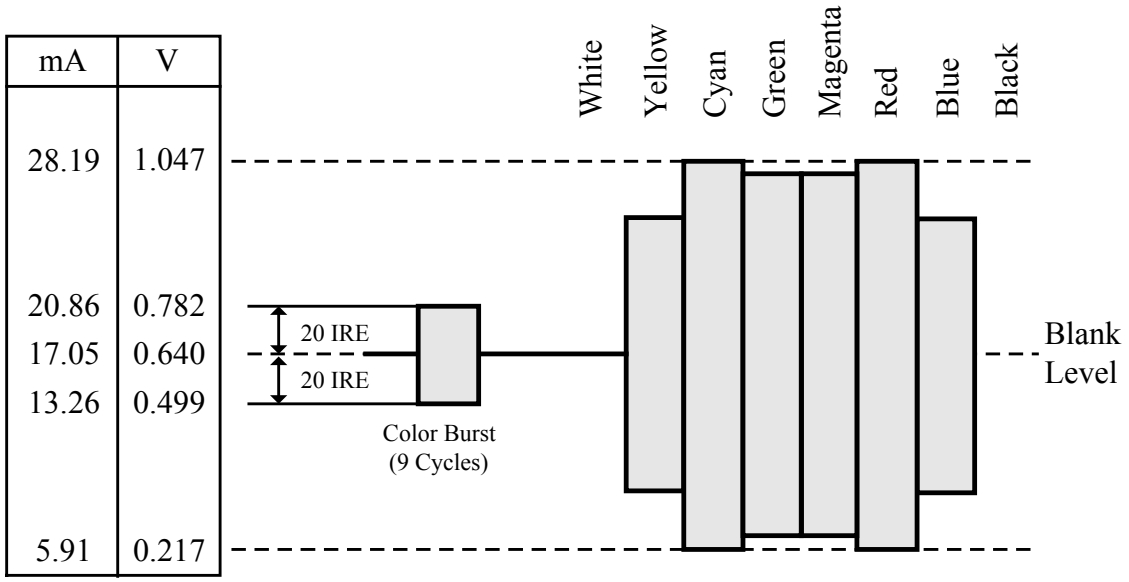


Figure 15. 525-line (NTSC/PAL-M) C (Chroma) Video Test Pattern Waveform

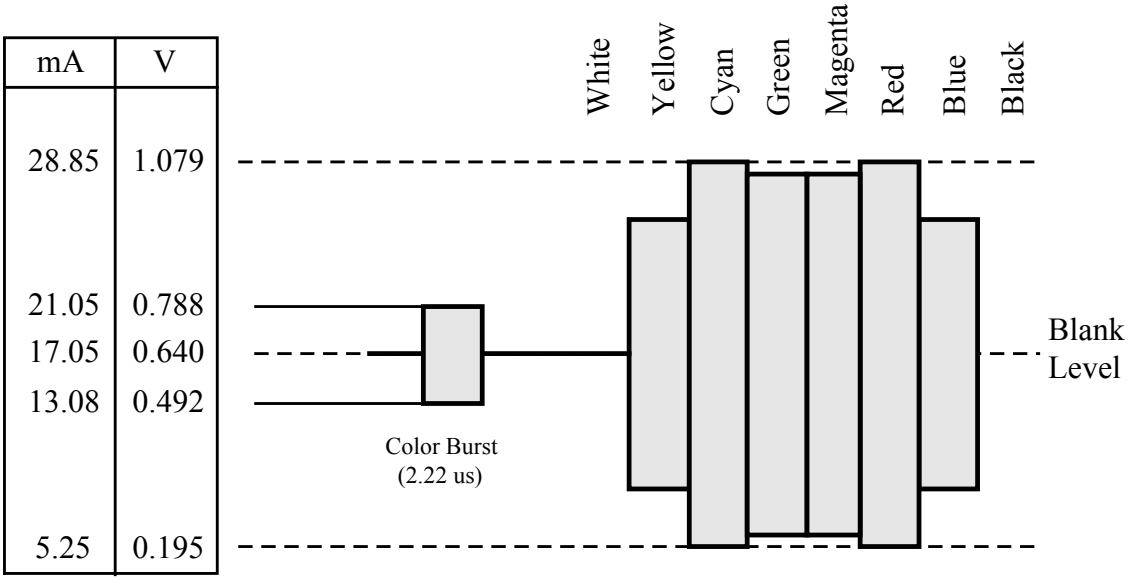


Figure 16. 625-Line (PAL-B, D, G, H, I, N, Nc) C (Chroma) Video Test Pattern Waveform

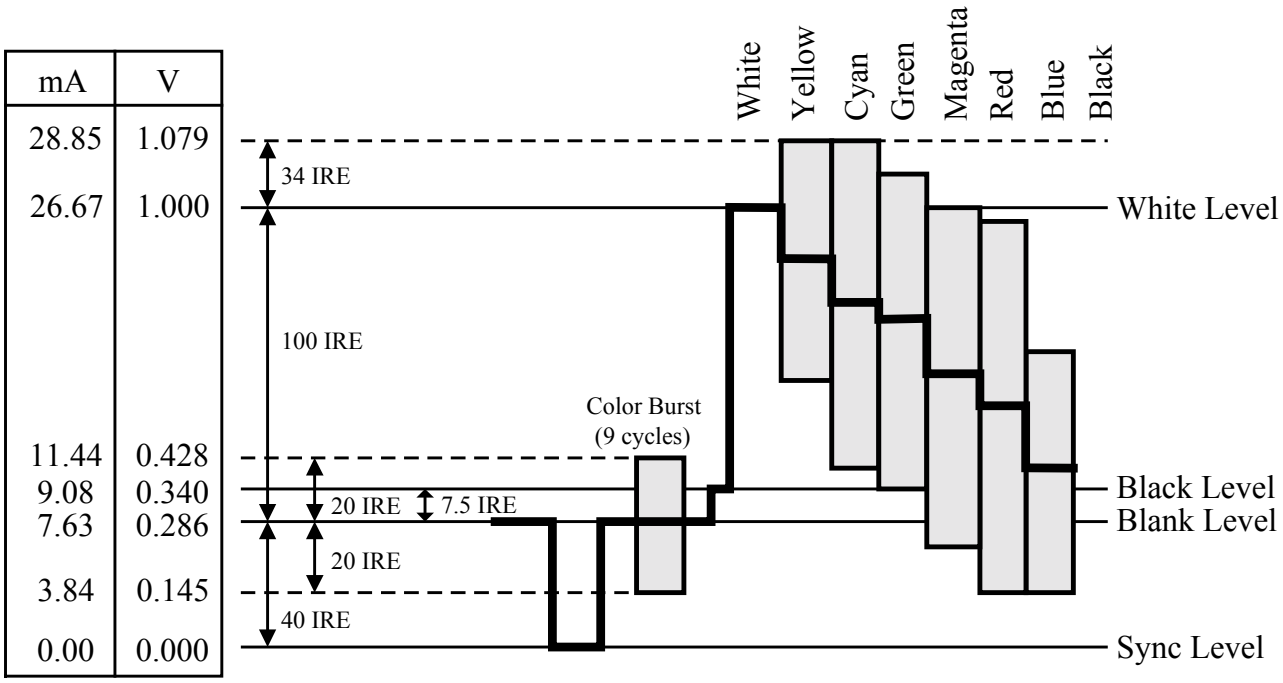


Figure 17. Composite 525-Line (NTSC/PAL-M) Video Test Pattern Waveform

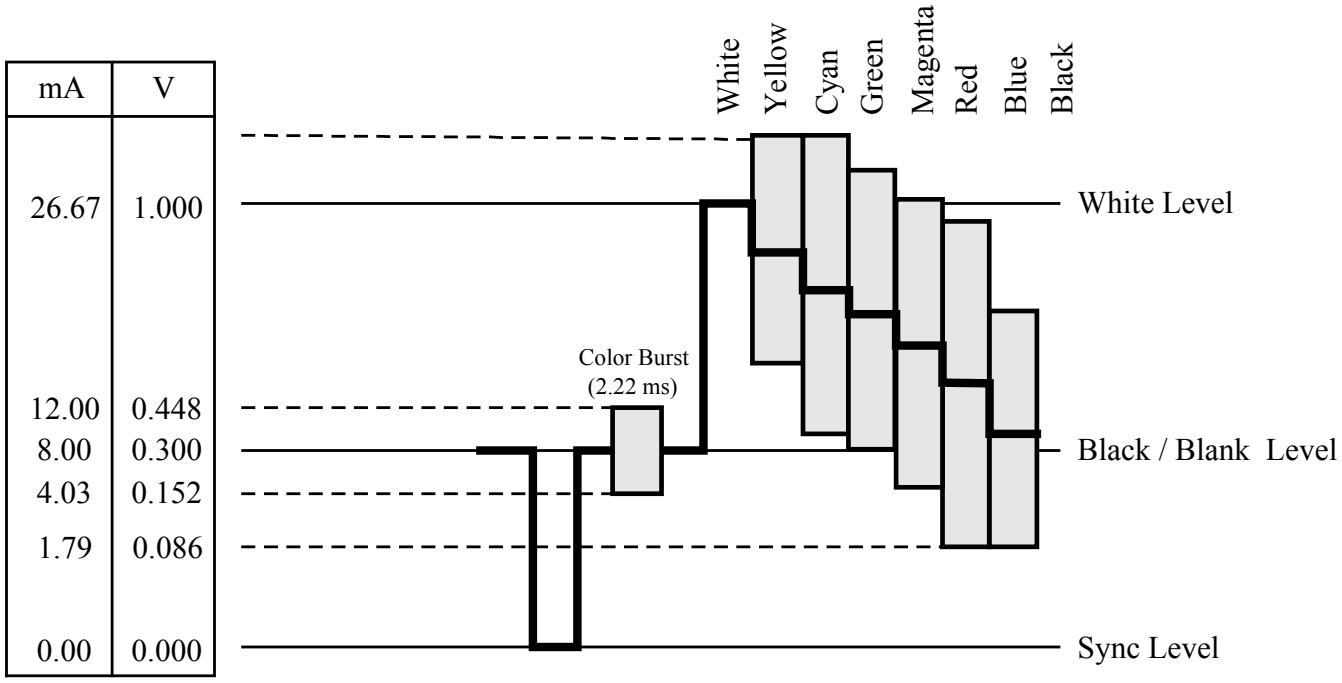


Figure 18. Composite 625-Line (PAL-B, D, G, H, I, N,Nc) Video Test Pattern Waveform

Color Bar Test Pattern Generator

The VT1621 and VT1621M all have a built-in color test pattern generator that produces 75% amplitude and 100% saturation EIA colors for NTSC and PAL video standards as illustrated in Figure 13 through Figure 18.

Subcarrier Generation

This device uses a 32-bit-word to synthesize the subcarrier. The value of the sub-carrier increment required to generate the desired subcarrier frequency is found with the following equations:

NTSC: $FSCI[31:0] = 2^{32} * [455 / (2 * H\_Total)]$
-or- $FSCI[31:0] = (int) (2^{32} * 3.579545 / F_{clk})$

PAL: $FSCI[31:0] = 2^{32} * [(1135/4 + 1/625) / (H\_Total)]$
-or- $FSCI[31:0] = (int) (2^{32} * 4.43361875 / F_{clk})$

The 32-bit Sub-Carrier Value, FSCI, is defined in Rx16-19. H_Total is the number of output pixels desired per line. F_{clk} is the encoder clock frequency if Rx5[4]=0 (FSCI Auto Adjust Disabled); F_{clk}=14.31818MHz if Rx5[4]=1 (FSCI Auto Adjust Enabled). This allows the generation of any desired subcarrier for any desired video standard. The 32-bit subcarrier increment FSCI[31:0] must be loaded by the serial interface before the subcarrier can be enabled. In order to prevent any residual errors from accumulating, the subcarrier is reset every two lines for the NTSC standard and every field for the PAL standard.

Burst Generation

Subcarrier burst generation is a function of the video standard (e.g. NTSC or PAL), the subcarrier frequency increment (FSCI), and the burst horizontal begin and end register settings. The burst will automatically be blanked during horizontal sync to prevent invalid sync pulses from being generated. The burst blanking is automatically controlled by the selected video format. The burst rise and fall times can be configured by programming the chip registers.

Power Down mode

The VT1621 and VT1621M can be powered down by programming their registers. All register contents are maintained when the TV Encoder chip is in power down mode.

Macrovision Anti-Copy Protection

The VT1621M features Macrovision 7.1 anti-copy protection. This algorithm modifies the NTSC/PAL signals to inhibit recording on VCR devices, while not affecting direct TV viewing. All of the parameters that control the anti-copy protection block are fully programmable.

Display Modes

There are a total of 27 display modes. Each mode is determined by four factors: Input resolution, TV standard, TV lines, and Scaling Ratio. Both VT1621 and VT1621M are designed to accept input resolutions of 640x480, 800x600, 640x400 (including 320x200 scan-doubled output), 720x400, and 512x384. The VT1621 and VT1621 are also designed to support output to either NTSC or PAL television standards. The VT1621 and VT1621M all provide interpolated scaling with selectable ratios of 1:1, 3:4, 5:4, 5:6, 7:8 and 7:10 in order to support adjustable overscan or underscan operation when displayed on TV. These combinations of ratios result in a matrix of useful operating modes. PAL-M has 525 lines just like NTSC but the horizontal frequency and the frame rate are different from NTSC. Therefore, PAL-M and NTSC share the same modes but the pixel clock frequency varies. All the modes are listed in Table 5 and Table 6 below.

Table 5. Display Modes for PAL (M)

Mode	Rx00 [7-5]	Rx04 [1-0]	Rx02 [5-3]	Input Format	H_Total * V_Total	Pixel Clock	Output Standard	Scaling
2	000	10	010	512 x 384	800 x 420	20.160020	PAL(M)	5/4
3	000	10	000	512 x 384	784 x 525	24.696025	PAL(M)	1/1
6	001	10	010	720 x 400	945 x 420	23.814024	PAL(M)	5/4
7	001	10	000	720 x 400	936 x 525	29.484029	PAL(M)	1/1
10	010	10	010	640 x 400	840 x 420	21.168021	PAL(M)	5/4
11	010	10	000	640 x 400	840 x 525	26.460026	PAL(M)	1/1
12	010	10	100	640 x 400	840 x 600	30.240030	PAL(M)	7/8
16	011	10	000	640 x 480	784 x 525	24.696025	PAL(M)	1/1
17	011	10	100	640 x 480	784 x 600	28.224028	PAL(M)	7/8
18	011	10	011	640 x 480	800 x 630	30.240030	PAL(M)	5/6
21	100	10	011	800 x 600	1040 x 630	39.312039	PAL(M)	5/6
22	100	10	001	800 x 600	1040 x 700	43.680044	PAL(M)	3/4
23	100	10	101	800 x 600	1064 x 750	47.880049	PAL(M)	7/10
25*	101	10	000	720 x 480	858 x 525	13.513514	PAL(M)	1/1

27*	110	10	000	640 x 400	910 x 525	14.332515	PAL(M)	1/1

* interlaced input mode

Table 6. Display Modes for NTSC (M, J) & PAL (B, D, G, H, I, N, Nc)

Mode	Rx00 [7-5]	Rx04 [1-0]	Rx02 [5-3]	Input Format	H_Total * V_Total	Pixel Clock	Output Standard	Scaling
0	000	00	010	512 x 384	840 x 500	21.000000	PAL	5/4
1	000	00	000	512 x 384	840 x 625	26.250000	PAL	1/1
2	000	11	010	512 x 384	800 x 420	20.139860	NTSC	5/4
3	000	11	000	512 x 384	784 x 525	24.671329	NTSC	1/1
4	001	00	010	720 x 400	1125 x 500	28.125000	PAL	5/4
5	001	00	000	720 x 400	1116 x 625	34.875000	PAL	1/1
6	001	11	010	720 x 400	945 x 420	23.790210	NTSC	5/4
7	001	11	000	720 x 400	936 x 525	29.454545	NTSC	1/1
8	010	00	010	640 x 400	1000 x 500	25.000000	PAL	5/4
9	010	00	000	640 x 400	1008 x 625	31.500000	PAL	1/1
10	010	11	010	640 x 400	840 x 420	21.146853	NTSC	5/4
11	010	11	000	640 x 400	840 x 525	26.433566	NTSC	1/1
12	010	11	100	640 x 400	840 x 600	30.209790	NTSC	7/8
13	011	00	010	640 x 480	960 x 500	24.000000	PAL	5/4
14	011	11	000	640 x 480	840 x 625	26.250000	PAL	1/1
15	011	00	011	640 x 480	840 x 750	31.500000	PAL	5/6
16	011	11	000	640 x 480	784 x 525	24.671329	NTSC	1/1
17	011	11	100	640 x 480	784 x 600	28.195804	NTSC	7/8
18	011	11	011	640 x 480	800 x 630	30.209790	NTSC	5/6
19	100	00	000	800 x 600	944 x 625	29.500000	PAL	1/1
20	100	00	011	800 x 600	960 x 750	36.000000	PAL	5/6
21	100	11	011	800 x 600	1040 x 630	39.272727	NTSC	5/6
22	100	11	001	800 x 600	1040 x 700	43.636364	NTSC	3/4
23	100	11	101	800 x 600	1064 x 750	47.832169	NTSC	7/10
24*	101	00	000	720 x 576	864 x 625	13.500000	PAL	1/1
25*	101	11	000	720 x 480	858 x 525	13.500000	NTSC	1/1
26*	110	00	000	800 x 500	1135 x 625	17.734375	PAL	1/1
27*	110	11	000	640 x 400	910 x 525	14.318182	NTSC	1/1

* interlaced input mode

Filters

The Y components are low-pass filtered, upsampled and low-pass filtered again (for removing the image of upsampling) with a filter response illustrated in Figure 19. The UV components also have the same operations; the filter response is illustrated in Figure 20. The pixel clock is different for each display mode. Therefore, the filter coefficients should be different for each mode so that the TV Encoder can generate a high quality TV image. All the filter coefficients are programmed through the serial bus interface to provide a controllable bandwidth output on both composite and S-video signals.

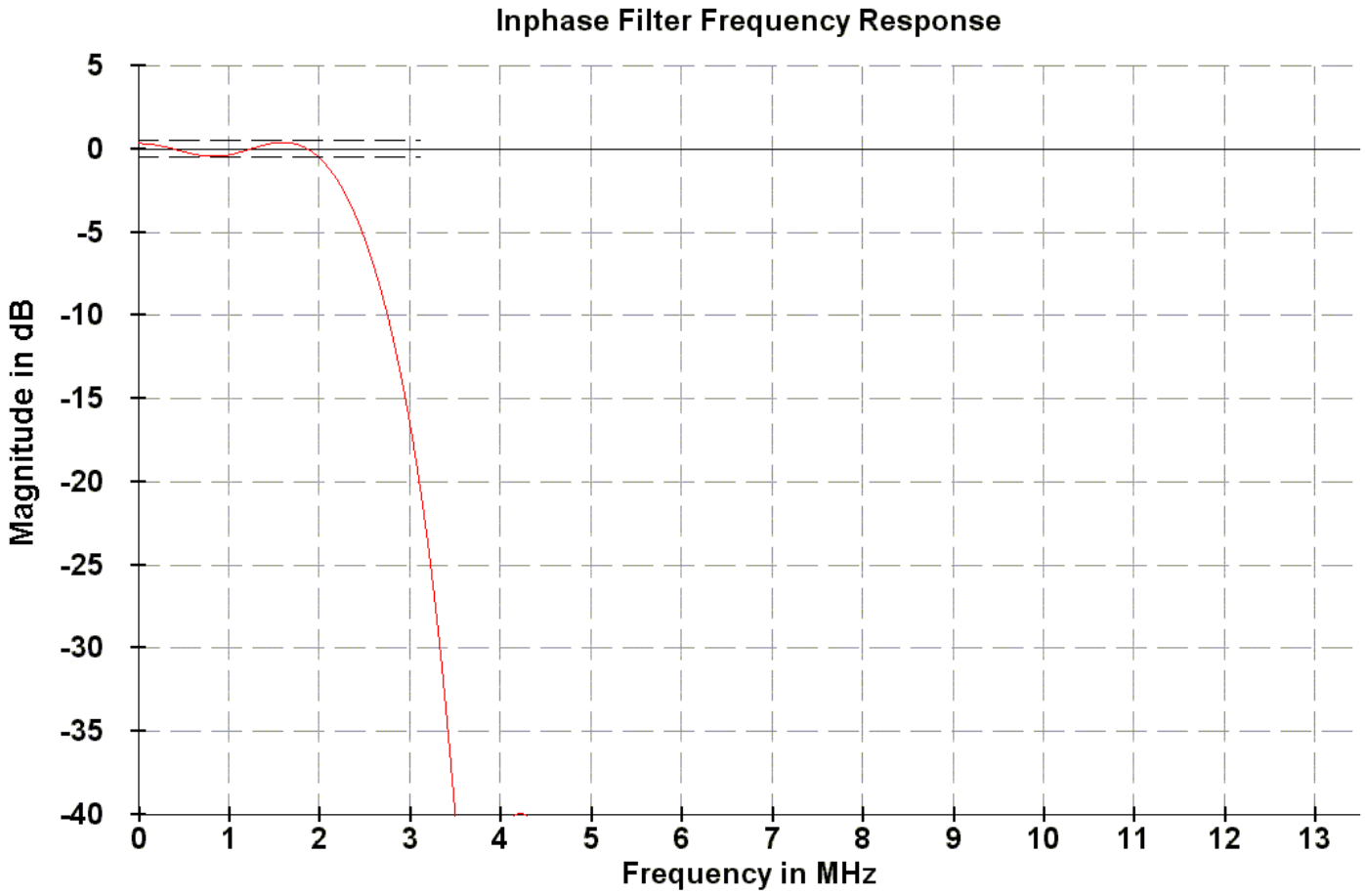


Figure 19. Luminance Lowpass Filter Response (27 MHz)

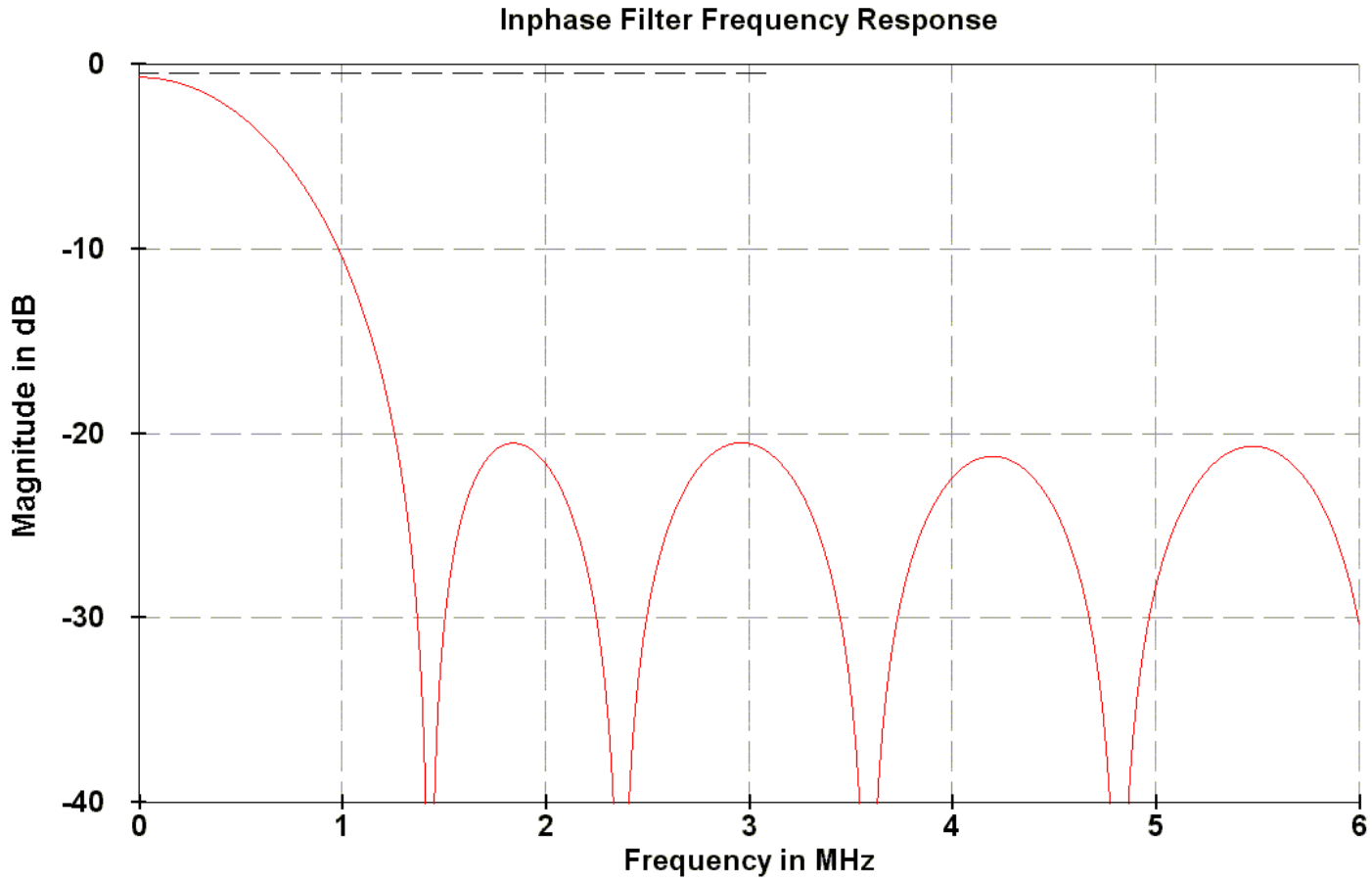


Figure 20. Chrominance Lowpass Filter Response (27MHz)

Clock Frequency

A crystal must be present between the XI and XO pins for generating a 14.31818 MHz reference clock for the PLL (Phase Lock Loop). In master clock mode, the PLL uses this clock as a reference. In slave mode, the PLL uses the clock from the XCLK pin as a reference clock. The PLL generates 2 clocks: One is pixel clock output on the PCLK pin (for master mode use only) and the other is the pixel clock used by the Scaler and Encoder engines. The frequency is calculated by the following formula:

$$F_{clk} = F_{RefClk} * N / (D*P)$$

The settings of the PLL control registers are listed in Table 3 on page 6.

Table 7. Clock Settings

Mode	Pixel(MHz)	D	N	P
0	21.000000	2.5	44	12
1	26.250000	2	44	12
2	20.139860	3.5	64	13
3	24.671329	2.5	56	13
4	28.125000	4	55	7
6	23.790210	2.5	54	13
7	29.454545	2.5	36	7
8	25.000000	3.5	55	9
9	31.500000	2	44	10
10	21.146853	2.5	48	13
11	26.433566	6.5	96	8
12	30.209790	6.5	96	7
13	24.000000	3.5	88	15
14	26.250000	3	44	8
15	31.500000	2	44	10
16	24.671329	2.5	56	13
17	28.195804	6.5	128	10
18	30.209790	6.5	96	7
19	29.500000	14.5	239	8
20	36.000000	2.5	44	7
21	39.272727	3.5	48	5
22	43.636364	3.5	32	3
23	47.832169	6.5	152	7
24*	13.500000	2.5	33	14
25*	13.500000	2.5	33	14
27*	14.318180	2	28	14

PC BOARD LAYOUT CONSIDERATIONS

Component Placement

The TV Encoder chip should be close to the video connectors and close to the video source device (e.g. VGA controller). All other digital components and high-speed digital signal traces should be located as far away as possible from analog circuits. Analog components or analog sections of mixed signal components should be placed directly over the analog power and ground planes and the same applies to the digital counterparts.

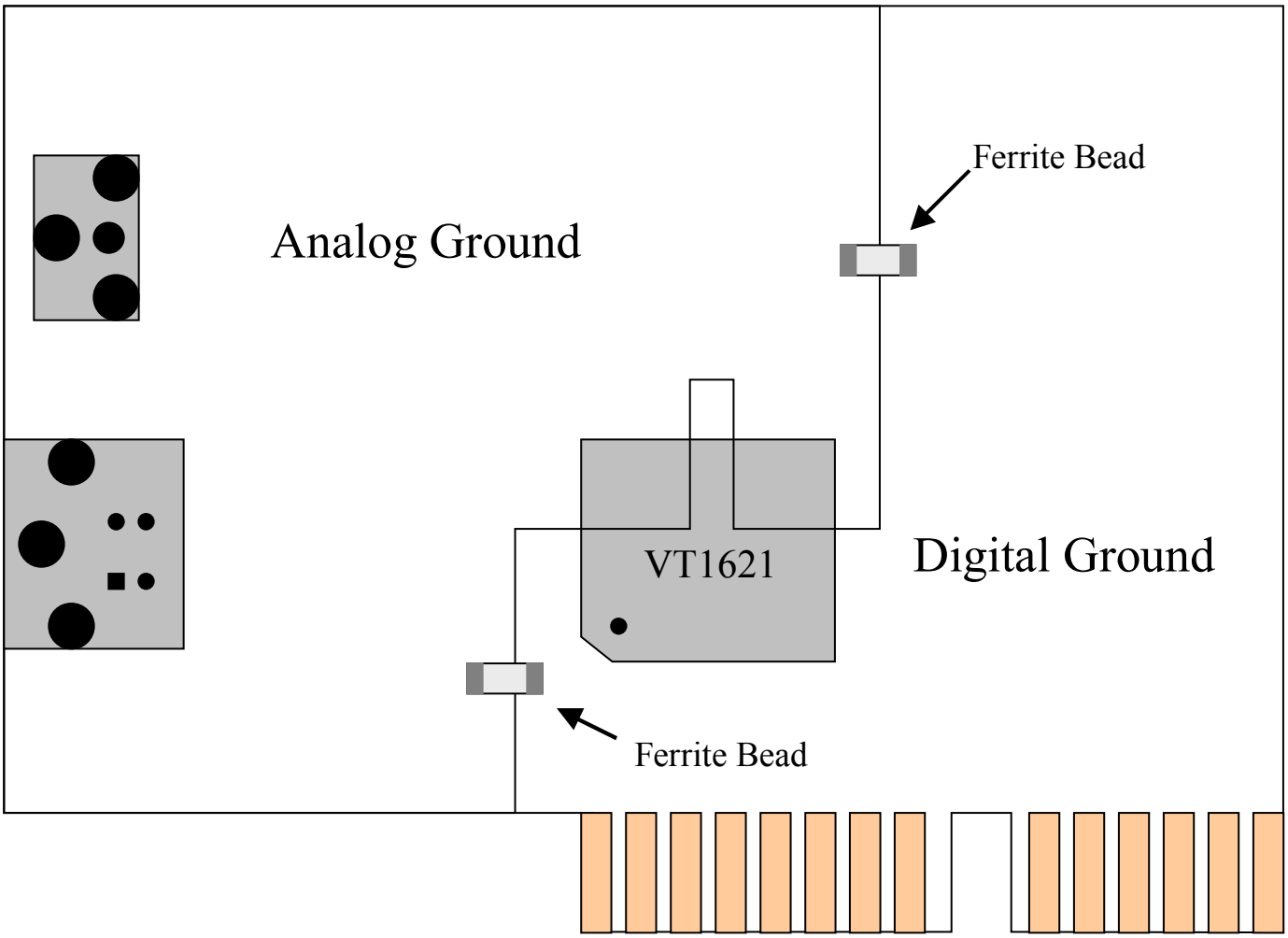


Figure 21. Ground Plane with 4 Layer PCB

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Unit
T_{STG}	Storage Temperature	–55		125	ºC
T_C	Case Operating Temperature	0		55	ºC
V_I	Input Voltage (all digital pins)	GND – 0.5		VCC+0.5	V
V_{ESD}	Electrostatic Discharge (Human Body)			2	kV
T_{VPS}	Vapor Phase Soldering (1 min.)			220	ºC

Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC33	I/O Voltage	2.97	3.3	3.63	V
VCC25	Digital Power Supply Voltage	2.25	2.5	2.75	V
VCCPLL	PLL Power	2.25	2.5	2.75	V
VCCDAC	DAC Power	2.25	2.5	2.75	V
RL	Output load to DAC outputs		37.5		Ω

Power Supply Current and Total Power Consumption Specifications

Symbol	Description	Min	Typ	Max	Unit
I_{D33}	VCC33		10		mA
I_{D25}	VCC25		50		mA
I_{Aall}	VCCDAC + VCCPLL (concurrent. Composite & S-Video)		150		mA
I_{ASV}	VCCDAC + VCCPLL (S-Video only)		120		mA
I_{AComp}	VCCDAC + VCCPLL (Composite only)		80		mA
P_{Tot}	Total Power Consumption		533		mW

Note: (Operating Conditions: TC = 25ºC, RSET = 4.87kΩ)

DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Condition
VCC33	I/O voltage	3.0		3.6	V	Normal op.
V_{IL}	Input low voltage	–0.5		0.3 VCC	V	non 5V tolerant
V_{IH}	Input high voltage	0.7 VCC		1.05 VCC	V	non 5V tolerant
V_{IH5T}	Input high voltage	0.7 VCC		5.5 V	V	5V tolerant
V_{OL}	Output low voltage	-		0.1 VCC	V	I_{OL}= 3.2mA
V_{OH}	Output high voltage	0.7 VCC		-	V	I_{OH}= -200mA
I_{OZ}	Input leakage	–10		10	mA	$0 < V_{IN} < VCC$
C_{IN}	Input capacitance	-		10	pF	
C_{OUT}	Output capacitance	-		10	pF	

DAC DC Characteristics

Parameter	Min	Typ	Max	Unit
Frequency		50		MHz
Output Delay			14	ns
Output Rising Time		10		ns
Output Falling Time		10		ns
Output Settling Time		20		ns
Glitch Energy, DAC step settling within ± 1LSB		75		pV*s
PSRR		45		dB
DAC to DAC Crosstalk		TBD		dB
DAC Matching		TBD		%

Note: (VDDA2=2.5V; RL=37.5Ω; RSET=4.87kΩ; Temp=60°C, unless otherwise noted)

DAC AC Characteristics

Parameter	Min	Typ	Max	Units
Frequency		50		MHz
Output Delay			14	ns
Output Rising Time		10		ns
Output Falling Time		10		ns
Output Settling Time		20		ns
Glitch Energy, DAC step settling within ± 1LSB		75		pV*s
PSRR		45		dB
DAC to DAC Crosstalk		TBD		dB
DAC Matching		TBD		%

Note: (VDDA2=2.5V; RL=37.5Ω; RSET=4.87kΩ; Temp=60°C, unless otherwise noted)

Display Signal Characteristics

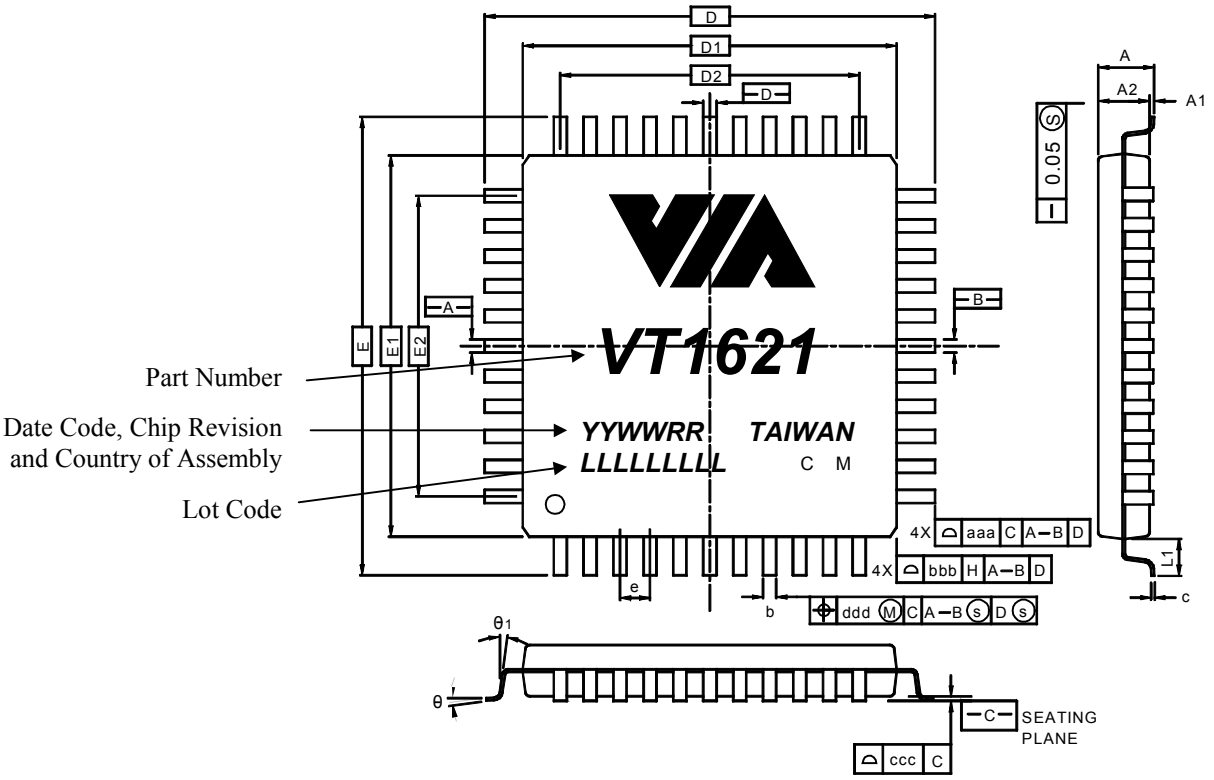
Parameters	Min	Typ	Max	Unit
Pixel Clock Width	10		25	ns
Horizontal Sync Width	1			tp
Setup time from Pixel Data to Pixel Clock	3		17	ns
Hold time from Pixel Clock to Pixel Data	2			ns

PLL Characteristics

Operating Conditions	Min	Typ	Max	Unit
Power Supply	2.25		2.75	V
Clock Output Duty Cycle	45		55	%

Note: Crystal Spec: 14.31818MHz (± 50 ppm)

PACKAGE MECHANICAL SPECIFICATIONS



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	12.00 BSC.			0.472 BSC.		
D1	10.00 BSC.			0.393 BSC.		
E	12.00 BSC.			0.472 BSC.		
E1	10.00 BSC.			0.393 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0	3.5	7	0	3.5	7
θ1	0	—	—	0	—	—
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.22	0.30	0.38	0.009	0.012	0.015
e	0.80 BSC.			0.031 BSC.		
D2	8.00			0.315		
E2	8.00			0.315		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.10			0.004		
ddd	0.20			0.008		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm AND 0.5mm PITCH PACKAGES.

3. DIMENSION "b" DIFFERENT FROM JEDEC SPEC:
   ASE: 0.22 / 0.30 / 0.38
   JEDEC: 0.30 / 0.37 / 0.45

Figure 22. Mechanical Specification – 44-Pin TQFP Thin Quad Flat Pack