

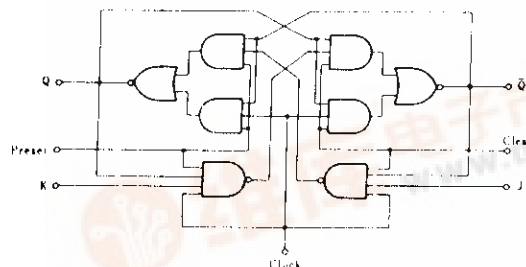
HD74LS112

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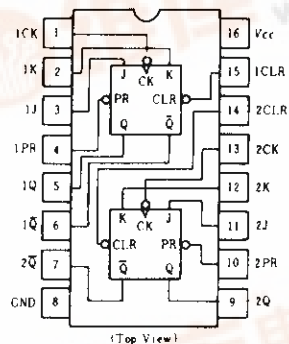
捷多邦, 专业PCB打样工厂, 24小时加急出货

Dual J-K Negative-edge-triggered Flip-Flops (with Preset and Clear)

BLOCK DIAGRAM(1/2)



PIN ARRANGEMENT



RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|-----------------|------------------|-----------|-----|-----|------|
| Clock frequency | f_{clock} | 0 | — | 30 | MHz |
| Pulse width | Clock High | t_{wH} | 20 | — | ns |
| | Clear Preset Low | t_{wL} | 25 | — | ns |
| Setup time | "H" Data | t_{suH} | 20 | — | ns |
| | "L" Data | t_{suL} | 20 | — | ns |
| Hold time | t_h | 0 | — | — | ns |

Note) ↓; The arrow indicates the falling edge.

FUNCTION TABLE

| Inputs | | | | | Outputs | |
|--------|-------|-------|---|---|----------------|-----------------|
| Preset | Clear | Clock | J | K | Q | Q̄ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H* | H* |
| H | H | ↓ | L | L | Q ₀ | Q̄ ₀ |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | Toggle | |
| H | H | H | X | X | Q ₀ | Q̄ ₀ |

Notes) H; high level, L; low level, X; irrelevant

↓; transition from high to low level

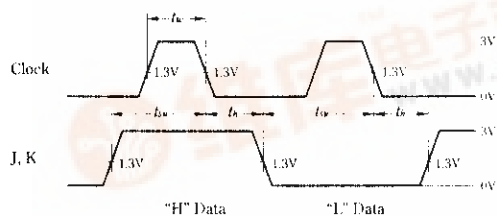
Q₀; level of Q before the indicated steady-state input conditions were established.

Q̄₀; complement of Q₀ or level of Q̄ before the indicated steady-state input conditions were established.

Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.

*; This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

TIMING DEFINITION



"H" Data

"L" Data



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■ ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

| Item | | Symbol | Test Conditions | min | typ* | max | Unit |
|------------------------------|--------|---------------|---|-----|------|------|---------------|
| Input voltage | | V_{IH} | | 2.0 | — | — | V |
| | | V_{IL} | | — | — | 0.8 | V |
| Output voltage | | V_{OH} | $V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}, I_{OH}=-400\mu\text{A}$ | 2.7 | — | — | V |
| | | V_{OL} | $V_{CC}=4.75\text{V}, V_{IH}=2\text{V}$ | — | — | 0.5 | V |
| | | | $V_{IL}=0.8\text{V}$ | — | — | 0.4 | |
| Input current | J, K | I_{IH} | $V_{CC}=5.25\text{V}, V_I=2.7\text{V}$ | — | — | 20 | μA |
| | Clear | | | — | — | 60 | |
| | Preset | | | — | — | 60 | |
| | Clock | | | — | — | 80 | |
| | J, K | I_{IL}^{**} | $V_{CC}=5.25\text{V}, V_I=0.4\text{V}$ | — | — | -0.4 | mA |
| | Clear | | | — | — | -0.8 | |
| | Preset | | | — | — | -0.8 | |
| | Clock | | | — | — | -0.8 | |
| | J, K | I_I | $V_{CC}=5.25\text{V}, V_I=7\text{V}$ | — | — | 0.1 | mA |
| | Clear | | | — | — | 0.3 | |
| | Preset | | | — | — | 0.3 | |
| | Clock | | | — | — | 0.4 | |
| Short-circuit output current | | I_{OS} | $V_{CC}=5.25\text{V}$ | -20 | — | -100 | mA |
| Supply current *** | | I_{CC} | $V_{CC}=5.25\text{V}$ | — | 4 | 8 | mA |
| Input clamp voltage | | V_{IK} | $V_{CC}=4.75\text{V}, I_{IN}=-18\text{mA}$ | — | — | -1.5 | V |

* $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$

** I_{IL} should not be measured when preset and clear inputs are low at same time.

*** With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn.
At the time of measurement, the clock input is grounded.

■ SWITCHING CHARACTERISTICS ($V_{CC}=5\text{V}, T_a=25^\circ\text{C}$)

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|-------------------------|-----------|--------------------------|--------------|--|-----|-----|-----|------|
| Maximum clock frequency | f_{max} | | | $C_L=15\text{pF}, R_L=2\text{k}\Omega$ | 30 | 45 | — | MHz |
| Propagation delay time | t_{PLH} | Clear Preset Clock | Q, \bar{Q} | | — | 11 | 20 | ns |
| | t_{PHL} | | | | — | 15 | 30 | ns |

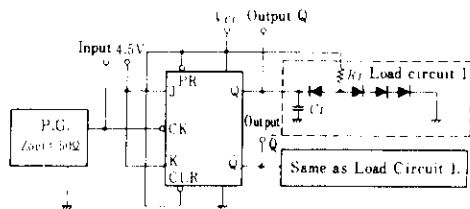


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■ TESTING METHOD

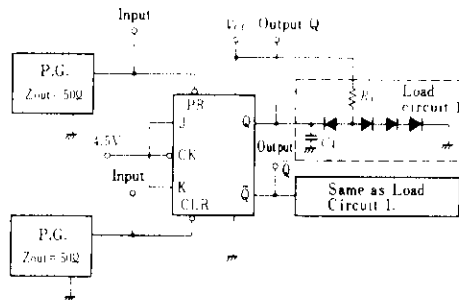
1) Test Circuit

1.1) f_{max} , t_{PLH} , t_{PHL} (Clock \rightarrow Q, \bar{Q})



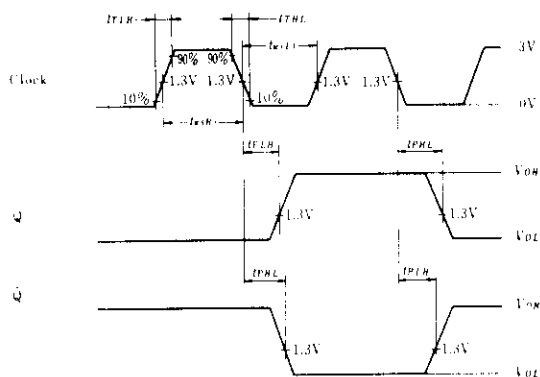
- Notes)
1. Test is put into the each flip-flop.
 2. All diodes are 1S2074 \oplus .
 3. C_L includes probe and jig capacitance.

1.2) t_{PHL} , t_{PLH} (Clear, Preset \rightarrow Q, \bar{Q})

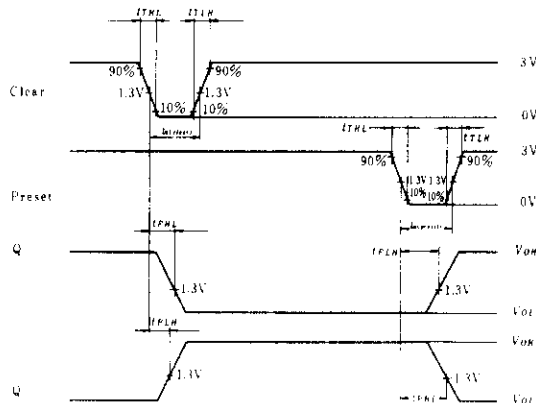


- Notes)
1. Test is put into the each flip-flop.
 2. All diodes are 1S2074 \oplus .
 3. C_L includes probe and jig capacitance.

Waveform

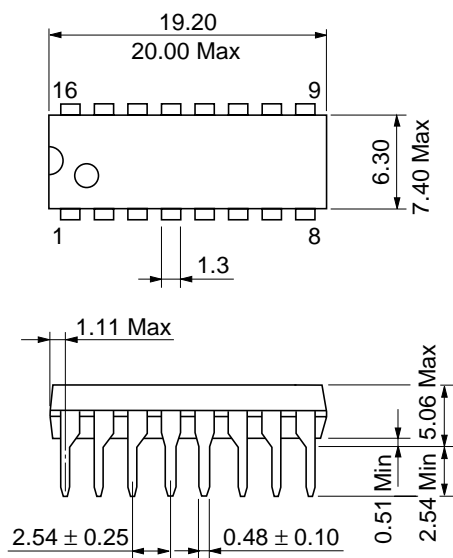


- Note) Clock input pulse; $t_{RLH} \leq 15\text{ns}$, $t_{FHL} \leq 6\text{ns}$, $PRR=1\text{MHz}$, duty cycle=50% and; for f_{max} , $t_{PLH}=t_{PHL} \leq 2.5\text{ns}$.

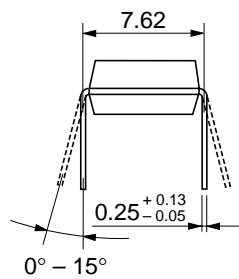
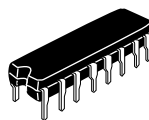


- Note) Clear and preset input pulse; $t_{RLH} \leq 15\text{ns}$, $t_{FHL} \leq 6\text{ns}$, $PRR=1\text{MHz}$

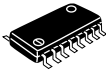
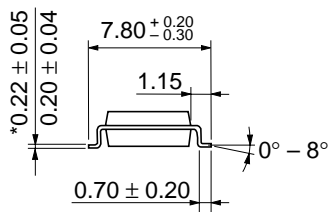
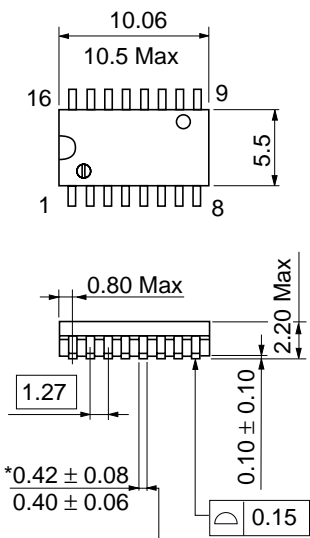




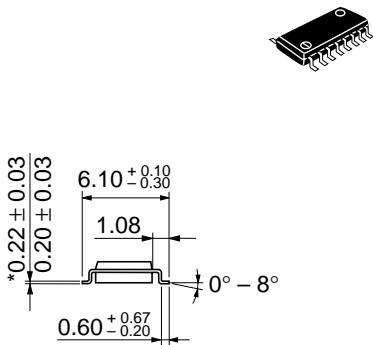
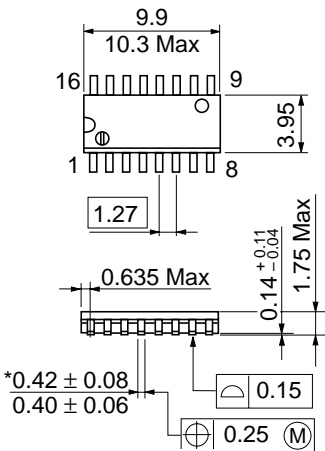
Unit: mm



Unit: mm



Unit: mm



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