Am2950-50A/Am2951-51A

Eight-Bit Bidirectional I/O Ports with Handshake

DISTINCTIVE CHARACTERISTICS

- **Eight-Bit, Bidirectional I/O Port with Handshake**– Two eight-bit, back-to-back registers store data moving in both directions between two bidirectional busses.
- **Register Full/Empty Flags**– On-chip flag flip-flops provide data transfer handshaking signals.
- **24mA Output Current Sink Capability.**
- **Separate Clock, Clock Enable and Three-State Output Enable for Each Register.**
- **Separate, Edge-Sensitive Clear Control for Each Flag Flip-Flop.**
- **Fast** – The Am2950A and Am2951A will be 25–30% faster than the Am2950 and Am2951.

GENERAL DESCRIPTION

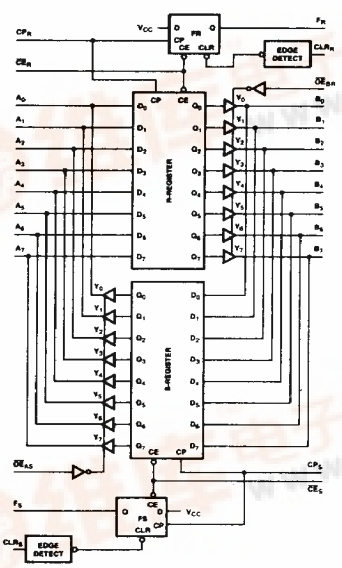
The Am2950 and Am2951, members of Advanced Micro Devices' Am2900 Family, are designed for use as parallel data I/O ports. Two eight-bit, back-to-back registers store data moving in both directions between two bidirectional, 3-state busses. On chip flag flip-flops, set automatically when a register is loaded, provide the handshaking signals required for demand-response data transfer.

Considerable flexibility is designed into the Am2950/Am2951. Separate clock, Clock Enable and Three-State Output Enable signals are provided for each register, and edge-sensitive clear inputs are provided for each flag flip-flop. A number of these circuits can be used for wider I/O ports. Both inverting and non-inverting versions are available.

24mA output current sink capability, sufficient for most three-state busses, is provided by the Am2950/Am2951.

The Am2950A and Am2951A feature AMD's ion-implanted micro-oxide (IMOX™) processing. They are plug-in replacements for the Am2950 and Am2951 respectively but will be approximately 30% faster.

BLOCK DIAGRAM



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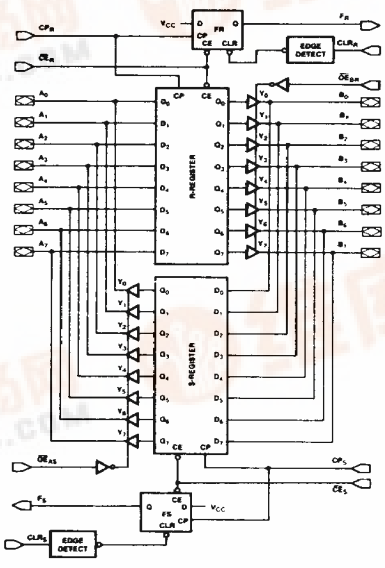

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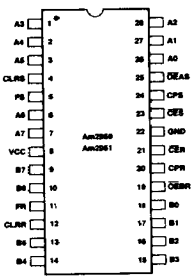
Note: The Am2951 provides inverting data outputs (B_{0-7}).

CONNECTION DIAGRAM
Top View

D-28



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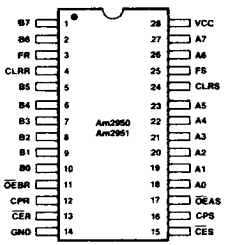

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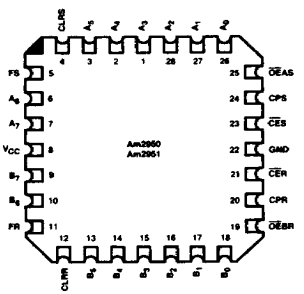
Chip-Pak™ L-28



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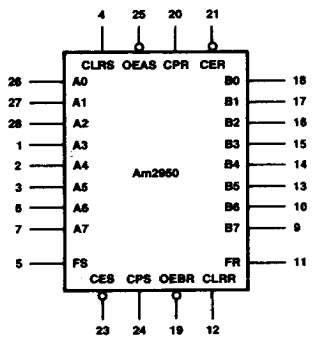
Note: Pin 1 is marked for orientation
Bi is inverted on Am2951.

LOGIC SYMBOL



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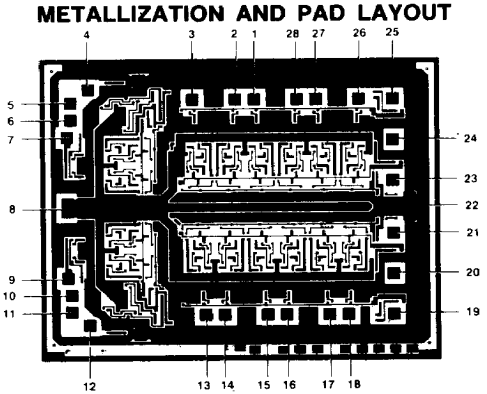
METALLIZATION AND PAD LAYOUT



DIE SIZE 0.107" x 0.138"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2950/50A
Am2951/51A **D** **C** **B**

- B — Screening Option: Blank – Standard processing; B – Burn-in
- C — Temperature (See Operating Range): C – Commercial (0°C to +70°C); M – Military (–55°C to +125°C)
- D — Package: D – 28-pin CERDIP; F – 28-pin flatpak; L – 28-pin leadless chip carrier; X – Dice
- Am2950/50A, Am2951/51A — Device type: 8-Bit Bidirectional I/O Ports

Valid Combinations	
Am2950/50A Am2951/51A	DC, DCB, DMB FMB LC, LMB, XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	A0-7	I/O	Eight bidirectional lines carrying the R Register inputs or S Register outputs.
	B0-7	I/O	Eight bidirectional lines carrying the S Register inputs or B Register outputs.
20	CPR	I	The clock for the R Register and FR Flip-Flop. When $\overline{CER}$ is LOW, data is entered into the R Register and the FR Flip-Flop is set on the LOW-to-HIGH transition of the CPR signal.
21	$\overline{CER}$	I	The Clock Enable for the R Register and FR Flip-Flop. When $\overline{CER}$ is LOW, data is entered into the R Register and the FR Flip-Flop is set on the LOW-to-HIGH transition of the CPR signal. When $\overline{CER}$ is HIGH, The R Register and FR Flip-Flop hold their contents, regardless of CPR signal transitions.
19	$\overline{OEBR}$	I	The Output Enable for the R Register. When $\overline{OEBR}$ is LOW, the R Register three-state outputs are enabled onto the B0-7 lines. When $\overline{OEBR}$ is HIGH, the R Register outputs are in the high-impedance state.
11	FR	O	The FR Flip-Flop output.
12	CLRR	I	The clear control for the FR Flip-Flop. The FR Flip-Flop is cleared on the LOW-to-HIGH transition of CLRR signal.
24	CPS	I	The clock for the S Register and FS Flip-Flop. When $\overline{CES}$ is LOW, data is entered into the S Register and the FS Flip-Flop is set on the LOW-to-HIGH transition of the CPS signal.
23	$\overline{CES}$	I	The clock enable for the S Register and FS Flip-Flop. When $\overline{CES}$ is LOW, data is entered into the S Register and the FS Flip-Flop is set on the LOW-to-HIGH transition of the CPS signal. When $\overline{CES}$ is HIGH, the S Register and FS Flip-Flop hold their contents, regardless of CPS signal transitions.
25	$\overline{OEAS}$	I	The output enable for the S Register. When $\overline{OEAS}$ is LOW, the S Register three-state outputs are enabled onto the A0-7 lines. When $\overline{OEAS}$ is HIGH, the S Register outputs are in the high-impedance state.
5	FS	O	The FS Flip-Flop output.
4	CLRS	I	The clear control for the FS Flip-Flop. The FS Flip-Flop is cleared on the LOW-to-HIGH transition of CLRS signal.

REGISTER FUNCTION TABLE (Applies to R or S Register)

Inputs			Internal	
D	CP	$\overline{CE}$	Q	Function
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	

OUTPUT CONTROL

$\overline{OE}$	Internal Q	Y-Outputs		Function
		Am2950	Am2951	
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

FLAG FLIP-FLOP FUNCTION TABLE (Applies to R or S Flag Flip-Flop)

Inputs			F-Output	Function
$\overline{CE}$	CP	CLR		
H	X	‡	NC	Hold Flag
X	X	↑	L	Clear Flag
L	↑	‡	H	Set Flag

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance

NC = NO CHANGE
↑ = LOW-to-HIGH Transition
‡ = NO LOW-to-HIGH Transition

APPLICATIONS

The Am2950/Am2951 provides data transfer handshaking signals as well as eight-bit, bidirectional data storage. Its flexibility allows it to be used in any type of computer system, including Am2900, 8080, 8085, 8086, Z80, and Z8000 systems.

Figure 1 shows an Am2950 used to store data moving in both directions between a bidirectional system data bus and a bidirectional peripheral data bus. The on-chip Flag flip-flops provide the data in, data out handshaking signals required for data transfer and interrupt request generation.

Figure 2 shows a multiple I/O port system using Am2950's. Two Am2950's are used at each port to interface the 16-bit system data bus. The Am2950 flags are used to generate I/O interrupt requests.

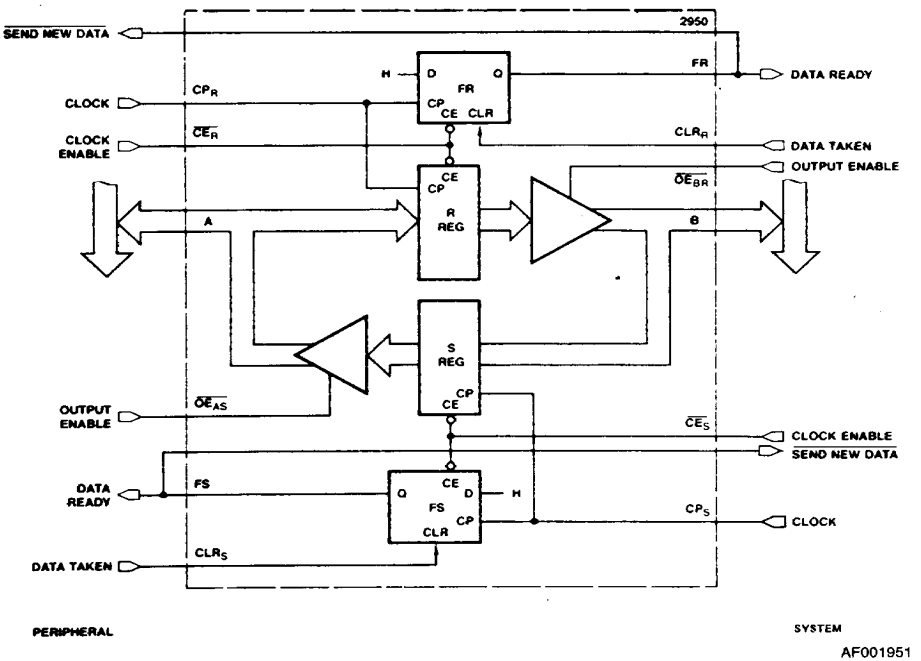


Figure 1. A Bidirectional I/O Port with Handshaking Using the Am2950.

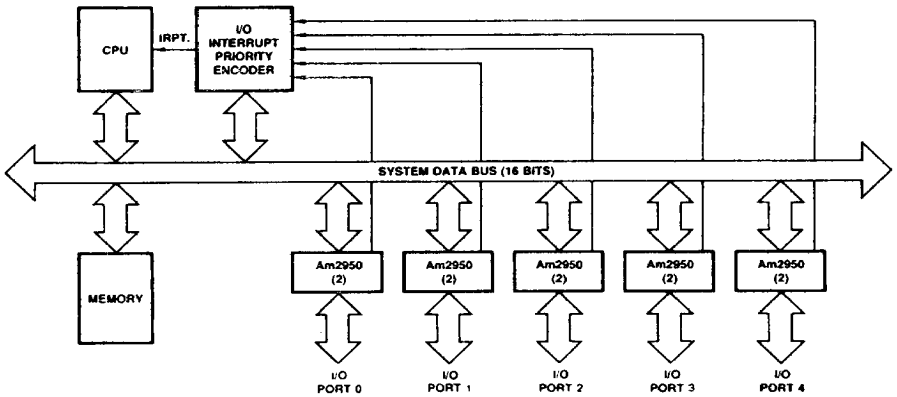


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Figure 2. Multiple I/O Port System.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

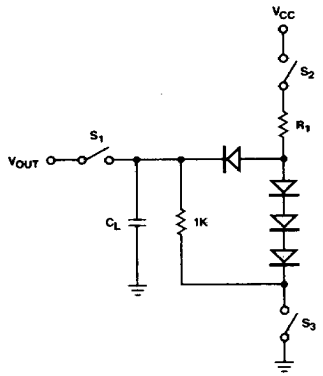
Am2950/Am2951

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	FR, FS	I_{OH} = −1mA	2.4	3.4		Volts
			A_{0-7}, B_{0-7}	MIL, I_{OH} = −2mA	2.4	3.4		
				COM'L, I_{OH} = −6.5mA	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	FR,FS	I_{OL} = 12mA			0.5	Volts
			A_{0-7}, B_{0-7}	MIL I_{OL} = 16mA			0.5	
				COM'L, I_{OL} = 2.4mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V		A_{0-7}, B_{0-7}			−250	μA
				CLRR,CLRS			−2.0	mA
				Others			−360	μA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		A_{0-7}, B_{0-7}			70	μA
				CLRR, CLRS			100	
				Others			20	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_O	Output Off-state Leakage Current	V_{CC} = MAX	A_{0-7}, B_{0-7}	V_O = 2.4V			70	μA
				V_O = 0.4V			−250	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−30		−85	mA
I_{CC}	Power Supply Current (Notes 4,5)	V_{CC} = MAX	COM'L	T_A = 0°C to +70°C			275	mA
				T_A = +70°C			228	
			MIL	T_C = −55°C to +125°C			309	
				T_C = +125°C			202	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is measured with all inputs at 4.5V and all outputs open.
5. Worst case I_{CC} is at minimum temperature.

SWITCHING TEST CIRCUIT

A. THREE-STATE OUTPUTS



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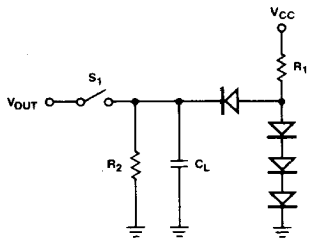
B. NORMAL OUTPUTS



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$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{1K}}$$

$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{R_2}}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2950/2951 (DIP)

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
–	A_{0-7}	A	220	1K
–	B_{0-7}	A	220	1K
5	FS	B	300	2.4K
11	FR	B	300	2.4K

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current when the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5–8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0V$ and $V_{IH} \geqslant 3.0V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

Am2950A/Am2951A SWITCHING CHARACTERISTICS

The tables below define the Am2950A/Am2951A switching characteristics. Tables A are setup and hold times relative to a clock LOW-to-HIGH transition. Tables B are propagational delays. Tables C are recovery times. Tables D are pulse-width requirements. Tables E are enable/disable times. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with RL on Ai and Bi = 220Ω and RL on FS and FR = 300Ω. CL = 50pF except output disable times which are specified at CL = 5pF.

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, C_L = 50pF)

A. Set-up and Hold Times.

Input	With Respect To	ts	th
A0-7	CPR ↓		
B0-7	CPS ↓		
$\overline{CES}$	CPS ↓		
$\overline{CER}$	CPR ↓		

B. Propagation Delays

Input	A0-7	B0-7	FS	FR
CPS ↓				
CPR ↓				
CLRS ↓				
CLRR ↓				

C. Recovery Times

From	To	tREC
CLRS ↓	CPS ↓	
CLRR ↓	CPR ↓	

D. Pulse-Width Requirements

Input	Min LOW Pulse Width	Min HIGH Pulse Width
CPS		
CPR		
CLRS		
CLRR		

E. Enable/Disable Times

From	To	Disable	Enable
$\overline{OEAS}$	A0-7		
$\overline{OEBR}$	B0-7		

GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

(T_C = −55 to +125°C, V_{CC} = 4.5 to 5.5V, C_L = 50pF)

A. Set-up and Hold Times.

Input	With Respect To	ts	th
A0-7	CPR ↓		
B0-7	CPS ↓		
$\overline{CES}$	CPS ↓		
$\overline{CER}$	CPR ↓		

B. Propagation Delays

Input	A0-7	B0-7	FS	FR
CPS ↓				
CPR ↓				
CLRS ↓				
CLRR ↓				

C. Recovery Times

From	To	tREC
CLRS ⌐¯	CPS ⌐¯	
CLRR ⌐¯	CPR ⌐¯	

D. Pulse-Width Requirements

Input	Min LOW Pulse Width	Min HIGH Pulse Width
CPS		
CPR		
CLRS		
CLRR		

E. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}$AS	A0-7		
$\overline{OE}$BR	B0-7		

Am2950/Am2951 SWITCHING CHARACTERISTICS

The tables below define the Am2950/Am2951 switching characteristics. Tables A are set-up and hold times relative to a clock LOW-to-HIGH transition. Tables B are propagational delays. Tables C are recovery times. Tables D are pulse-width requirements. Tables E are enable/disable times. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with RL on Ai and Bi = 220Ω and RL on FS and FR = 300Ω. CL = 50pF except output disable times which are specified at CL = 5pF.

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, C_L = 50pF)

A. Set-up and Hold Times.

Input	With Respect To	ts	th
A0-7	CPR ⌐¯	7	5
B0-7	CPS ⌐¯	7	5
$\overline{CE}$S	CPS ⌐¯	*19/15	4
$\overline{CE}$R	CPR ⌐¯	*19/15	4

B. Propagation Delays

Input	A0-7	B0-7	FS	FR
CPS ⌐¯	*30/26	–	20	–
CPR ⌐¯	–	*30/26	–	20
CLRS ⌐¯	–	–	22	–
CLRR ⌐¯	–	–	–	22

C. Recovery Times

From	To	tREC
CLRS ⌐¯	CPS ⌐¯	31
CLRR ⌐¯	CPR ⌐¯	31

D. Pulse-Width Requirements

Input	Min LOW Pulse Width	Min HIGH Pulse Width
CPS	20	20
CPR	20	20
CLRS	20	20
CLRR	20	20

E. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}$AS	A0-7	22	27
$\overline{OE}$BR	B0-7	22	27

*Where two numbers appear, the first is the Am2950 spec, the second is the Am2951 spec.

GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

(T_C = −55 to +125°C, V_{CC} = 4.5 to 5.5V, C_L = 50pF)

A. Set-up and Hold Times.

Input	With Respect To	ts	th
A0-7	CPR ↓	11	8
B0-7	CPS ↓	11	8
$\overline{CES}$	CPS ↓	*20/15	4
$\overline{CER}$	CPR ↓	*20/15	4

B. Propagation Delays

Input	A0-7	B0-7	FS	FR
CPS ↓	*35/28	–	20	–
CPR ↓	–	*35/28	–	20
CLRS ↓	–	–	22	–
CLRR ↓	–	–	–	22

C. Recovery Times

From	To	tREC
CLRS ↓	CPS ↓	34
CLRR ↓	CPR ↓	34

D. Pulse-Width Requirements

Input	Min LOW Pulse Width	Min HIGH Pulse Width
CPS	20	20
CPR	20	20
CLRS	20	20
CLRR	20	20

E. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}$AS	A0-7	24	28
$\overline{OE}$BR	B0-7	24	28

*Where two numbers appear, the first is the Am2950 spec, the second is the Am2951 spec.