



VC0702

TV Camera Processors

Datasheet

Preliminary

Version 0.99

April 20, 2006

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1. GENERAL DESCRIPTION

VC0702 is a high performance video camera device designed for applications that requiring small package, low voltage, low power consumption. It supports various video outputs, such as interlaced/progressive PAL/NTSC composite video output, RGB/YCbCr component video output, and S-Video output. The devices use VC0702 can directly link with a VCR, TV monitor or other A/V device.

VC0702 can be designed in applications, such as security, surveillance, video conference, video phone, vision-enabled toys, digital camcorder, and medical equipment. It works in a low voltage and low power consumption environment and requires only a single 3.3 V DC power supply. VC0702 has motion detection and trigger function which targets to automatic surveillance applications.

VC0702 has two different variations as listed in the below table. They have the same functionalities, but the packages are different.

| PRODUCT NUMBER | PACKAGE |
|----------------|-------------|
| VC0702PLSB | 48-Pin LQFP |
| VC0702NJSB | 40-Pin QFN |

2. KEY PARAMETERS

| PARAMETERS | VALUES | UNIT |
|-------------------------|---|-------|
| Sensor Type Supported | VGA/CIF CMOS and CCD | |
| NTSC output | 720 x 480 | Pixel |
| PAL output | 720 x 576 | Pixel |
| Maximum Frame Rate | 30 (@ 27MHz in NTSC) 25 (@ 27MHz in PAL) | fps |
| Crystal input Frequency | 6.0 | MHz |
| Power Supply | 3.3 | V |
| Operating Temperature | -40 ~ +85 | °C |
| Package | VC0702NJSB (40-pin QFN) VC0702PLSB (48-pin LQFP) | |

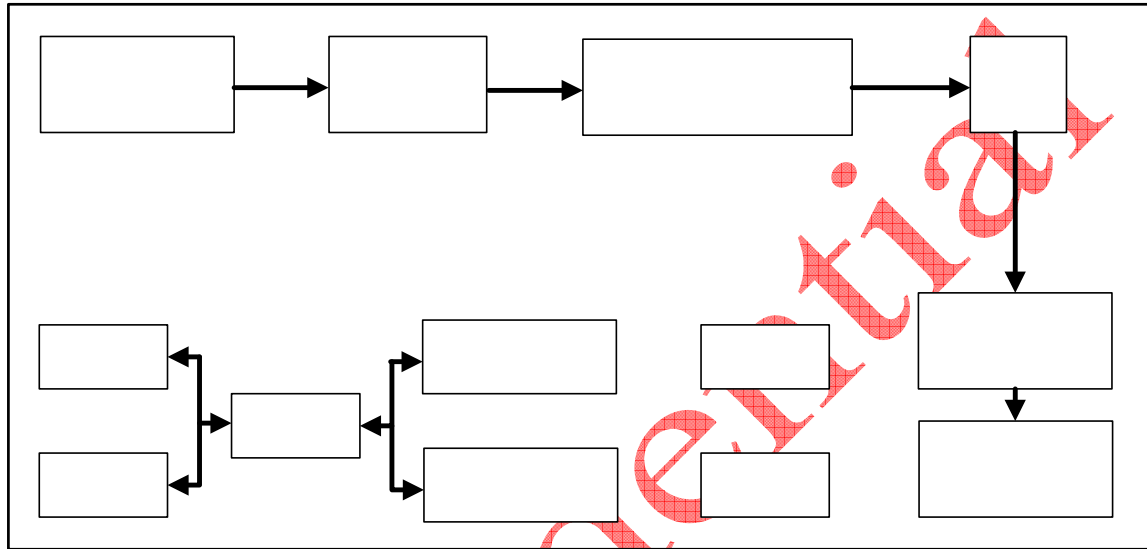
3. GENERAL FEATURE

- ✓ Support CIF/VGA sensors
- ✓ Support Color or BW CMOS and CCD sensors
- ✓ Build-in 8-bit MCU
- ✓ Video Out
 - ✧ Composite video: NTSC or PAL
 - ✧ Component Video: RGB or YCbCr (VC0702PLSB only)
 - ✧ S-Video (VC0702PLSB only)
 - ✧ Scan mode: interlaced and progressive
 - ✧ External field sync.
- ✓ GPIO support typical control function
 - ✧ Motion detection alarm output
 - ✧ Color/BW manual conversion switch control
 - ✧ Infrared LED control output
- ✓ Image Pipeline
 - ✧ 10-bit width accuracy in color processing
 - ✧ On-chip color bar generator for testing
 - ✧ Auto Exposure (AE)
 - ✧ Auto White Balance (AWB)
 - ✧ Auto Gain Control (AGC)
 - ✧ Auto bad pixel detection and cancellation
 - ✧ Auto flicker detection and cancellation
 - ✧ Auto lens shading compensation
 - ✧ Configurable image noise reduction
 - ✧ Configurable image sharpness enhancement
 - ✧ Configurable gamma and color correction
 - ✧ Configurable brightness, color saturation, and hue
 - ✧ Edge-adaptive CFA interpolation
 - ✧ Up to 16 windows for statistical collection, exposure
 - ✧ Color/BW video image auto/manual conversion
 - ✧ Up to 16-window auto motion detection supply
 - ✧ Auto frame rate conversion
 - ✧ Build-in IPP for image size conversion
 - ✧ Built-in 3-ch 10-bit generic video DACs
- ✓ One input clock: 6MHz crystal
- ✓ Others:
 - ✧ EEPROM configurable
 - ✧ UART controllable
- ✓ Power management
 - ✧ Normal mode
 - ✧ Low power mode

4. CHIP BLOCK DIAGRAM

VC0702 integrates image processor, frame rate control unit, image post-processor, TV encoder, VIDEO DAC and 8051 compatible MCU with built-in code-ROM/data-RAM.

Chip registers can be programmed through EEPROM or serial bus. Multiple GPIO channels support typical control functions.



Sensor I/F

ISP

Interrupt

MCU
Program R

MCU

5. PIN ASSIGNMENT

5.1. Type Definitions

| SYMBOL | DESCRIPTIONS | NOTE |
|--------|------------------------------|------------------------------|
| I | Input | |
| O | Output | |
| I/O | Bidirectional (Input/Output) | |
| P | Power | VDD, VDDA, |
| G | Ground | VSS, VSSA |
| PD | Pull Down | |
| PU | Pull Up | |
| A | Analog links | To a resistor, capacity etc. |

5.2. PIN Definitions

| PIN NUMBER | | NAME | TYPE | DESCRIPTION |
|------------|------------|------------|---------|--------------------------------|
| VC0702NJSB | VC0702PLSB | | | |
| - | 1 | GPIO8 | I/O | GPIO 8 |
| 10 | 2 | GPIO2 | I/O | GPIO 2 |
| 11 | 3 | CS_PWDN | O, PD | CMOS Sensor Power Down Control |
| | | SIF_EDGE | I | Hardware strap pin: SIF_EDGE |
| 12 | 4 | CS_RST | I/O, PD | Sensor Reset Output |
| | | TST_SEL_I2 | I/O | Test Mode Select In Bit 2 |
| | | PAL_MOD | I/O | Hardware strap pin. |
| 13 | 5 | CS_D7 | I, PD | Sensor data input 7 |
| 14 | 6 | CS_D6 | I, PD | Sensor data input 6 |
| 15 | 7 | CS_D5 | I, PD | Sensor data input 5 |
| 16 | 8 | CS_HSYNC | I, PD | Sensor Horizontal sync input |
| 17 | 9 | CS_D4 | I, PD | Sensor data input 4 |

| PIN NUMBER | | | | |
|------------|----|-----------|---------|---|
| 18 | 10 | CS_D3 | I, PD | Sensor data input 3 |
| 19 | 11 | CS_D2 | I, PD | Sensor data input 2 |
| 20 | 12 | CS_VSYNC | I, PD | Sensor vertical sync input |
| - | 13 | GPIO7 | I/O, PD | GPIO 7 |
| | | PRG_MOD | | Hardware strap pin: PRGMOD |
| 21 | 14 | CS_D1 | I/O, PD | Sensor data input bit 1 |
| | | EEP_SCK | O | EEPROM I2C master SCK output |
| 22 | 15 | CS_D0 | I/O | CMOS Sensor data input 0 |
| | | EEP_SDA | I/O | EEPROM I2C master SDA in and out |
| - | 16 | GPIO6 | I/O, PD | GPIO 6 |
| | | CPON_MOD | | Hardware strap pin: CPON_MOD |
| - | 17 | GPIO5 | I/O, PD | GPIO 5 |
| | | TV_HSYNC | O | TV encoder HSYNC output |
| | | RGB_MOD | I | Hardware strap pin: RGB_MOD |
| 23 | 18 | CLK_IN | I | Crystal input |
| 24 | 19 | CLK_OUT | O | Crystal output (loopback) |
| 25 | 20 | VDD_IO | P | Digital IO Power 3.3V |
| 26 | 21 | PR_CAP1 | A | PR' s external CAP connector (10nF) |
| 27 | 22 | VSS | P | Digital core/IO ground |
| 28 | 23 | VDDA_PR | P | Analog Power Supply 3.3V for Internal Power Regulator (LDO) |
| 29 | 24 | PR_CAP2 | A | PR' s external CAP connector (4.7uf) |
| 30 | 25 | VSSA_PLL | P | PLL Analog ground |
| 31 | 26 | VDDA_PLL | P | PLL Analog power |
| - | 27 | DAC_C | A, O | C/Cr/R channel signal analog output |
| - | 28 | VDDA_C | P | C/Cr/R channel analog power (3.3V) |
| - | 29 | DAC_Y | A, O | Y/Y/G channel signal analog output |
| - | 30 | VDDA_Y | P | Y/Y/G channel analog power(3.3V) |
| 32 | 31 | DAC_CVBS | A,O | CVBS/Cb/B channel signal analog output |
| 33 | 32 | VDDA_CVBS | P | CVBS/Cb/B channel analog power (3.3V) |

| PIN NUMBER | | | | |
|------------|----|------------|--------------|--|
| 34 | 33 | DAC_REXT | A | DAC external resistor pin |
| 35 | 34 | DAC_COMP | A | DAC Compensation pin |
| 36 | 35 | VSSA_DAC | P | DAC analog ground |
| 37 | 36 | VDDA_DAC | P | DAC analog Power (3.3V) |
| 38 | 37 | RSTN | I, PU | Power on reset |
| 39 | 38 | TEST | I, PD | Manufacture test mode, should be connected to 0 in normal mode |
| 40 | 39 | GPIO4 | I/O | GPIO 4: |
| | | TV_VSYNC_O | O | TV Vertical SYNC Output |
| | | TV_CSYNC_O | O | TV Composite SYNC Output |
| | | ESYNC_MOD | I/O | Hardware strap pin |
| 1 | 40 | GPIO3 | I/O | GPIO 3 |
| | | TV_VSYNC_I | I | TV VSYNC Input |
| | | TV_CSYNC_I | I | TV CSYNC Input |
| 2 | 41 | GPIO1 | I/O | GPIO 1 |
| | | UART_IN | I | UART Input |
| | | TST_SEL_I1 | I | Test Mode Select in Bit 1 |
| 3 | 42 | GPIO0 | I/O, PD | GPIO 0 |
| | | UART_OUT | O | UART Output |
| | | TST_SEL_I0 | I | Test Mode Select in Bit 0 |
| | | E2_MOD | I | Hardware strap pin |
| 4 | 43 | CS_SCK | I/O, PD | Sensor I2C bus SCK output |
| | | TST_SEL_I3 | I | Test Mode Select In Bit3 |
| | | CVBS_MOD | I | Hardware strap pin |
| 5 | 44 | CS_SDA | I/O, Schmitt | Sensor I2C bus SDA pin |
| 6 | 45 | CS_CLK | I/O, PD | Sensor CLK output |
| | | UM_MOD | I | Reserved |
| 7 | 46 | CS_ENBN | I/O, PD | Sensor enable pin, Output |
| | | E2_BUS | I/O | Hardware strap pin |
| 8 | 47 | CS_D9 | I, PD | Sensor data input bit 9 |

| PIN NUMBER | | | | |
|------------|----|-------|-------|-------------------------|
| 9 | 48 | CS_D8 | I, PD | Sensor data input bit 8 |

5.3. Hardware Strap Pin Descriptions

VC0702 has hardware strap pins. Those pins are multiplex usage pins. When the VC0702 is reset, the pull-up or pull-down status of these pins will set the configuration of VC0702.

The table below listed the hardware strap pins and their functions,

In the table, 0 means pull-down, 1 means pull-up, the on-chip pull-down resistors will select the default setting if no external resistors used to pull-up the hardware strap pins.

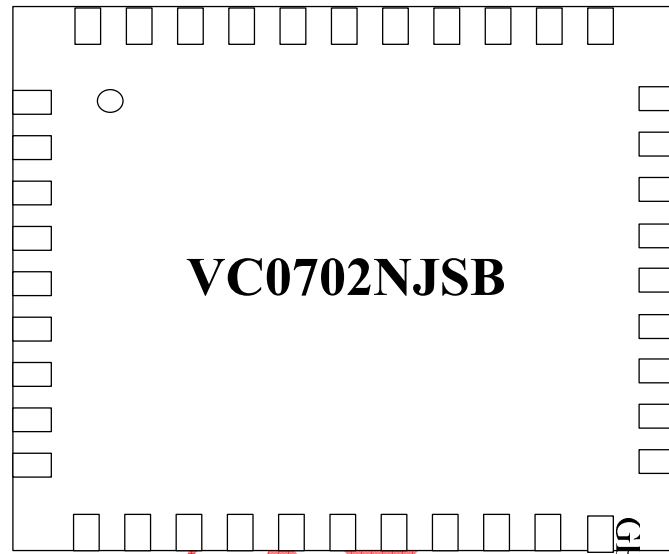
| SIGNAL NAME | DESCRIPTION |
|-------------|---|
| PAL_MOD | Used for the selection of 50Hz output mode or 60Hz output mode 0 (default): 50Hz 1: 60Hz |
| RGB_MOD | Used for the selection of YCbCr or RGB output mode 0(default): YCbCr 1: RGB |
| CPON_MOD | When RGB_MOD select YCbCr, this pin used for the selection of composite or component output mode, when RGB_MOD select RGB, this pin used for the selection of non-bypass or bypass output mode 0(default): composite/non-bypass 1: component/bypass |
| PRG_MOD | Used for the selection of interlaced or progressive output mode 0(default): interlaced 1: progressive |
| CVBS_MOD | Used for the selection of CVBS or S-VIDEO, this pin only valid when composite output mode is selected 0(default): CVBS 1: S-VIDEO |
| EEPRM_MOD | Used for the selection of 8 bit EEPROM or 16 bit EEPROM 0 (default): 8 bit EEPROM 1: 16 bit EEPROM |

| SIGNAL NAME | DESCRIPTION |
|-------------|---|
| EERPM_BUS | Used for the selection of EEPROM I2C bus used pin 0 (default): share Sensor I2C bus 1: occupy Sensor data in [1:0] |
| OROM_MOD | Used for the selection of system will boot from internal ROM or External ROM 0(default): boot from internal ROM 1: boot from external ROM |
| SIF_EDGE | Used for the selection of sensor-interface sample sensor's input clock edge 0(default): use default setting for sampling 1: use reverse edge for sampling |
| ESYNC_MOD | Used for the selection of external sync signal or not 0(default): disable external sync signal 1: enable external sync. Signal |
| UM_MODE | Reserved. |

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6. PIN LAYOUT

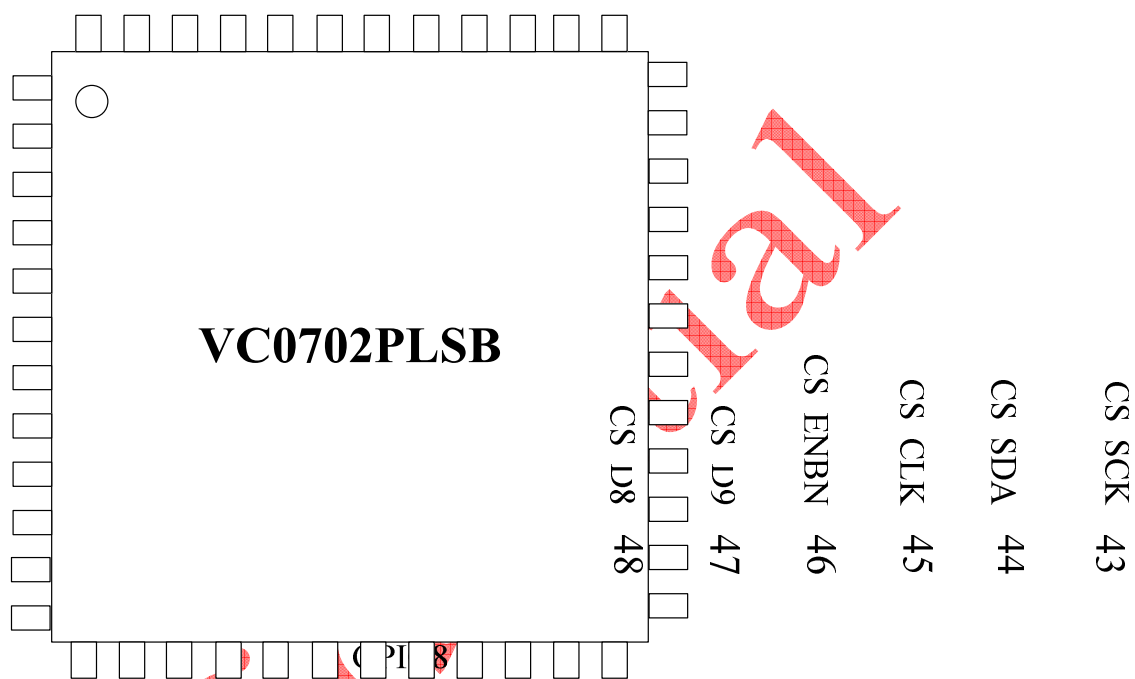
6.1. VC0702NJSB 40-Pin QFN layout



GPIO4 40
TEST 39
RSIN 38
VDDA DAC 37
VSSA DAC 36
DAC COM 35

GPIO3 1
GPIO1 2
GPIO0 3
CS_SCK 4
CS_SDA 5
CS_CLK 6
CS_ENBN 7

6.2. VC0702PLSB 48-Pin LQFP Layout



| | |
|----------|----|
| GPIO2 | 2 |
| CS_PWDN | 3 |
| CS_RST | 4 |
| CS_D7 | 5 |
| CS_D6 | 6 |
| CS_D5 | 7 |
| CS_HSYNC | 8 |
| CS_D4 | 9 |
| CS_D3 | 10 |
| CS_D2 | 11 |
| CS_VSYNC | 12 |

7. OUTPUT MODE

7.1. Output Mode Supported

| MODE | CH 1 | CH 2 | CH 3 | NOTE | FORMAT |
|------|------|------|------|--------------------------|---------|
| 0 | CVBS | Y | C | NTSC | 720x480 |
| 1 | CVBS | Y | C | PAL | 720x576 |
| 2 | Cb | Y | Cr | YCbCr, interlace, 60Hz | 720x480 |
| 3 | Cb | Y | Cr | YCbCr, interlace, 50Hz | 720x576 |
| 4 | B | G | R | RGB, interlace, 60Hz | 720x480 |
| 5 | B | G | R | RGB, interlace, 50Hz | 720x576 |
| 6 | Cb | Y | Cr | YCbCr, progressive, 60Hz | 720x480 |
| 7 | B | G | R | RGB, progressive, 60Hz | 720x480 |
| 8 | Cb | Y | Cr | YCbCr, progressive, 50Hz | 720x576 |
| 9 | B | G | R | RGB, progressive, 50Hz | 720x576 |
| 10 | B | G | R | VGA mode bypass | 640x480 |
| 11 | B | G | R | CIF mode bypass | 352x288 |

7.2. Hardware strap pin Setting on output mode list

| Mode No. | RGB_MOD | CPON_MOD | PRG_MOD | PAL_MOD |
|----------|---------|----------|---------|---------|
| 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 1 |
| 3 | 0 | 1 | 0 | 0 |
| 4 | 1 | 0 | 0 | 1 |
| 5 | 1 | 0 | 0 | 0 |
| 6 | 0 | 1 | 1 | 1 |
| 7 | 1 | 0 | 1 | 1 |
| 8 | 0 | 1 | 1 | 0 |
| 9 | 1 | 0 | 1 | 0 |
| 10/11 | 1 | 1 | 1 | 1 |

NOTES:

Mode10 and mode11 are bypass modes that indicate output the image with the same size as input from sensor.

8. ELECTRICAL CHARACTERISTICS

8.1. Recommended Operating Conditions

| SYMBOL | DESCRIPTIONS | MIN | TYP. | MAX | UNIT |
|----------------|------------------------------|------|------|------|------|
| VDD_IO | I/O Digital Voltage (3.3V) | 2.97 | 3.3 | 3.63 | V |
| VDD_CORE | Core Digital Voltage | 1.08 | 1.2 | 1.32 | V |
| VDDA_DAC | Video DAC Voltage | 2.97 | 3.3 | 3.63 | V |
| VDDA_PLL | PLL Voltage | 2.97 | 3.3 | 3.63 | V |
| VDDA_PR | Power Regulator (PR) Voltage | 2.97 | 3.3 | 3.63 | V |
| T _o | Operating Temperature | -40 | | +85 | °C |
| T _s | Storage Temperature | -40 | | +125 | °C |

8.2. Digital I/O Electrical Characteristic

For 3.3 V I/O Application

| SYMBOL | DESCRIPTION | MIN | TYP. | MAX | UNIT |
|--------|--------------------------------------|------|------|----------|------|
| VIL | Input low voltage | -0.3 | | 0.8 | V |
| VIH | Input high voltage | 2.0 | | OVDD+0.3 | V |
| IL | Input Leakage Current | | | ±1 | μA |
| RPU | Internal pull-up resistor | 56 | 73 | 113 | kΩ |
| RPD | Internal pull-down resistor | 55 | 79 | 155 | kΩ |
| VOL | Output low voltage | | | 0.4 | V |
| VOH | Output high voltage | 2.4 | | | V |
| IOL | Low Level output current @ VOL=0.4V | 4.5 | 7.4 | 9.3 | mA |
| IOH | High Level output current @ VOH=2.4V | 4.5 | 9.4 | 14.7 | mA |

8.3. VIDEO DAC Electrical Characteristics

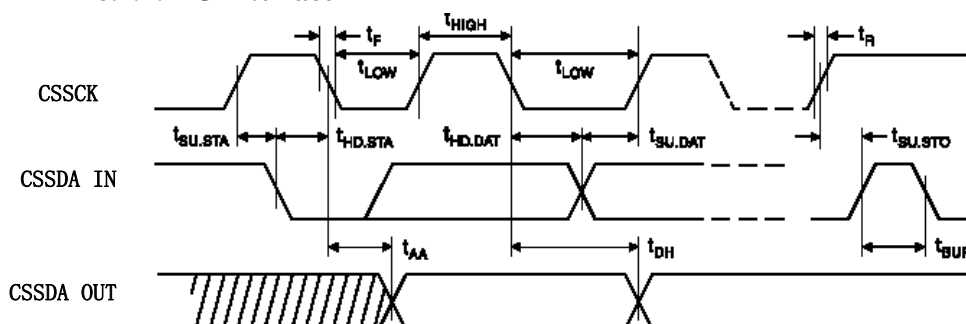
(VDD_VDAC = 3.3V , RL=37.5ohm , CL=10pF , VREFIN=1.24V; TEMP = 25° c)

| SYMBOL | DESCRIPTION | MIN | TYP. | MAX | UNIT |
|--------|-------------|-----|------|-----|------|
|--------|-------------|-----|------|-----|------|

| | | | | | |
|--------------------|----------------------------------|--|-------|------|------|
| I _{fs} | Max per-channel output current | | 34.1 | | mA |
| V _{fs} | Max output voltage | | 1.278 | | V |
| - | DAC resolution | | 10 | | bits |
| ERR _{inl} | Integral non-linearity error | | ±1 | ±1.5 | LSB |
| ERR _{dnl} | Differential non-linearity error | | ±0.5 | ±1 | LSB |

8.4. AC Electrical Characteristic

8.4.1: I²C Interface



| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---------------------|--|-----|-----|-----|------|
| f _{SCK} | CS_SCK clock frequency | 0 | | 100 | KHz |
| t _{BUF} | Bus free time between a STOP and a START | 4.7 | | - | μs |
| t _{HD.STA} | Hold time for a START | 4.0 | | - | μs |
| t _{LOW} | Low period of CS_SCK | 4.7 | | - | μs |
| t _{HIGH} | High period of CS_SCK | 4.0 | | - | μs |
| t _{SU.STA} | Setup time for START | 4.7 | | - | μs |
| t _{HD.DAT} | Data hold time | 0 | | - | μs |
| t _{SU.DAT} | Data setup time | 200 | | - | ns |
| t _R | Rise time of CS_SDA and CS_SCK | - | | 1 | μs |
| t _F | Fall time of CS_SDA and CS_SCK | - | | 300 | ns |
| t _{AA} | CS_SCK low to data out valid | | 2.5 | | μs |
| t _{DH} | Data out hold time | | 2.5 | | μs |
| t _{SU.STO} | Setup time for STOP | 4.7 | | - | μs |

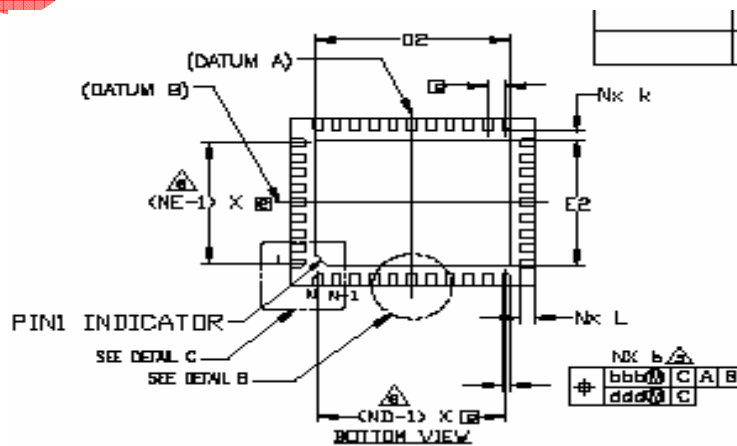
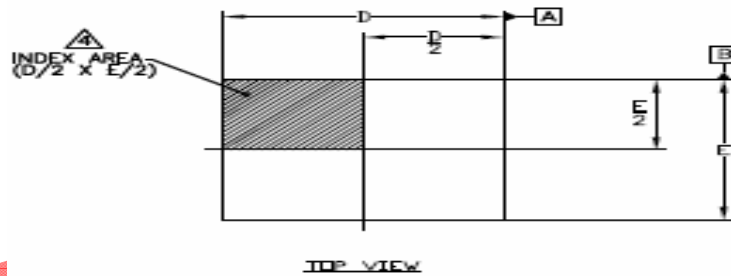
9. PACKAGE INFORMATION

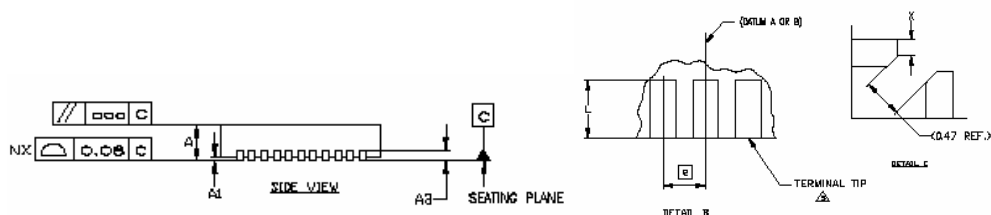
9.1. Chip Marking Information

On-chip markings are shown as in following table. The last line is a 7-digit tracking number.

| MARKING INFORMATION | LEAD-FREE PACKAGE |
|---------------------|--------------------------------------|
| | Vimicro VC0702NJSB Tracking No |
| | Vimicro VC0702PLSB Tracking No |

9.2. VC0702NJSB Package Specification





| SYMBOL | COMMON DIMENSIONS | | | NOTE |
|---------------------------------|-------------------|----------|------|------|
| | MIN. | NOM. | MAX. | |
| A1 | 0.00 | 0.02 | 0.05 | |
| A3 | - | 0.20 REF | - | |
| k | 0.20 | - | - | |
| X | b/2 | - | - | |
| TOLERANCES OF FORM AND POSITION | | | | |
| bbb | | 0.10 | | |
| ccc | | 0.10 | | |
| ddd | | 0.05 | | |

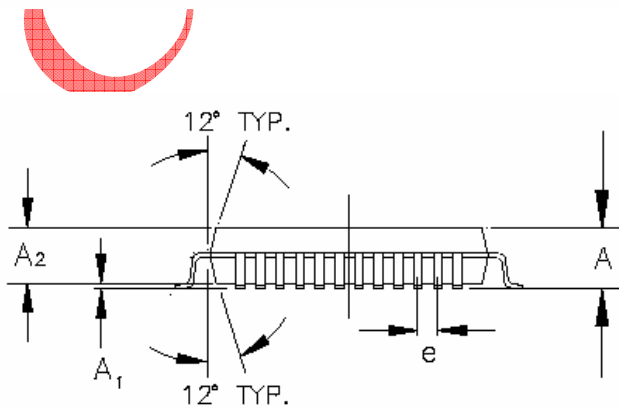
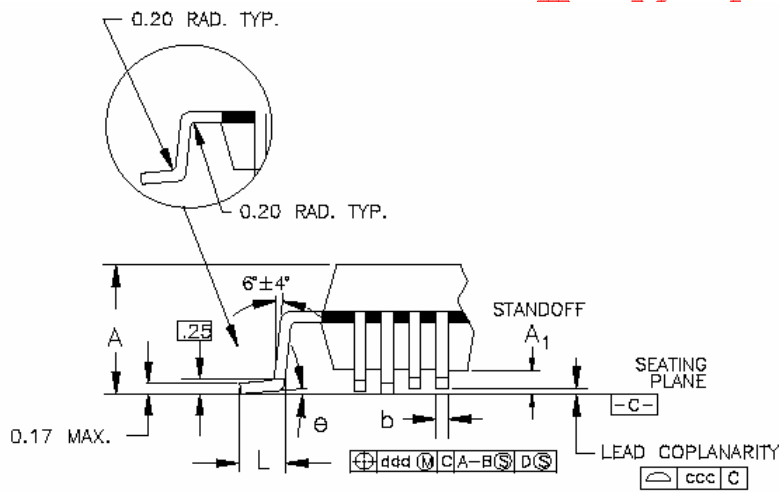
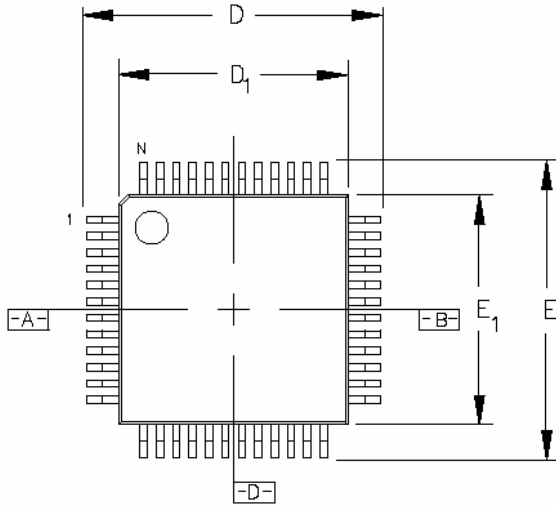
| PACKAGE | 40L 6.5 * 5.5 - 0.50 | | |
|---------|----------------------|------|------|
| REF. | MIN. | NOM. | MAX. |
| A | 0.80 | 0.90 | 1.00 |
| b | 0.18 | 0.25 | 0.30 |
| D | 6.40 | 6.50 | 6.60 |
| D2 | 5.00 | 5.15 | 5.30 |
| E | 5.40 | 5.50 | 5.60 |
| E2 | 4.00 | 4.15 | 4.30 |
| e | 0.50 BSC. | | |
| L | 0.35 | 0.40 | 0.45 |
| N | 40 | | |
| ND | 11 | | |
| NE | 9 | | |

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC PUB. 95 SEC. 4.3 SPP-002. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZOED INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.

- DETAIL C; AS REQUIRED TO MAINTAIN MINIMUM SPACING BETWEEN LEADS.
- REF. TO JEDEC MO-220G. IT IS FOR DIMENSIONS TOLERANCE CONTROL ONLY EXCEPT D2, E2.

9.3. VC0702PLSB Package Specification

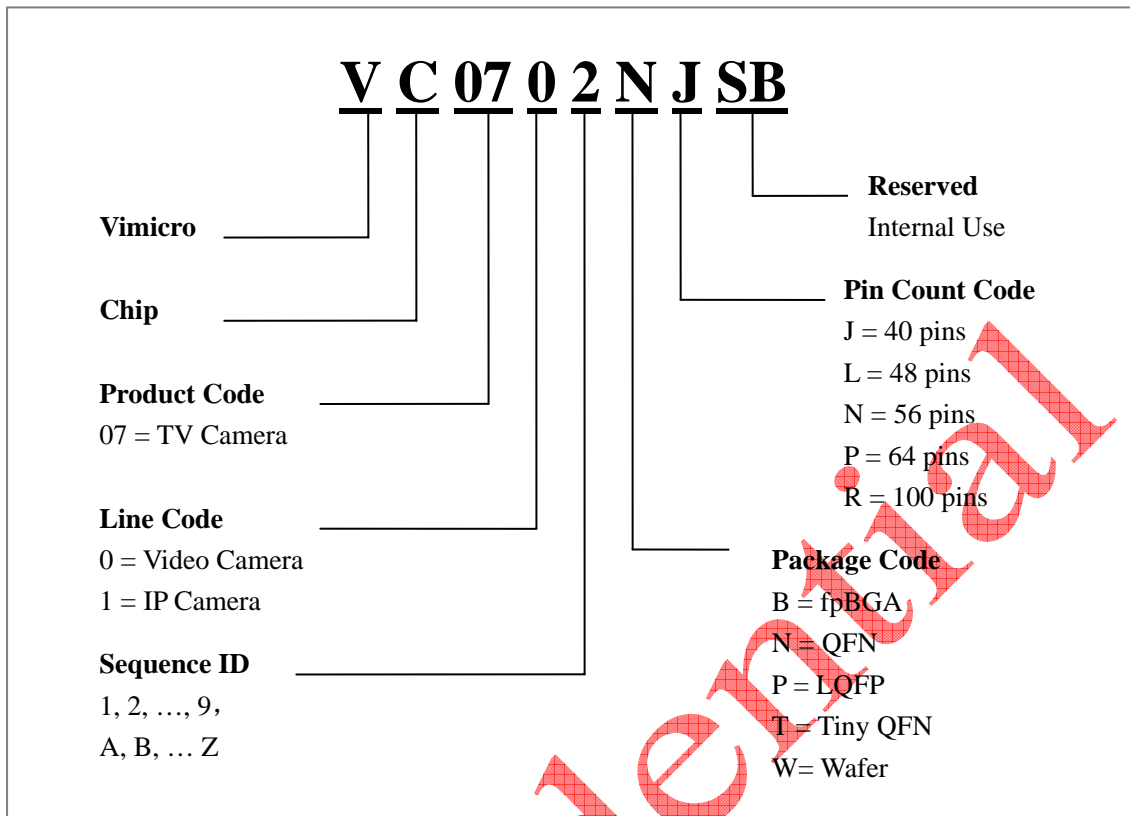


| 48L LEAD COUNT , 1.4 mm THICK | | |
|-------------------------------|-------------|--------------------|
| DIMS. | TOL. | |
| A | MAX. | 1.60 |
| A1 | | .05 MIN./ .15 MAX. |
| A2 | ±.05 | 1.40 |
| D | ±.20 | 9.00 |
| D1 | .10 | 7.00 |
| E | ±.20 | 9.00 |
| E1 | .10 | 7.00 |
| L | + .15/- .10 | .60 |
| e | BASIC | .50 |
| b | ±.05 | .22 |
| θ | | 0°-7° |
| ddd | MAX. | .08 |
| ccc | MAX. | .08 |
| JEDEC REFERENCE DRAWING | | MS-026 |
| VARIATION DESIGNATOR | | ABC BBC |

NOTES :

1. All dimensions in mm .
2. Dimension shown are nominal with tolerances indicated .
3. Foot length 'L' is measured at gage plane 0.25mm above seating plane .
4. L/F: Eftec 64T Cu or equivalent, 0.127mm(0.005") thick

10. TV CAMERA PRODUCT NAMING CONVENTION



11. CONTACT INFORMATION

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12. REVISION HISTORY

| REVISION No. | REMARKS | DATE |
|--------------|-----------------------------------|-----------|
| 0.98 | Preliminary release | 2006-2-21 |
| 0.99 | Updated for VC0702NJSB/VC0702PLSB | 2006-4-20 |
| | | |