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Signetics

74181, LS181, S181 Arithmetic Logic Units

4-Bit Arithmetic Logic Unit
Product Specification

Logic Products

FEATURES

- **Provides 16 arithmetic operations: ADD, SUBTRACT, COMPARE, DOUBLE, plus 12 other arithmetic operations**
- **Provides all 16 logic operations of two variables: Exclusive-OR, Compare, AND, NAND, NOR, OR, plus 10 other logic operations**
- **Full lookahead carry for high-speed arithmetic operation on long words**

DESCRIPTION

The '181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs ($S_0 - S_3$) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74181	22ns	91mA
74LS181	22ns	21mA
74S181	11ns	120mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$
Plastic DIP	N74181N, N74LS181N, N74S181N

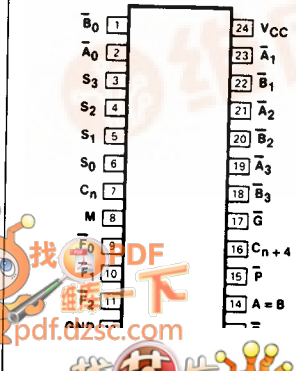
NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

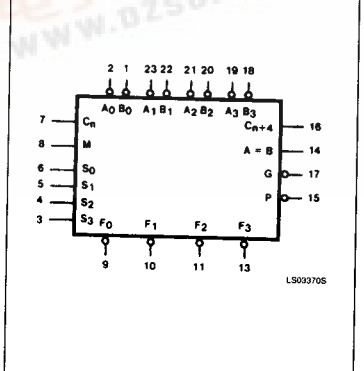
PINS	DESCRIPTION	74	74S	74LS
Mode	Input	1ul	1Sul	1LSul
$\overline{A}$ or $\overline{B}$	Inputs	3ul	3Sul	3LSul
S	Inputs	4ul	4Sul	4LSul
Carry	Input	5ul	5Sul	5LSul
$F_0 - F_3$, = B, C_{n+4}	Outputs	10ul	10Sul	10LSul
$\overline{G}$	Output	10ul	10Sul	40LSul
$\overline{P}$	Output	10ul	10Sul	20LSul

NOTE:
Where a 74 unit load (ul) is understood to be 40μA I_{IH} and -1.6mA I_{IL}, a 74S unit load (Sul) is 50μA I_{IH} and -2.0mA I_{IL}, and 74LS unit load (LSul) is 20μA I_{IH} and -0.4mA I_{IL}.

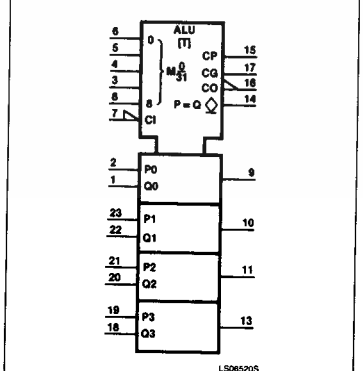
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high-speed operation the device is used in conjunction with the '182 carry lookahead circuit. One carry lookahead package is required for each group of four '181 devices. Carry lookahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

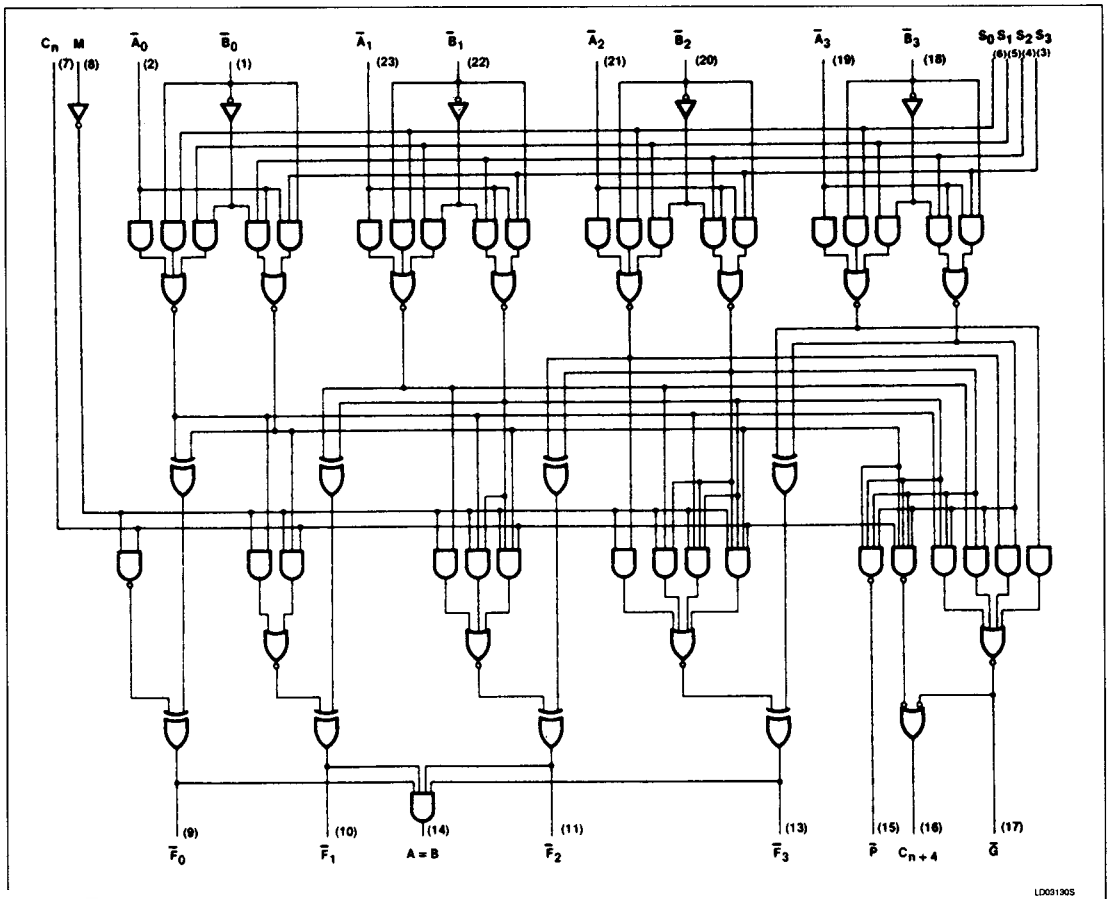
The A = B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over 4 bits when the unit is in the subtract mode. The A = B output is open collector and can be wired-AND with other A = B outputs to give a comparison for more than 4 bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied.

Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus, a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

LOGIC DIAGRAM



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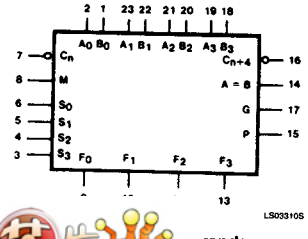
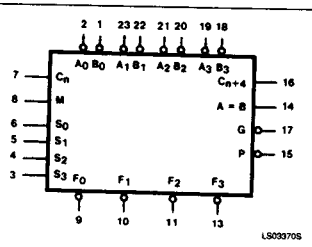
MODE SELECT — FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE HIGH INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	Logic (M = H)	Arithmetic** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A
L	L	L	H	$\overline{A+B}$	A + B
L	L	H	L	$\overline{A}B$	A + $\overline{B}$
L	L	H	H	Logical 0	minus 1
L	H	L	L	$\overline{AB}$	A plus A$\overline{B}$
L	H	L	H	$\overline{B}$	(A + B) plus A$\overline{B}$
L	H	H	L	A ● B	A minus B minus 1
L	H	H	H	A$\overline{B}$	AB minus 1
H	L	L	L	$\overline{A}$ + B	A plus AB
H	L	L	H	$\overline{A \bullet B}$	A plus B
H	L	H	L	B	(A + $\overline{B}$) plus AB
H	L	H	H	AB	AB minus 1
H	H	L	L	Logical 1	A plus A*
H	H	L	H	A + $\overline{B}$	(A + B) plus A
H	H	H	L	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A minus 1

MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	Logic (M = H)	Arithmetic** (M = L) (C_n = L)
L	L	L	L	$\overline{A}$	A minus 1
L	L	L	H	$\overline{AB}$	AB minus 1
L	L	H	L	$\overline{A}$ + B	A$\overline{B}$ minus 1
L	L	H	H	Logical 1	minus 1
L	H	L	L	$\overline{A+B}$	A plus (A + $\overline{B}$)
L	H	L	H	$\overline{B}$	AB plus (A + $\overline{B}$)
L	H	H	L	$\overline{A \bullet B}$	A minus B minus 1
L	H	H	H	A + $\overline{B}$	A + $\overline{B}$
H	L	L	L	$\overline{AB}$	A plus (A + B)
H	L	L	H	$\overline{A \bullet B}$	A plus B
H	L	H	L	B	A$\overline{B}$ (A + B)
H	L	H	H	A + B	A + B
H	H	L	L	Logical 0	A plus A*
H	H	L	H	A$\overline{B}$	AB plus A
H	H	H	L	AB	A$\overline{B}$ plus A
H	H	H	H	A	A

L = LOW voltage
H = HIGH voltage level
*Each bit is shifted to the next more significant position.
**Arithmetic operations expressed in 2s complement notation.





ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			74S			UNIT
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current			−12			−18			−18	mA
I_{OH}	HIGH-level output current			−800			−400			−1000	μA
I_{OL}	LOW-level output current			16			8			20	mA
T_A	Operating free-air temperature	0		70	0		70	0		70	°C

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SUM MODE TEST TABLE I

FUNCTION INPUTS: $S_0 = S_3 = 4.5V$, $S_1 = s_2 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

DIFF MODE TEST TABLE II

FUNCTION INPUTS: $S_0 = S_3 = 4.5V$, $S_1 = S_2 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	Any $\overline{F}$ or C_{n+4}

LOGIC MODE TEST TABLE III

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			74181			74LS181			74S181			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Any output except A = B		2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX All outputs			0.2	0.4		0.35	0.5			0.5	V
			I_{OL} = 4mA						0.25	0.4				V
			I_{OL} = 16mA $\overline{G}$ output						0.47	0.7				V
			I_{OL} = 8mA $\overline{P}$ output						0.35	0.5				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5			−1.5			−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	Mode input				1.0			0.1			1.0	mA
			$\overline{A}$ or $\overline{B}$ inputs				1.0			0.3			1.0	mA
			S inputs				1.0			0.4			1.0	mA
			Carry input				1.0			0.5			1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	Mode input			40							μA
				$\overline{A}$ or $\overline{B}$ inputs			120							μA
				S inputs			160							μA
				Carry input			200							μA
			V_I = 2.7V	Mode input						20			50	μA
				$\overline{A}$ or $\overline{B}$ inputs						60			150	μA
				S inputs						80			200	μA
				Carry input						100			250	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V	Mode input			−1.6			−0.4				mA
				$\overline{A}$ or $\overline{B}$ inputs			−4.8			−1.2				mA
				S inputs			−6.4			−1.6				mA
				Carry input			−8			−2				mA
			V_I = 0.5V	Mode input									−2	mA
				$\overline{A}$ or $\overline{B}$ inputs									−6	mA
				S inputs									−8	mA
				Carry input									−10	mA
I_{OH}	HIGH-level output current	V_{IH} = MIN, V_{IL} = MAX, V_{OH} = 5.5V A = B only					250			100			250	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX Any output except A = B			−18		−57	−15		−100	−40		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX		Note 4a		88	140		20	34		120	220	mA
				Note 4b		94	150		21	37		120	220	mA

NOTES:

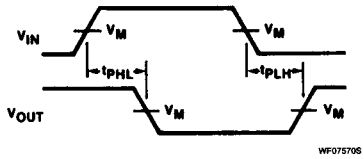
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

nditions: a. S_0 through S_3, M, and A inputs are at 4.5V, other inputs grounded, all outputs open. b. S_0 through S_3 and M inputs , all outputs open.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

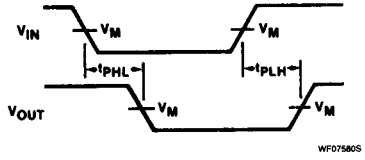
PARAMETER		TEST CONDITIONS	74		74LS		74S		UNIT
			$C_L = 15pF$ $R_L = 400\Omega$		$C_L = 15pF$ $R_L = 2k\Omega$		$C_L = 15pF$ $R_L = 280\Omega$		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	M = 0V, Sum or Diff Mode see Waveform 2 and Tables I & II		18 19		27 20		10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay C_n to $\overline{F}$ outputs	M = 0V, Sum or Diff Mode see Waveform 2 and Tables I & II		19 18		26 20		12 12	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5V Sum Mode, see Waveform 2 and Table I		19 19		29 23		12 12	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V Diff Mode, see Waveform 3 and Table II		25 25		32 32		15 15	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5V Sum Mode, see Waveform 2 and Table I		19 25		30 30		12 12	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V Diff Mode, see Waveform 3 and Table II		25 25		30 33		15 15	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5V Sum Mode, see Waveform 2 and Table I		42 32		32 20		16.5 16.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V Diff Mode, see Waveform 3 and Table II		48 34		32 32		20 22	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs	M = 4.5V, Logic Mode see Waveform 2 and Table III		48 34		33 38		20 22	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to C_{n+4} output	M = 0V, S_0 = S_3 = 4.5V, S_1 = S_2 = 0V Sum Mode, see Waveform 1 and Table I		43 41		38 38		18.5 18.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to C_{n+4} outputs	M = 0V, S_0 = S_3 = 0V, S_1 = S_2 = 4.5V Diff Mode, see Waveform 4 and Table II		50 50		41 41		23 23	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to A = B output	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V Diff Mode, see Waveform 3 and Table II		50 48		50 62		23 30	ns

AC WAVEFORMS



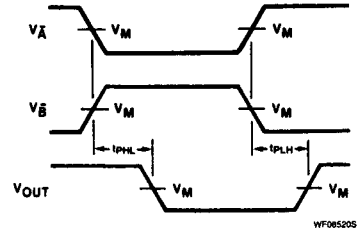
V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS

Waveform 1



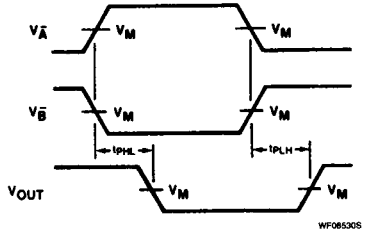
V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS

Waveform 2



V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS

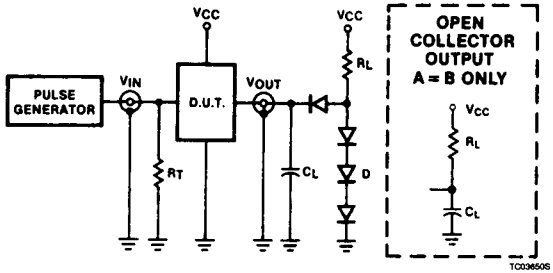
Waveform 3



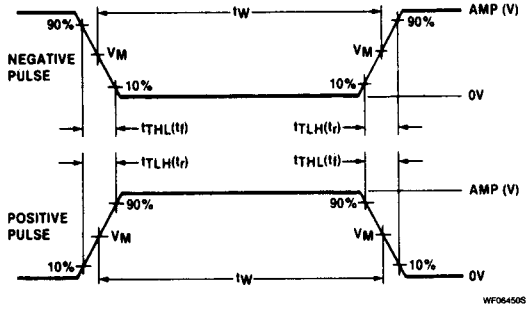
V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS

Waveform 4

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Totem-Pole Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

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