Octal dual supply translating transceiver; 3-state 74LVC4245A

FEATURES

- In accordance with JEDEC standard no. 8-1A
- Wide supply voltage range:
  3 V port: 1.5 to 3.6 V
  5 V port: 1.5 to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Control inputs accept voltages up to 5.5 V.

DESCRIPTION

The 74LVC4245A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC4245A is an octal dual supply translating transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. It is designed to interface between a 3 and 5 V bus in a mixed 3/5 V supply environment.

The 74LVC4245A features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. ($\overline{OE}$) controls the outputs so that the buses are effectively isolated.

In suspend mode, when V_{CCA} is zero, there will be no current flow from one supply to the other supply. The A-outputs must be set 3-state and the voltage on the A-bus must be smaller than V_{diode} (typ. 0.7 V). $V_{CCA} \geq V_{CCB}$ (except in suspend mode).

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay	C_L = 50 pF		
	A_n to B_n	V_{CCA} = 5.0 V	4.0	ns
	B_n to A_n	V_{CCB} = 3.3 V	4.0	ns
$C_{I/O}$	input/output capacitance		10.0	pF
C_{PDA}	A port			
	A_n to B_n	V_I = GND to V_{CC}; note 1	7.8	pF
	B_n to A_n	V_I = GND to V_{CC}; note 1	27.9	pF
C_{PDB}	B port			
	A_n to B_n	V_I = GND to V_{CC}; note 1	26	pF
	B_n to A_n	V_I = GND to V_{CC}; note 1	10.4	pF

Note

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

FUNCTION TABLE

See note 1.

INPUT		INPUT/OUTPUT	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

Note

1. H = HIGH voltage level;
   L = LOW voltage level;
   X = don't care;
   Z = high-impedance OFF-state.

ORDERING INFORMATION

OUTSIDE NORTH AMERICA	NORTH AMERICA	PACKAGE				
		TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC4245AD	74LVC4245AD	−40 to +85 °C	24	SO	plastic	SOT137-1
74LVC4245ADB	74LVC4245ADB		24	SSOP	plastic	SOT340-1
74LVC4245APW	74LVC4245ADH		24	TSSOP	plastic	SOT355-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	V_{CCA}	DC supply voltage (5 V bus)
2	DIR	direction control
3, 4, 5, 6, 7, 8, 9 and 10	A_0 to A_7	data inputs/outputs
11, 12 and 13	GND	ground (0 V)
14, 15, 16, 17, 18, 19, 20 and 21	B_7 to B_0	data inputs/outputs
22	$\overline{OE}$	output enable input (active LOW)
23 and 24	V_{CCB}	DC supply voltage (3 V bus)

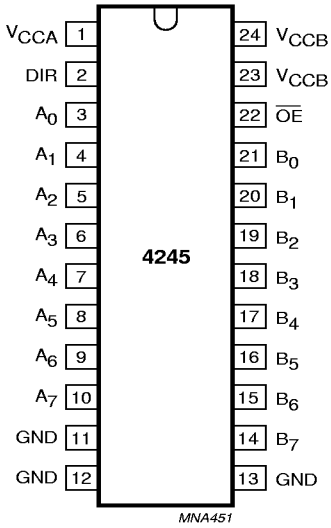


Fig.1 Pin configuration.

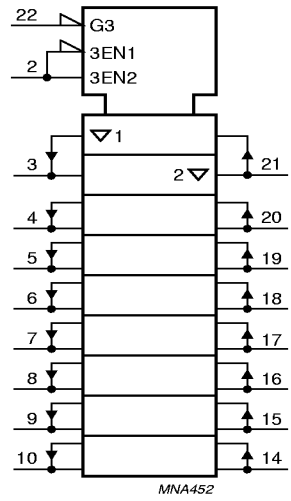


Fig.3 IEC logic symbol.

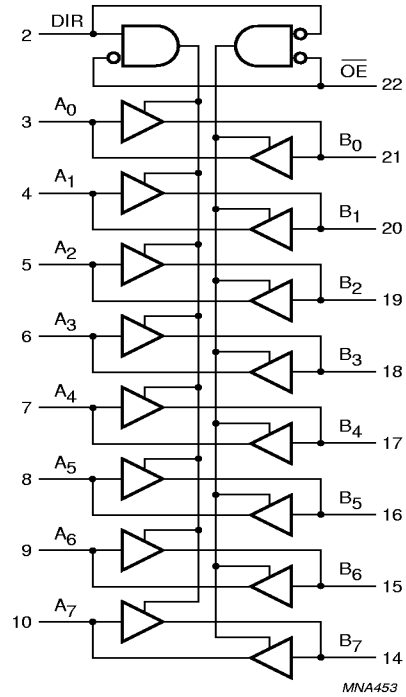


Fig.2 Logic symbol.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN.	MAX.	
V_{CCA}	DC supply voltage 5 V port (for maximum speed performance)	$V_{CCA} \geq V_{CCB}$ (see Fig.5)	1.5	5.5	V
V_{CCB}	DC supply voltage 3 V port (for low-voltage applications)	$V_{CCA} \geq V_{CCB}$ (see Fig.5)	1.5	3.6	V
V_I	DC input voltage range (control inputs)		0	5.5	V
$V_{I/O}$	DC input voltage range; output 3-state		0	5.5	V
	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
T_{amb}	operating ambient temperature range	see DC and AC characteristics per device	−40	+85	°C
t_r, t_f	input rise and fall times	V_{CCB} = 2.7 to 3.0 V	0	20	ns/V
		V_{CCB} = 3.0 to 3.6 V	0	10	
		V_{CCA} = 3.0 to 4.5 V	0	20	
		V_{CCA} = 4.5 to 5.5 V	0	10	

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	DC supply voltage 5 V port		−0.5	+6.5	V
V_{CCB}	DC supply voltage 3 V port		−0.5	+4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–	−50	mA
V_I	DC input voltage	note 1	−0.5	+6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
$V_{I/O}$	DC output voltage; output HIGH or LOW	note 1	−0.5	V_{CC} + 0.5	V
	DC input voltage; output 3-state	note 1	−0.5	+6.5	V
I_O	DC output diode current	V_O = 0 to V_{CC}	–	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	power dissipation per package				
	plastic mini-pack (SO)	above 70 °C derate linearly with 8 mW/K	–	500	mW
	plastic shrink mini-pack (SSOP and TSSOP)	above 60 °C derate linearly with 5.5 mW/K	–	500	mW

Note

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions; voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)			UNIT
		OTHER	$V_{CCA/B}$ (V)	–40 to +85			
				MIN.	TYP.(1)	MAX.	
V_{IH}	HIGH-level input voltage	3 V port	2.7 to 3.6	2.0	–	–	V
		5 V port	4.5 to 5.5	2.0	–	–	
V_{IL}	LOW-level input voltage	3 V port	2.7 to 3.6	–	–	0.8	V
		5 V port	4.5 to 5.5	–	–	0.8	
V_{OH}	HIGH-level output voltage (3 V port)	$V_I = V_{IH}$ or V_{IL}; $I_O = -12$ mA	2.7	$V_{CC} - 0.5$	–	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -100$ µA	3.0	$V_{CC} - 0.2$	V_{CC}	–	
		$V_I = V_{IH}$ or V_{IL}; $I_O = -24$ mA	3.0	$V_{CC} - 1.0$	–	–	
	HIGH-level output voltage (5 V port)	$V_I = V_{IH}$ or V_{IL}; $I_O = -12$ mA	4.5	$V_{CC} - 0.5$	–	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -100$ µA	4.5	$V_{CC} - 0.2$	V_{CC}	–	
		$V_I = V_{IH}$ or V_{IL}; $I_O = -24$ mA	4.5	$V_{CC} - 0.8$	–	–	
V_{OL}	LOW-level output voltage (3 V port)	$V_I = V_{IH}$ or V_{IL}; $I_O = 12$ mA	2.7	–	–	0.40	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 100$ µA	3.0	–	–	0.20	
		$V_I = V_{IH}$ or V_{IL}; $I_O = 24$ mA	3.0	–	–	0.55	
	LOW-level output voltage (5 V port)	$V_I = V_{IH}$ or V_{IL}; $I_O = 12$ mA	4.5	–	–	0.40	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 100$ µA	4.5	–	–	0.20	
		$V_I = V_{IH}$ or V_{IL}; $I_O = 24$ mA	4.5	–	–	0.55	
I_I	input leakage current	$V_I = 5.5$ V or GND; note 2	3.6	–	±0.1	±5	µA
I_{IHZ}/I_{ILZ}	input current for common I/O pins (3 V port)	$V_I = V_{CC}$ or GND	3.6	–	0.1	±15	µA
	input current for common I/O pins (5 V port)	$V_I = V_{CC}$ or GND	5.5	–	0.1	±15	µA
I_{OZ}	3-state output OFF-state current (3 V port)	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND	3.6	–	0.1	±5	µA
	3-state output OFF-state current (5 V port)	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND	5.5	–	0.1	±5	µA
I_{CC}	quiescent supply current (3 V port)	$V_I = V_{CC}$ or GND; $I_O = 0$	3.6	–	0.1	10	µA
	quiescent supply current (5 V port)	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5	–	0.1	10	µA
ΔI_{CC}	additional quiescent supply current per control pin (3 V port)	$V_I = V_{CC} - 0.6$ V; $I_O = 0$	2.7 to 3.6	–	5	500	µA
	additional quiescent supply current per control pin (5 V port)	$V_I = V_{CC} - 2.1$ V; $I_O = 0$	4.5 to 5.5	–	5	500	µA

Notes

1. All typical values are at $V_{CCA} = 5.0$ V, $V_{CCB} = 3.3$ V and $T_{amb} = 25$ °C.
2. Not for I/O pins.

AC CHARACTERISTICS

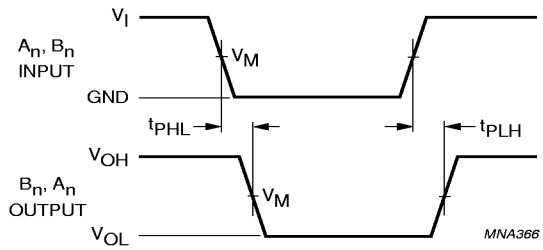
GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $T_{amb} = -40$ to 85 °C.

SYMBOL	PARAMETER	WAVEFORMS	LIMITS						UNIT
			V_{CCA} = 5 V ± 0.5 V						
			V_{CCB} = 3.3 V ± 0.3 V			V_{CCB} = 2.7 V			
			MIN.	TYP.(1)	MAX.	MIN.	TYP.(2)	MAX.	
t_{PHL}/t_{PLH}	propagation delay A_n to B_n	see Figs 4 and 7	1.5	4.0	6.5	1.5	4.5	7.0	ns
	propagation delay B_n to A_n	see Figs 4 and 7	1.5	4.0	6.5	1.5	4.5	7.0	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to A_n	see Figs 6 and 7	1.5	6.2	10	1.5	7.0	11.0	ns
	3-state output enable time $\overline{OE}$ to B_n	see Figs 6 and 7	1.5	5.0	8.1	1.5	5.7	8.7	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to A_n	see Figs 6 and 7	1.5	5.3	7.5	1.5	5.7	8.0	ns
	3-state output disable time $\overline{OE}$ to B_n	see Figs 6 and 7	1.5	5.8	7.8	1.5	6.2	8.5	ns

Notes

1. Typical values are measured at V_{CCA} = 5.0 V and V_{CCB} = 3.3 V and T_{amb} = 25 °C.
2. Typical values are measured at V_{CCA} = 5.0 V and T_{amb} = 25 °C.

AC WAVEFORMS



V_M = 1.5 V at 2.7 V ≤ V_{CCB} ≤ 3.6 V;
$V_M = 0.5V_{CCA}$ at $V_{CCA} \geq 4.5$ V;
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.4 The input (A_n, B_n) to output (B_n, A_n) propagation delays.

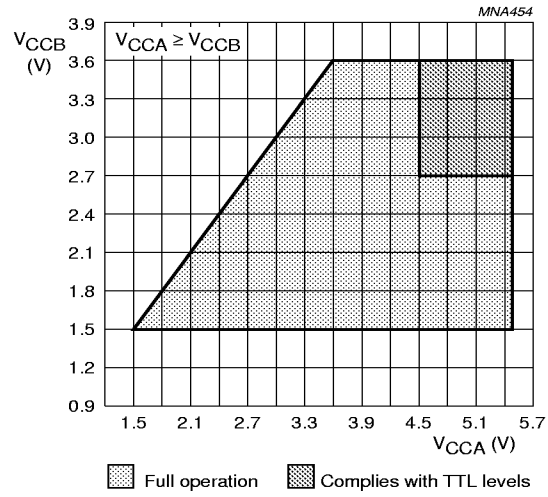
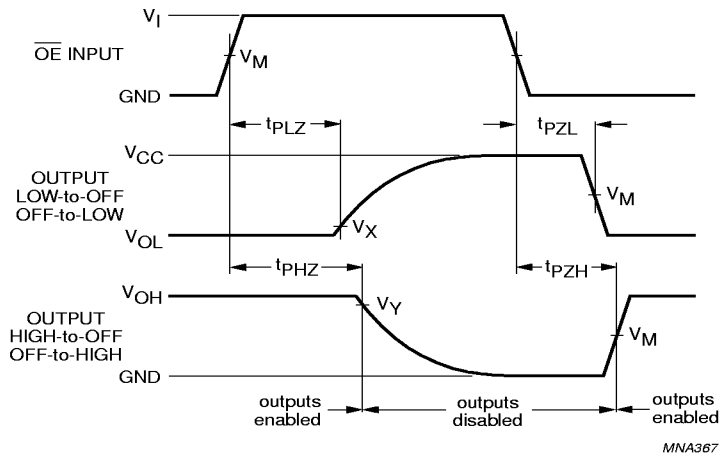


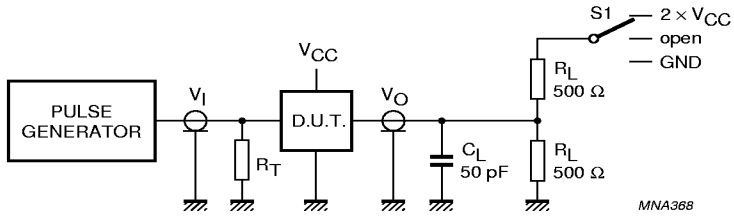
Fig.5 Supply operation area.



V_M = 1.5 V at 2.7 V ≤ V_{CCB} ≤ 3.6 V;
V_M = 0.5V_{CCA} at V_{CCA} ≥ 4.5 V;
V_X = V_{OL} + 0.3 V at V_{CCB} ≤ 3.6 V;
V_X = V_{OL} + 0.1 (V_{CCA} – V_{OL}) at V_{CCA} ≥ 4.5 V

V_Y = V_{OH} – 0.3 V at V_{CCB} ≤ 3.6 V;
V_Y = V_{OH} – 0.1 (V_{OH} – GND) at V_{CCA} ≥ 4.5 V;
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.6 The 3-state enable and disable times.



TEST	S_1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

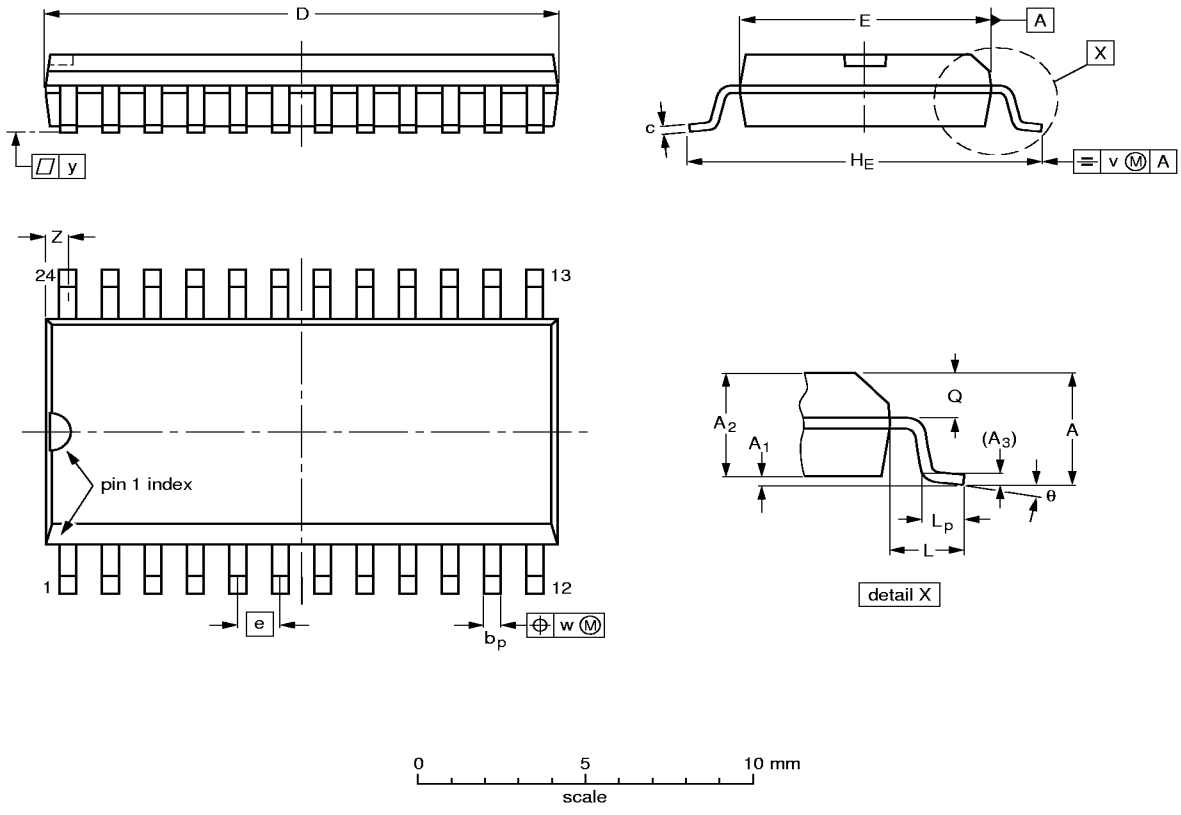
V_{CC}	V_I
for A and B port <2.7 V	V_{CC}
for B port 2.7 to 3.6 V	2.7 V
for A port 4.5 to 5.5 V	3.0 V

Definitions for test circuit:
R_L = Load resistor; see chapter “AC characteristics”.
C_L = Load capacitance including jig and probe capacitance (see chapter “AC characteristics”).
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.7 Load circuitry for switching times.

PACKAGE OUTLINES

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

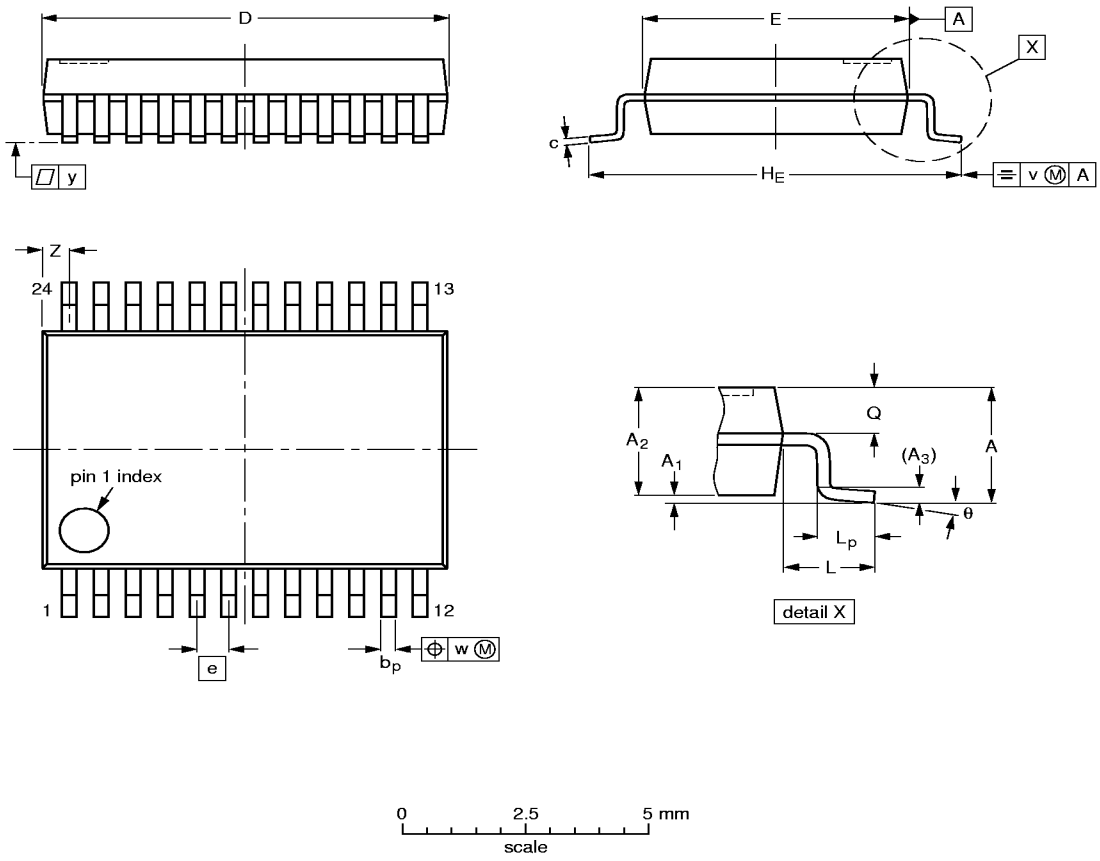
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

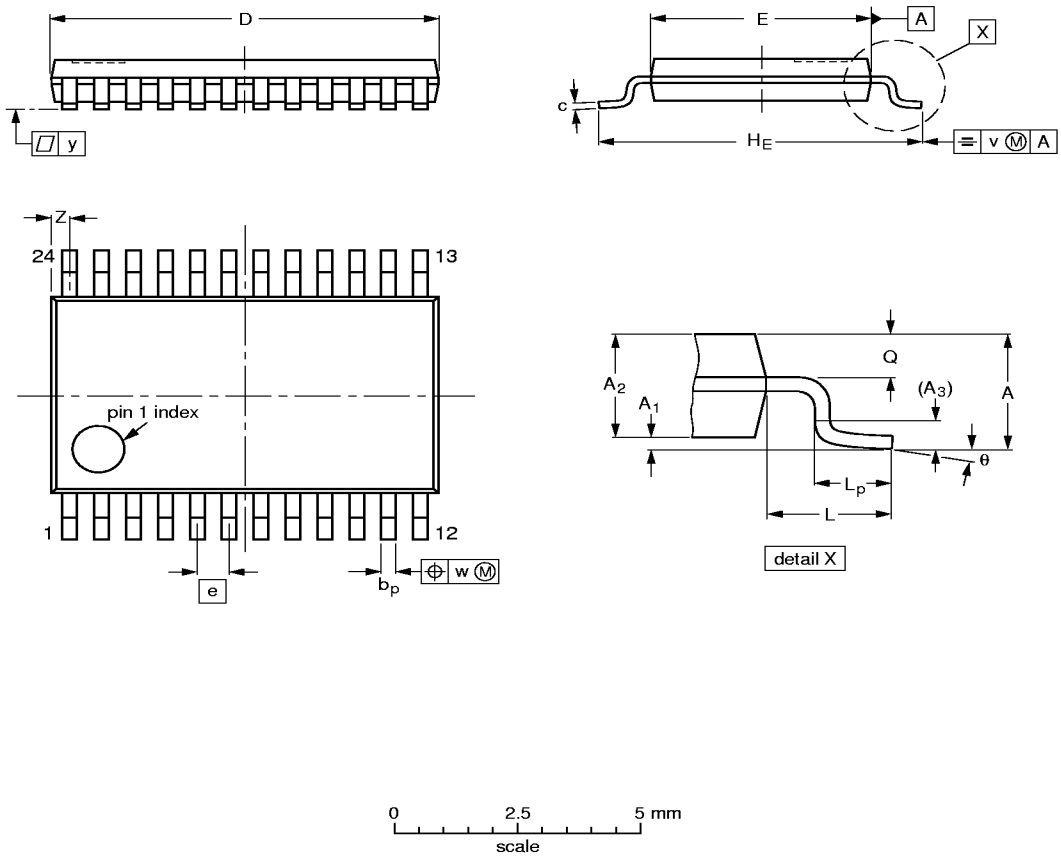
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				~~93-06-16~~ 95-02-04

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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