National Semiconductor

November 1993

# NMC27C64
# 65,536-Bit (8192 x 8) CMOS EPROM



## General Description

The NMC27C64 is a 64K UV erasable, electrically reprogrammable and one-time programmable (OTP) CMOS EPROM ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C64 is designed to operate with a single +5V power supply with ±10% tolerance. The CMOS design allows the part to operate over extended and military temperature ranges.

The NMC27C64Q is packaged in a 28-pin dual-in-line package with a quartz window. The quartz window allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

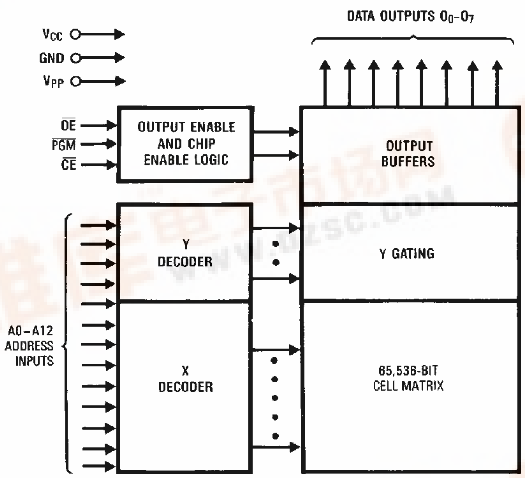
The NMC27C64N is packaged in a 28-pin dual-in-line plastic molded package without a transparent lid. This part is ideally suited for high volume production applications where cost is an important factor and programming only needs to be one once.

This family of EPROMs are fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

## Features

- High performance CMOS
  — 150 ns access time
- JEDEC standard pin configuration
  — 28-pin DIP package
  — 32-pin chip carrier
- Drop-in replacement for 27C64 or 2764
- Manufacturers identification code

## Block Diagram

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**Pin Names**

| | |
|---|---|
| A0–A12 | Addresses |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $O_0$–$O_7$ | Outputs |
| $\overline{PGM}$ | Program |
| NC | No Connect |
| $V_{PP}$ | Programming Voltage |
| $V_{CC}$ | Power Supply |
| GND | Ground |

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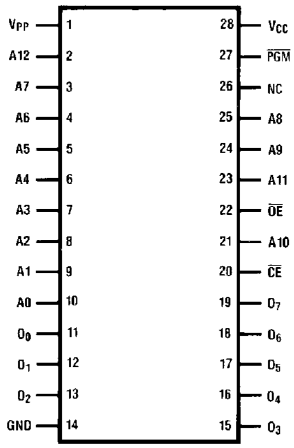
## Connection Diagram

| 27C512<br>27512 | 27C256<br>27256 | 27C128<br>27128 | 27C32<br>2732 | 27C16<br>2716 |
|---|---|---|---|---|
| A15 | $V_{PP}$ | $V_{PP}$ | | |
| A12 | A12 | A12 | | |
| A7 | A7 | A7 | A7 | A7 |
| A6 | A6 | A6 | A6 | A6 |
| A5 | A5 | A5 | A5 | A5 |
| A4 | A4 | A4 | A4 | A4 |
| A3 | A3 | A3 | A3 | A3 |
| A2 | A2 | A2 | A2 | A2 |
| A1 | A1 | A1 | A1 | A1 |
| A0 | A0 | A0 | A0 | A0 |
| $O_0$ | $O_0$ | $O_0$ | $O_0$ | $O_0$ |
| $O_1$ | $O_1$ | $O_1$ | $O_1$ | $O_1$ |
| $O_2$ | $O_2$ | $O_2$ | $O_2$ | $O_2$ |
| GND | GND | GND | GND | GND |

**NMC27C64Q/N**
**Dual-In-Line Package**




| 27C16<br>2716 | 27C32<br>2732 | 27C128<br>27128 | 27C256<br>27256 | 27C512<br>27512 |
|---|---|---|---|---|
| | | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |
| | | $\overline{PGM}$ | A14 | A14 |
| $V_{CC}$ | $V_{CC}$ | A13 | A13 | A13 |
| A8 | A8 | A8 | A8 | A8 |
| A9 | A9 | A9 | A9 | A9 |
| $V_{PP}$ | A11 | A11 | A11 | A11 |
| $\overline{OE}$ | $\overline{OE}/V_{PP}$ | $\overline{OE}$ | $\overline{OE}$ | $\overline{OE}/V_{PP}$ |
| A10 | A10 | A10 | A10 | A10 |
| $\overline{CE}/PGM$ | $\overline{CE}$ | $\overline{CE}$ | $\overline{CE}/\overline{PGM}$ | $\overline{CE}$ |
| $O_7$ | $O_7$ | $O_7$ | $O_7$ | $O_7$ |
| $O_6$ | $O_6$ | $O_6$ | $O_6$ | $O_6$ |
| $O_5$ | $O_5$ | $O_5$ | $O_5$ | $O_5$ |
| $O_4$ | $O_4$ | $O_4$ | $O_4$ | $O_4$ |
| $O_3$ | $O_3$ | $O_3$ | $O_3$ | $O_3$ |

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**Note:** Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C64 pins.

**Commercial Temperature Range**
**$V_{CC}$ = 5V ±10%**

| Parameter/Order Number | Access Time (ns) |
|---|---|
| NMC27C64Q, N150 | 150 |
| NMC27C64Q, N200 | 200 |
| NMC27C64Q, N250 | 250 |

**Extended Temp Range (−40°C to +85°C)**
**$V_{CC}$ = 5V ±10%**

| Parameter/Order Number | Access Time (ns) |
|---|---|
| NMC27C64QE150 | 150 |
| NMC27C64QE200 | 200 |

**Military Temp Range (−55°C to +125°C)**
**$V_{CC}$ = 5V ±10%**

| Parameter/Order Number | Access Time (ns) |
|---|---|
| NMC27C64QM200 | 200 |
| NMC27C64QM250 | 250 |

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Temperature Under Bias | −55°C to +125°C |
| Storage Temperature | −65°C to +150°C |
| All Input Voltages except A9 with Respect to Ground (Note 10) | +6.5V to −0.6V |
| All Output Voltages with Respect to Ground (Note 10) | $V_{CC}$ + 1.0V to GND − 0.6V |
| $V_{PP}$ Supply Voltage and A9 with Respect to Ground During Programming | +14.0V to −0.6V |
| $V_{CC}$ Supply Voltage with Respect to Ground | +7.0V to −0.6V |
| Power Dissipation | 1.0W |
| Lead Temperature (Soldering, 10 sec.) | 300°C |
| ESD Rating (Mil Spec 883C, Method 3015.2) | 2000V |

## Operating Conditions (Note 7)

| | |
|---|---|
| Temperature Range | |
| NMC27C64Q150, 200, 250<br>NMC27C64N150, 200, 250 | 0°C to +70°C |
| NMC27C64QE150, 200 | −40°C to +85°C |
| NMC27C64QM200, M250 | −55°C to +125°C |
| $V_{CC}$ Power Supply | +5V ±10% |

## READ OPERATION

## DC Electrical Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN} = V_{CC}$ or GND | | | 10 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$ | | | 10 | µA |
| $I_{CC1}$ (Note 9) | $V_{CC}$ Current (Active) TTL Inputs | $\overline{CE} = V_{IL}$, f = 5 MHz Inputs = $V_{IH}$ or $V_{IL}$, I/O = 0 mA | | 5 | 20 | mA |
| $I_{CC2}$ (Note 9) | $V_{CC}$ Current (Active) CMOS Inputs | $\overline{CE}$ = GND, f = 5 MHz Inputs = $V_{CC}$ or GND, I/O = 0 mA | | 3 | 10 | mA |
| $I_{CCSB1}$ | $V_{CC}$ Current (Standby) TTL Inputs | $\overline{CE} = V_{IH}$ | | 0.1 | 1 | mA |
| $I_{CCSB2}$ | $V_{CC}$ Current (Standby) CMOS Inputs | $\overline{CE} = V_{CC}$ | | 0.5 | 100 | µA |
| $I_{PP}$ | $V_{PP}$ Load Current | $V_{PP} = V_{CC}$ | | | 10 | µA |
| $V_{IL}$ | Input Low Voltage | | −0.1 | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | | $V_{CC}$ + 1 | V |
| $V_{OL1}$ | Output Low Voltage | $I_{OL}$ = 2.1 mA | | | 0.45 | V |
| $V_{OH1}$ | Output High Voltage | $I_{OH}$ = −400 µA | 2.4 | | | V |
| $V_{OL2}$ | Output Low Voltage | $I_{OL}$ = 0 µA | | | 0.1 | V |
| $V_{OH2}$ | Output High Voltage | $I_{OH}$ = 0 µA | $V_{CC}$ − 0.1 | | | V |

## AC Electrical Characteristics

| Symbol | Parameter | Conditions | NMC27C64Q/N | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | 150, E150 | | 200, E200, M200 | | 250, M250 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{ACC}$ | Address to Output Delay | $\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$ | | 150 | | 200 | | 250 | ns |
| $t_{CE}$ | $\overline{CE}$ to Output Delay | $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$ | | 150 | | 200 | | 250 | ns |
| $t_{OE}$ | $\overline{OE}$ to Output Delay | $\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$ | | 60 | | 60 | | 70 | ns |
| $t_{DF}$ | $\overline{OE}$ High to Output Float | $\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$ | 0 | 60 | 0 | 60 | 0 | 60 | ns |
| $t_{CF}$ | $\overline{CE}$ High to Output Float | $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$ | 0 | 60 | 0 | 60 | 0 | 60 | ns |
| $t_{OH}$ | Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First | $\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$ | 0 | | 0 | | 0 | | ns |

## Capacitance $T_A = +25°C$, f = 1 MHz (Note 2) NMC27C64Q

| Symbol | Parameter | Conditions | Typ | Max | Units |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN} = 0V$ | 6 | 8 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT} = 0V$ | 9 | 12 | pF |

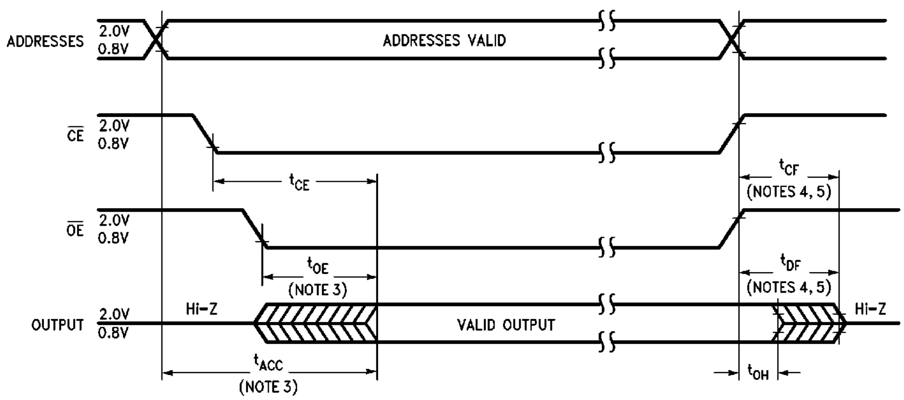
## Capacitance $T_A = +25°C$, f = 1 MHz (Note 2) NMC27C64N

| Symbol | Parameter | Conditions | Typ | Max | Units |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN} = 0V$ | 5 | 10 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT} = 0V$ | 8 | 10 | pF |

## AC Test Conditions

| | |
|---|---|
| Output Load | 1 TTL Gate and $C_L = 100$ pF (Note 8) |
| Input Rise and Fall Times | ≤5 ns |
| Input Pulse Levels | 0.45V to 2.4V |
| Timing Measurement Reference Level | |
| Inputs | 0.8V and 2V |
| Outputs | 0.8V and 2V |

## AC Waveforms (Notes 6 & 9)

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**Note 1:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** This parameter is only sampled and is not 100% tested.

**Note 3:** $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting $t_{ACC}$.

**Note 4:** The $t_{DF}$ and $t_{CF}$ compare level is determined as follows:
High to TRI-STATE, the measured $V_{OH1}$ (DC) − 0.10V;
Low to TRI-STATE, the measured $V_{OL1}$ (DC) + 0.10V.

**Note 5:** TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

**Note 6:** The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between $V_{CC}$ and GND.

**Note 7:** The outputs must be restricted to $V_{CC}$ + 1.0V to avoid latch-up and device damage.

**Note 8:** 1 TTL Gate: $I_{OL}$ = 1.6 mA, $I_{OH}$ = −400 µA.
$C_L$: 100 pF includes fixture capacitance.

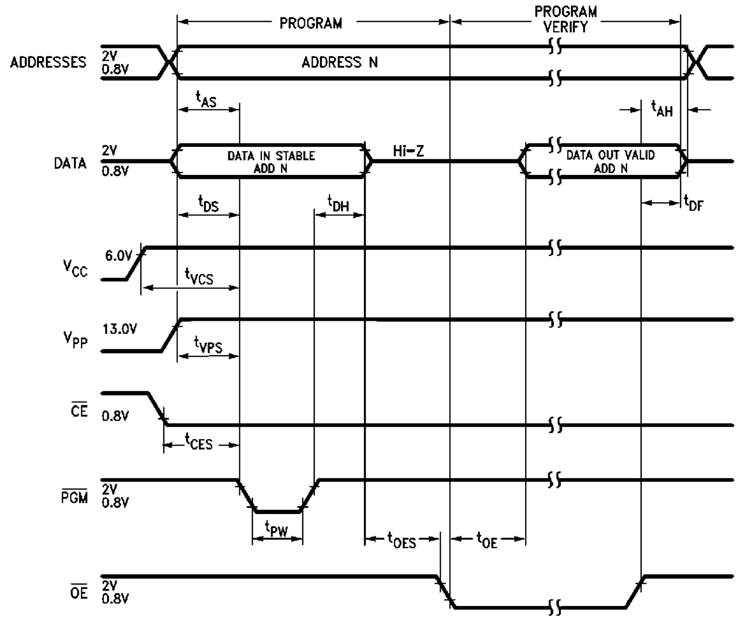
**Note 9:** $V_{PP}$ may be connected to $V_{CC}$ except during programming.

**Note 10:** Inputs and outputs can undershoot to −2.0V for 20 ns Max.

## Programming Characteristics (Notes 1, 2, 3 & 4)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{AS}$ | Address Setup Time | | 2 | | | µs |
| $t_{OES}$ | $\overline{OE}$ Setup Time | | 2 | | | µs |
| $t_{CES}$ | $\overline{CE}$ Setup Time | | 2 | | | µs |
| $t_{DS}$ | Data Setup Time | | 2 | | | µs |
| $t_{VPS}$ | $V_{PP}$ Setup Time | | 2 | | | µs |
| $t_{VCS}$ | $V_{CC}$ Setup Time | | 2 | | | µs |
| $t_{AH}$ | Address Hold Time | | 0 | | | µs |
| $t_{DH}$ | Data Hold Time | | 2 | | | µs |
| $t_{DF}$ | Output Enable to Output Float Delay | $\overline{CE} = V_{IL}$ | 0 | | 130 | ns |
| $t_{PW}$ | Program Pulse Width | | 0.45 | 0.5 | 0.55 | ms |
| $t_{OE}$ | Data Valid from $\overline{OE}$ | $\overline{CE} = V_{IL}$ | | | 150 | ns |
| $I_{PP}$ | $V_{PP}$ Supply Current During Programming Pulse | $\overline{CE} = V_{IL}$<br>$\overline{PGM} = V_{IL}$ | | | 30 | mA |
| $I_{CC}$ | $V_{CC}$ Supply Current | | | | 10 | mA |
| $T_A$ | Temperature Ambient | | 20 | 25 | 30 | °C |
| $V_{CC}$ | Power Supply Voltage | | 5.75 | 6.0 | 6.25 | V |
| $V_{PP}$ | Programming Supply Voltage | | 12.2 | 13.0 | 13.3 | V |
| $t_{FR}$ | Input Rise, Fall Time | | 5 | | | ns |
| $V_{IL}$ | Input Low Voltage | | | 0.0 | 0.45 | V |
| $V_{IH}$ | Input High Voltage | | 2.4 | 4.0 | | V |
| $t_{IN}$ | Input Timing Reference Voltage | | 0.8 | 1.5 | 2.0 | V |
| $t_{OUT}$ | Output Timing Reference Voltage | | 0.8 | 1.5 | 2.0 | V |

## Programming Waveforms (Note 3)

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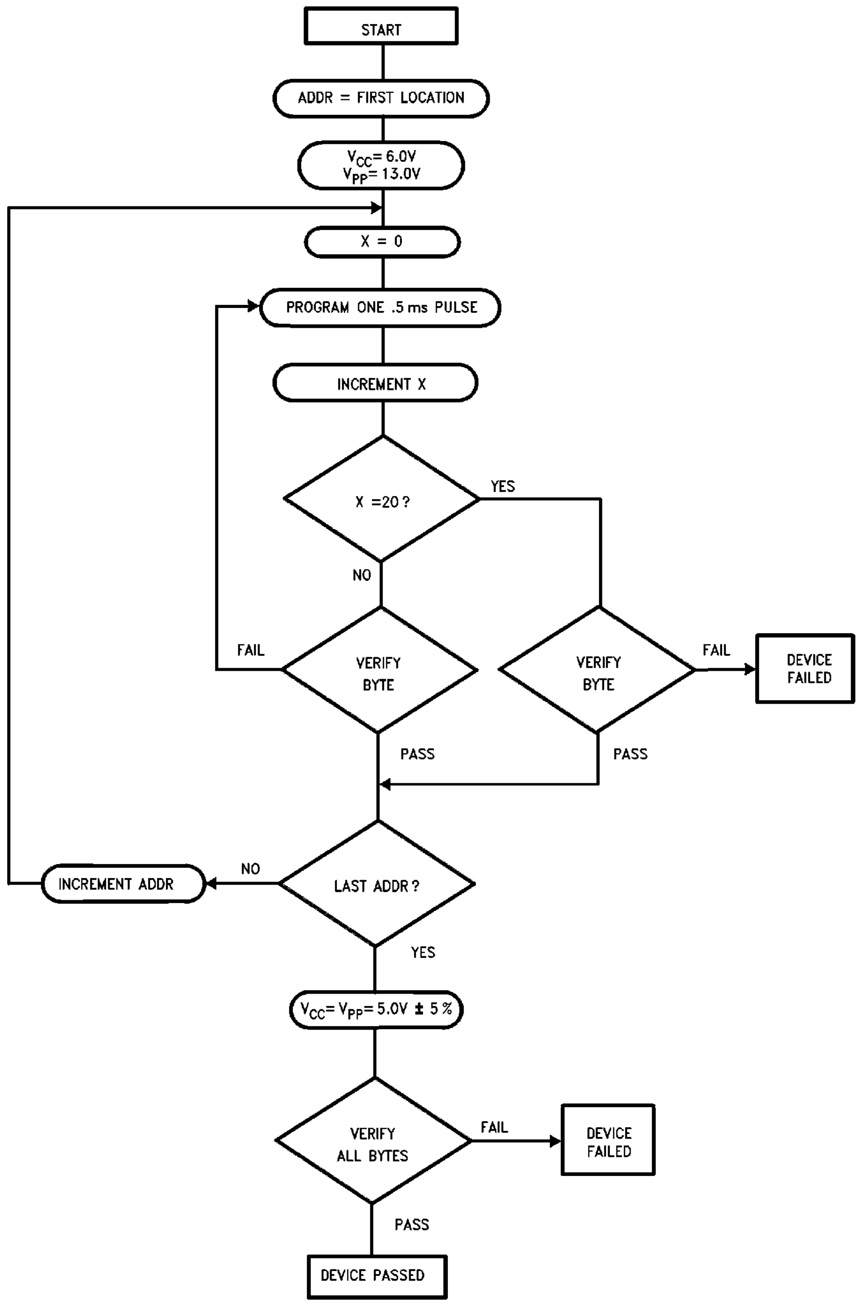
**Note 1:** National's standard product warranty applies to devices programmed to specifications described herein.

**Note 2:** $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$. The EPROM must not be inserted into or removed from a board with voltage applied to $V_{PP}$ or $V_{CC}$.

**Note 3:** The maximum absolute allowable voltage which may be applied to the $V_{PP}$ pin during programming is 14V. Care must be taken when switching the $V_{PP}$ supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 $\mu$F capacitor is required across $V_{PP}$, $V_{CC}$ to GND to suppress spurious voltage transients which may damage the device.

**Note 4:** Programming and program verify are tested with the interactive Program Algorithm, at typical power supply voltages and timings.

## Interactive Programming Algorithm Flow Chart

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## Functional Description

### DEVICE OPERATION

The six modes of operation of the NMC27C64 are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are $V_{CC}$ and $V_{PP}$. The $V_{PP}$ power supply must be at 13.0V during the three programming modes, and must be at 5V in the other three modes. The $V_{CC}$ power supply must be at 6V during the three programming modes, and at 5V in the other three modes.

### Read Mode

The NMC27C64 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. The programming pin ($\overline{PGM}$) should be at $V_{IH}$ except during programming. Assuming that addresses are stable, address access time ($t_{ACC}$) is equal to the delay from $\overline{CE}$ to output ($t_{CE}$). Data is available at the outputs $t_{OE}$ after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. $V_{CC}$ should therefore be maintained at operating voltage during read and verify. If $V_{CC}$ temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

### Standby Mode

The NMC27C64 has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27C64 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

### Output OR-Tying

Because NMC27C64s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

### Programming

CAUTION: Exceeding 14V on pin 1 ($V_{PP}$) will damage the NMC27C64.

Initially, all bits of the NMC27C64 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. A "0" cannot be changed to a "1" once the bit has been programmed.

The NMC27C64 is in the programming mode when the $V_{PP}$ power supply is at 13.0V and $\overline{OE}$ is at $V_{IH}$. It is required that at least a 0.1 $\mu$F capacitor be placed across $V_{PP}$, $V_{CC}$ to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{CE}$ should be kept TTL low at all times while $V_{PP}$ is kept at 13.0V.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C64 is designed to be programmed with interactive programming, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). The NMC27C64 must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple NMC27C64s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C64s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled NMC27C64s. If an application requires erasing and reprogramming, the NMC27C64Q UV erasable PROM in a windowed package should be used.

**TABLE I. Mode Selection**

| Pins / Mode | $\overline{CE}$ (20) | $\overline{OE}$ (22) | $\overline{PGM}$ (27) | $V_{PP}$ (1) | $V_{CC}$ (28) | Outputs (11–13, 15–19) |
|---|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | 5V | 5V | $D_{OUT}$ |
| Standby | $V_{IH}$ | Don't Care | Don't Care | 5V | 5V | Hi-Z |
| Output Disable | Don't Care | $V_{IH}$ | $V_{IH}$ | 5V | 5V | Hi-Z |
| Program | $V_{IL}$ | $V_{IH}$ | | 13V | 6V | $D_{IN}$ |
| Program Verify | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | 13V | 6V | $D_{OUT}$ |
| Program Inhibit | $V_{IH}$ | Don't Care | Don't Care | 13V | 6V | Hi-Z |

## Functional Description (Continued)

### Program Inhibit

Programming multiple NMC27C64s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel NMC27C64 may be common. A TTL low level program pulse applied to an NMC27C64's PGM input with $\overline{CE}$ at $V_{IL}$ and $V_{PP}$ at 13.0V will program that NMC27C64. A TTL high level $\overline{CE}$ input inhibits the other NMC27C64s from being programmed.

### Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with $V_{PP}$ at 13.0V. $V_{PP}$ must be at $V_{CC}$, except during programming and program verify.

### MANUFACTURER'S IDENTIFICATION CODE

The NMC27C64 has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C64 is "8FC2", where "8F" designates that it is made by National Semiconductor, and "C2" designates a 64k part.

The code is accessed by applying 12V $\pm$ 0.5V to address pin A9. Addresses A1–A8, A10–A12, $\overline{CE}$, and $\overline{OE}$ are held at $V_{IL}$. Address A0 is held at $V_{IL}$ for the manufacturer's code, and at $V_{IH}$ for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C $\pm$ 5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in a EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

### ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C64 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

After programming, opaque labels should be placed over the NMC27C64's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C64 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm$^2$.

The NMC27C64 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C64 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

### SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, $I_{CC}$, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated $V_{CC}$ transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 $\mu$F ceramic capacitor be used on every device between $V_{CC}$ and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 $\mu$F bulk electrolytic capacitor should be used between $V_{CC}$ and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

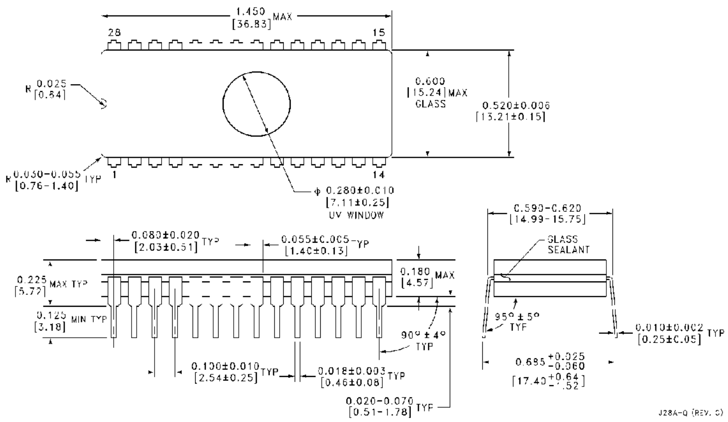
**TABLE II. Manufacturer's Identification Code**

| Pins | $A_0$ (10) | $O_7$ (19) | $O_6$ (18) | $O_5$ (17) | $O_4$ (16) | $O_3$ (15) | $O_2$ (13) | $O_1$ (12) | $O_0$ (11) | Hex Data |
|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer Code | $V_{IL}$ | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 8F |
| Device Code | $V_{IH}$ | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | C2 |

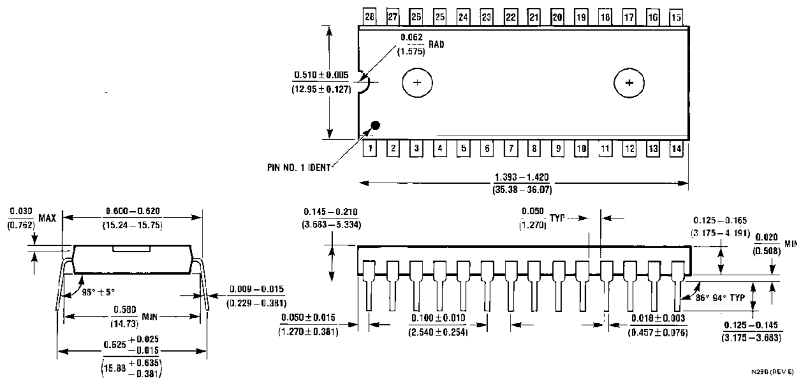
**TABLE III. Minimum NMC27C64 Erasure Time**

| Light Intensity (Micro-Watts/cm$^2$) | Erasure Time (Minutes) |
|---|---|
| 15,000 | 20 |
| 10,000 | 25 |
| 5,000 | 50 |

## Physical Dimensions inches (millimeters) unless otherwise noted




**Dual-In-Line Package (Q)**
**Order Number NMC27C64Q**
**NS Package Number J28AQ**




**Dual-In-Line Package (N)**
**Order Number NMC27C64N**
**NS Package Number N28B**

### LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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