查询TDA8202供应商 捷多邦，专业PCB打样工厂，24小时加急出货

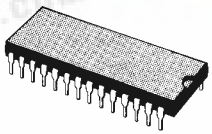
SGS-THOMSON MICROELECTRONICS

TDA8202

TV STEREO DECODER AND AUDIO PROCESSOR

ADVANCE DATA

- IDENTIFICATION OF TRANSMISSION MODE (mono/stereo/bilingual)
- DEMATRIXING OF THE STEREO AUDIO SIGNAL, WITH AN INTERNAL PROGRAMMABLE S-BUS NETWORK FOR MINIMAL CROSS-TALK
- DE-EMPHASIS OF THE AUDIO SIGNAL WITHOUT EXTERNAL COMPONENTS
- FILTERS FOR PSEUDOSTEREO AND ENLARGED STEREO BASE SPECIAL EFFECTS
- MONOPHONIC INPUT FOR MULTISTANDARD APPLICATIONS
- STEREO INPUT/OUTPUT FOR VCR
- VOLUME AND BALANCE CONTROL FOR LOUDSPEAKER OUTPUT
- ALL FUNCTION PROGRAMMABLE THROUGH USE OF S-BUS



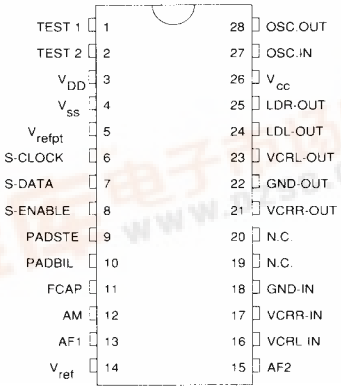
DIP28
(Plastic Package)

ORDER CODE : TDA8202

DESCRIPTION

The TDA8202 combines the functions of audio processor and lowcost stereo decoder for the European 2-carrier B/G system ; moreover, the device also includes input and a stereophonic output for reception of the audio signal coming from the SCART connector as well as a monophonic input for MULTISTANDARD applications (e.g., B/G and L).

PIN CONNECTION



E89TDA8202-01

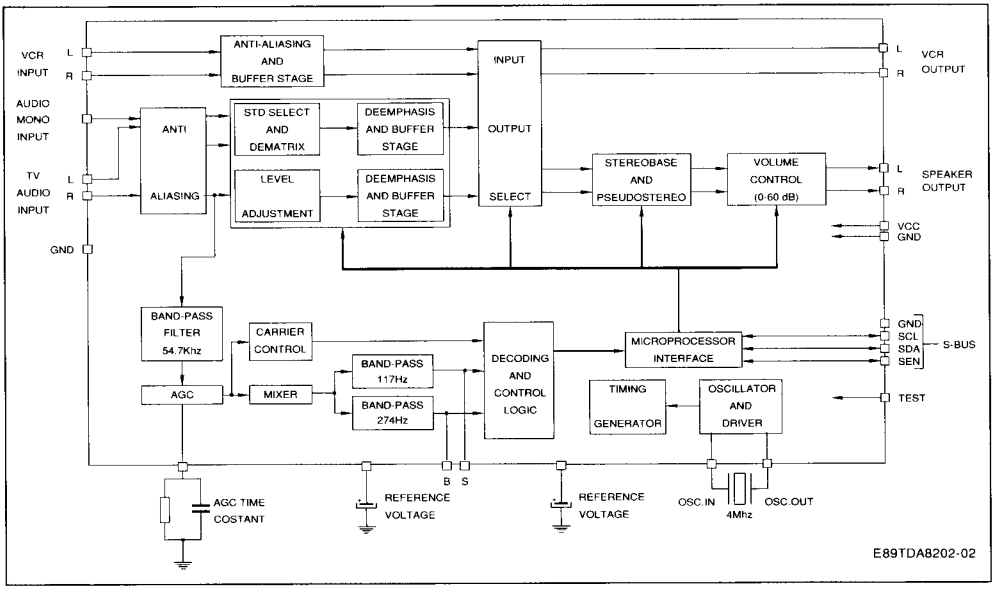
找PDF 维库一下 pdf.dzsc.com

This is advi development or undergoing evaluation. Details are subject to change without notice.

PIN DESCRIPTION

Pin	Function
1	Reserved for device testing, normally should be connected to mass.
2	Reserved for device testing, normally should be unconnected.
3	Power Voltage for Digital Part and Pilot Tone Vd = 8.5V
4	Mass for Digital Part and for Pilot Tone
5	Reference Voltage for Pilot Tone
6	SCL Clock Input for S-BUS
7	SDA Data Input for S-BUS
8	SEN Enable Input for S-BUS
9	Stereo Modulating Output (117Hz) for Pilot Tone
10	Bilingual Modulating Output (274Hz) for pilot Tone
11	Time Constant for AGC
12	Monophonic Input for Multistandard "AM"
13	Audio Input Signal from 5.5MHz Demodulator, AF1
14	Reference Voltage for Audio Part
15	Audio Input Signal from 5.74MHz Demodulator, AF2
16	Audio Input Signal from Right Channel of VCRR-IN Videotape Machine
17	Audio Input Signal from Left Channel of VCRL-IN Videotape Machine
18	Mass for Audio Input Signal
19	Not Connected
20	Not Connected
21	Audio Output Signal from Right Channel of VCRR-OUT Videotape Machine
22	Mass for Audio Output Signal
23	Audio Output Signal from Left Channel of VCRL-OUT Videotape Machine
24	Audio Output Signal from Right Channel of LDR-OUT Loudspeakers
25	Audio Output Signal from Left Channel of LDL-OUT Loudspeakers
26	Input Voltage for Analog Part Va = 8.5V
27	Oscillator Input at 4MHz
28	Oscillator Output at 4MHz

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The device is made up of 5 main sections :

1 S-BUS interface
2 Oscillator and power on reset
3 Pilot tone decoder
4 Dematrixing and de-emphasis of the audio signal
5 Reception of the audio signal

1) S-BUS INTERFACE

All of the TDA8202 functions are activated by microprocessors, using a 3-wire serial bus (SCL, SDA, SEN). For further information, see the software section.

2) OSCILLATOR AND POWER ON RESET

OSCILLATOR. The device functions with an external 4MHz crystal quartz connected to pins 27 and 28. A possible alternative is to connect pin 27 to an external 4MHz generator. If the clock frequency does not remain stable, there will be variations in the audio response and pilot tone decoding.

POWER ON RESET. About 120ms after V_{CC} power has reached the required level for correct device operation, the power on reset circuit signals correct operating status, using the RES bit in the RR register. For further information, see the software section.

3) PILOT TONE DECODING

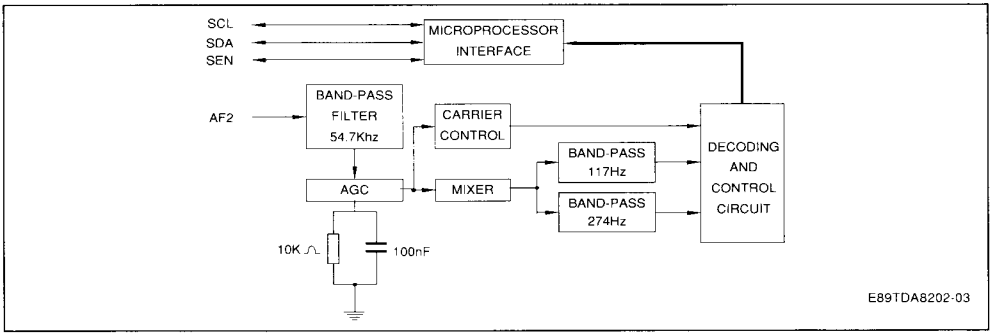
The pilot tone decoding section is used to identify the transmission mode (monophonic, stereophonic or bilingual) in B/G standard.

Figure 1 shows the block diagram for the circuit described hereafter :

The decoding signal goes through the pass-band filter at a frequency of 54.7kHz to the AF2 input in order to eliminate undesirable frequencies.

To guarantee a recognition range from 10 to 300mVeff for a carrier at 54.7kHz, the signal goes throught an AGC circuit the control velocity of which is based on pin 11's capacity. To be able to esta-blish transmission type, the signal is demodulated by the MIXER and filtered into the 117Hz (stereo transmission) and 274Hz (bilingual transmission) fixed frequencies. If, at the output of only one of the two filters, the signal is present, the "DECODING AND CONTROL CIRCUIT" block verifies if the carrier frequency is correct, using the "CARRIER CONTROL" block, and transmits the information to bits B and S of the RR register.

Figure 1 : Pilot Tone Decoder.



4) DEMATRIXING AND DE-EMPHASIS

DEMATRIXING. No external component is used for dematrixing the audio signal, but only a programmable attenuator throught S-BUS. Attenuation value must be set in calibration phase for the television set, and loaded every time the TV is turned on by the microprocessor in the R7 and R0 registers of the TDA8202.

Shown below is the dematrixing circuit which differentiates between the STEREO and BILINGUAL signals.

Figure 2 : Stereo Scheme.

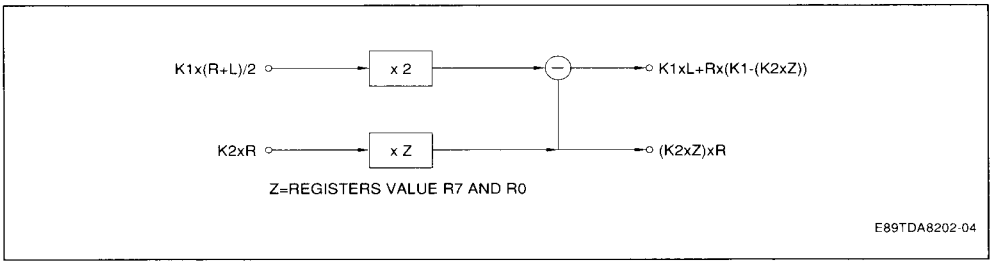
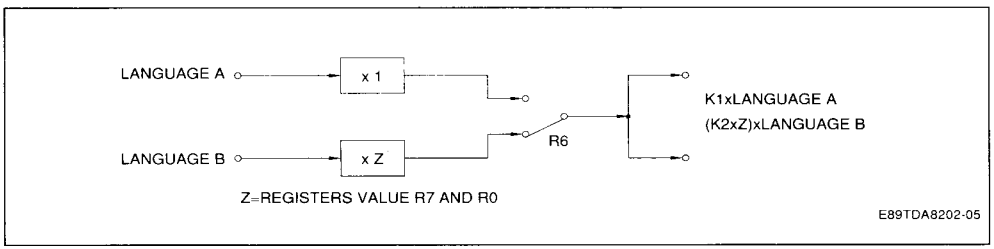


Figure 3 : Bilingual Scheme.



In both circuits, account is taken of the K1 and K2 constants which represent the removal of the AF1 and AF2 signals arriving from the FM demodulator in favor of the real AF1 and AF2 signals transmitted by the generator.

From the output equations can be deduced that, for K1 = K2x Z, can be obtained, based on precision of Z, the left (L) channel and the correct amplitude of the outputs for the STEREO signal, as well as for the BILINGUAL signals.

As far as the STEREO signal is concerned, a typical value of diaphony between left and right channels of 48dB can be guaranteed by a relationship between K1/K2 of 0.5 to 2, calculated in the following equation :

$$CT = 20*log[(K1/K2) /2E-9]$$

In the case of a BILINGUAL signal, a minimal difference in the signal ; between languages A and B of 0.05dB can be guaranteed by a relationship between K1 and K2 between 0.3 and 2, calculated with the following equation :

$$K(l-r) = 20*log\{(K1/K2) /[(K1/K2) + 2E-9]\}$$

DE-EMPHASIS. The de-emphasis of the AF1 and AF2 signals coming from the FM demodulator are carried out internally in the device without using external components.

5) AUDIO SIGNAL RECEPTION

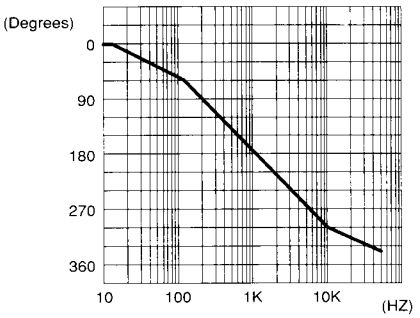
Audio signal reception is made up of three essential parts (see block diagram) :

a) INPUT OUTPUT SELECT. This circuit deals with shunting the signal coming from the three inputs (VCR, MONO, TV) into the two outputs (VCR, SPEAKER) in the modes described by the 5 bits S0-S4 in the R6 register. Information on possible configuration is detailed in the software section.

b) ENLARGED STEREO BASE AND PSEUDO-STEREO. The special effects function only for the loudspeaker output, and are activated by the PS and ES bits of R6. Operation is as follows :

- **PSEUDOSTEREO**, activated by the PS bit, is used with monophonic signals, and consists in the movement of the right channel phase toward the left, on the basis of the frequency as described in figure 4.
- **ENLARGED STEREO BASE**, activated by the ES bit, is used for stereophonic signals, and the function is that of making the stereo effect evident, even when the distance between the loudspeakers is reduced. For that purpose, diaphony is introduced in opposition to the right phase and vice versa. The extent of the diaphony to be introduced depends on the distance between the loudspeakers ; in the TDA8202, the diaphony is in the range of 50%.

Figure 4 : Right Channel Phase.



c) VOLUME CONTROL. The loudspeaker output also has a circuit to control and balance volume, carried out by two logarithmic attenuators of 2dB a spet with a maximum attenuation value of 60dB. The attenuation depends on the configuration of the 5 bits, CS1-CS5 of R3 for the left channel and the 5 bits, CD1-CD5 of R4 for the right channel ; the values in dB are shown in table N. 3 shown in the software section.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V28	Analog. Supply Voltage	Max 10	V
Vi	Input Voltage (all input)	– 0.3 to Vs + 0.3	V
Ii	Input Current (all input)	Max 5	mA
Io	Output Current (all output)	Max 10	mA
Tstg	Storage Temperature	– 25 to 125	°C

ELECTRICAL CHARACTERISTICS

Refer to the test circuit, Vs = 8.5V, Tamb = 25°C, without special effects, unless otherwise specified.

DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vs	Suppply Voltage	8	8.5	9	V
Is	Supply Current		30		mA
SVR	Supply Voltage Rejection (Fripple = 100Hz)		35		dB

AUDIO INPUT CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vin	Voltage Amplitude on all Inputs		1		Vrms
n	Amplitude Ratio between AF1/AF2	0.5		2	
Rin	Resistance on all Audio Inputs	10	40		kΩ

VOLUME CONTROL CHARACTERISTICS

Speaker

Symbol	Parameter	Min.	Typ.	Max.	Unit
KV	Volume Control Range ; Kvmax/Kvmin		60		dB
KVmin	Attenuator Resolution/step		2		dB
Ke	Tracking Error KV = 0 to 60dB		± 1	± 2	dB
KB	Balance Control Range ; KV = 0dB		60		dB

SPECIAL EFFECT CHARACTERISTICS

Pseudostereo

Symbol	Parameter	Min.	Typ.	Max.	Unit
Psh	Phase Shifter Response at : 100HZ 1kHZ 10kHZ		0 180 360		Deg Deg Deg
K(l-r)	Amplitude Tracking Error between Left and Right Channels (KV = 0dB)		± 0.5	± 1	dB

Enlarged Stereo Base

Symbol	Parameter	Min.	Typ.	Max.	Unit
K(l-r)	Amplitude Tracking Error between Left and Right Channel (KV = 0dB)		± 0.5	± 1	dB

DE-EMPHASIS CHARACTERISTICS (active only in AF1/AF2 input)

Symbol	Parameter	Min.	Typ.	Max.	Unit
td	Time Constant	45	50	55	µs

ELECTRICAL CHARACTERISTICS (continued)

AUDIO OUTPUT CHARACTERISTICS

Symbol	Parameter		Min.	Typ.	Max.	Unit
Vo	Audio Output Voltage Amplitude (THD ≤ 1%, all outputs)			Vin		Vrms
Kmax	Max Gain at Min. Attenuation (all outputs)		− 1	0	+ 1	dB
K(l-r)	Gain Tolerance between Left and Right Channel at Min. Attenuation (speaker K = 0dB)			± 0.5	± 1	dB
Ro	Resistance on all Audio Output				1	kΩ
R_l	Load Resistance (all outputs) Note : all outputs are short circuit protected.		5			kΩ
C_l	Load Capacitance (all outputs)				2	nF
AT	Muting Attenuation (all outputs)		70	80		dB
En	Output Noise Voltage (CCIR 468-2)					
	VCR Input					
	OUTPUT					
	Loudspeaker	KV = 0dB		100	200	µV
		KV = 40dB		50	100	µV
	VCR			100	200	µV
	AM Input					
	OUTPUT					
	Loudspeaker	KV = 0dB		100	200	µV
		KV = 40dB		50	100	µV
	VCR			100	200	µV
	AF1/AF2 Input					
	OUTPUT					
	Loudspeaker	KV = 0dB		200	300	µV
		KV = 40dB		50	100	µV
	VCR			200	300	µV
S/N	Signal to Noise Ratio (CCIR 468-2)					
	VCR Input : (Vi = 1Vrms, Fi = 1kHz)					
	OUTPUT					
	Loudspeaker	KV = 0dB	75	80		dB
		KV = 40dB	35	45		dB
	VCR		75	80		dB
	AM Input : (Vi = 1Vrms, Fi = 1kHz)					
	OUTPUT					
	Loudspeaker	KV = 0dB	75	80		dB
		KV = 40dB	35	45		dB
	VCR		75	80		dB
	AF1/AF2 Input Bilingual : (Vi = 1Vrms, Fi = 1kHz)					
	OUTPUT					
	Loudspeaker	KV = 0dB	70	75		dB
		KV = 40dB	35	45		dB
	VCR		70	75		dB

ELECTRICAL CHARACTERISTICS (continued)

AUDIO OUTPUT CHARACTERISTICS (continued)

Symbol	Parameter		Min.	Typ.	Max.	Unit
d	Total Harmonic Distortion					
	VCR Input : (Vi = 1Vrms, Fi = 1kHz)					
	OUTPUT					
	Loudspeaker	KV = 0dB		0.2	0.4	%
	VCR			0.2	0.4	%
	AM Input : (Vi = 1Vrms, Fi = 1kHz)					
	OUTPUT					
	Loudspeaker	KV = 0dB		0.2	0.4	%
	VCR			0.2	0.4	%
	AF1/AF2 Input Bilingual : (Vi = 1Vrms, Fi = 1kHz)					
	OUTPUT					
	Loudspeaker	KV = 0dB		0.2	0.4	%
	VCR			0.2	0.4	%
CT	Crosstalk between Left and Right Channel					
	(Vi = 1Vrms, Fi = 50Hz ÷ 15kHz, Bw = 10Hz)					
	VCR Input Stereo :					
	OUTPUT					
	Loudspeaker	KV = 0dB	70	80		dB
		KV = 20dB	60	70		dB
	VCR		70	80		dB
	AF1/AF2 Input Stereo :					
	OUTPUT					
	Loudspeaker	KV = 0dB	70	80		dB
		KV = 20dB	60	70		dB
	VCR		70	80		dB
CTb	Bilingual Crosstalk					
	(Vi = 1Vrms, Fi = 50Hz ÷ 15kHz, Bw = 10Hz)					
	VCR Input Bilingual :					
	OUTPUT					
	Loudspeaker	KV = 0dB	75	85		dB
		KV = 20dB	75	85		dB
	AF1/AF2 Input Bilingual :					
	OUTPUT					
	Loudspeaker	KV = 0dB	70	80		dB
		KV = 20dB	70	80		dB
CTI	Crosstalk between VCR and TV Section		70	80		dB

S-BUS CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vil	Input Voltage Low Level	Vss		0.8	V
Vih	Input Voltage High Level	2		VDD	V
Iil-ih	Input Current			1	µA
Iol	Output Low Current Capability (Vol = 0.45V)	5			mA
Ioh	Leakage Output Current (Vo = 5.25V, output off, Vs = 8.5V)			10	µA

SGS-THOMSON MICROELECTRONICS

ELECTRICAL CHARACTERISTICS (continued)

PILOT TONE CHARACTERISTICS V1 = 50mVrms, m = 0.5, unless otherwise specified.

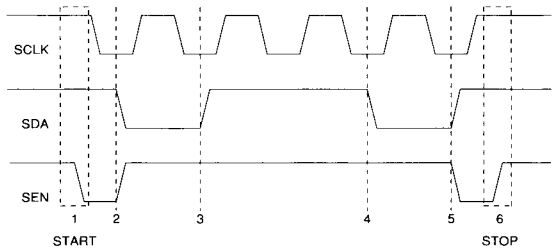
Symbol	Parameter	Min.	Typ.	Max.	Unit
V1	Input Voltage Amplitude (without AM modulation)	10		300	mVrms
dfp	Frequency Range of Carrier to 54687.5Hz		± 1		kHz
dfs	Frequency Range of Stereo Filter (117.4Hz)		± 3		Hz
dft	Frequency Range of Bilingual Filter (274Hz)		± 6		Hz
dm	Range of AM Modulation Index	40	50	60	%

SOFTWARE INFORMATIONS

S-BUS DESCRIPTION

Shown below is the timing diagram of the S-BUS protocol :

Figure 5 : S-BUS Timing Diagram.



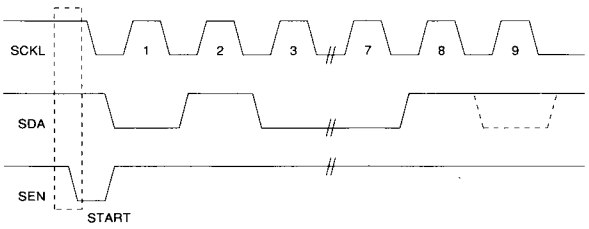
The START/STOP conditions (points 1 and 6) occur only by a transmission of SEN wire (10 and 01 respectively) while the SCL wire is in high state (1).

During transmission, the SDA wire can change only when SCL wire is in low state (points 2, 3, 4, 5). After START condition (point 1), the SEN wire must change to high state (point 2) and it remains in this condition for the whole transmission.

At the end of transmission (point 5), the SDA wire change to high state and in the mean time, the SEN wire must go to low state and then it returns to high state to generate the STOP condition (point 6).

After the transmission of each byte (composed of 8 bits), there is an ACKNOWLEDGE bit appointed by a high state on SDA wire generated by the transmitter. The device that acknowledges, forces to low state the SDA wire during the time of the acknowledge clock pulse, as described in figure 6 :

Figure 6 : Acknowledge Bit.



In normal conditions, the addressed device must acknowledge after each byte received. If the SDA wire, during the 9th pulse, remains in high state, the master-transmitter can generate the STOP condition to abort the transfer.

Interface between the microprocessor and the TDA8202 occurs through use of the following protocol :

- a start condition (START) see figure 7 and 8
- an address byte, containing the address reserved for the TDA8202 (1000000x) and the bus transmission direction (this information is located in the byte's 8th bit, in which "0" indicates a write, and "1", a read, by the microprocessor). At the end of each byte, the TDA8202 must give the ACKNOWLEDGE signal
- a byte for addressing the registers in write, or the content of register RR in a read
- a third byte containing the information to be written on the register
- a stop condition (STOP)

Figure 7 : Write Protocol Example.

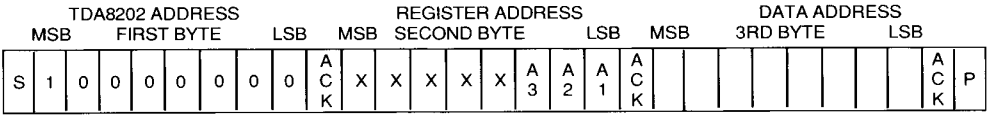


Figure 8 : Read Protocol Example.

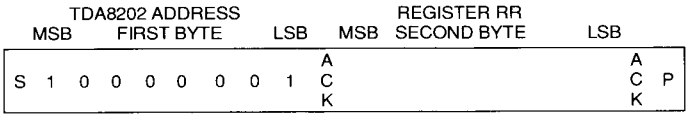
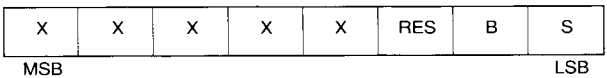


Table 1 : TDA8202 Register Address.

Register Name	Address			Content	Type of Operation
	A3	A2	A1		
R0	0	0	0	Dematrixing and Muting	WRITE ONLY
R3	0	1	1	Left Speaker Volume Channel (60dB)	WRITE ONLY
R4	1	0	0	Right Speaker Volume Channel (60dB)	WRITE ONLY
R6	1	1	0	Configuration Switch and Special Effects	WRITE ONLY
R7	1	1	1	Dematrixing	WRITE ONLY
RR				Transmission Conditions and Power on Reset	READ ONLY

REGISTER CONTENTS

RR REGISTER : (Transmission conditions and power on reset)



B = Bilingual transmission (active at "1")
S = Stereo transmission (active at "1")
RES = Power on reset (active at "1")
X = Not used

RES

The RES bit in RR register is set to "1" every time that the supply voltage falls under the minimum level required for the correct operation of TDA8202. In this case the device automatically inserts the muting on the outputs (R0, ML and MV ; R3 and R4 are both at "1"), and resets bits B and S in RR to "0".

The microprocessor must verify this situation and when the RES bit returns to "0", it initializes the registers to the desired audio status.

B and S

B and S are the bits reserved to identify the transmission type in B/G standard. If both bits are at "0", the transmission is MONO, while if only one bit is at "1", the transmission is STEREO (S at "1") or BILINGUAL (B at "1").

REGISTER R0 : (Dematrixing and muting)

X	X	X	TS	X	MV	A8	A9

MSB LSB

REGISTER R7 : (Dematrixing)

A0	A1	A2	A3	A4	A5	A6	A7

MSB LSB

TS = Testing bit (active at "1")
MV = VCR muting (active at "1")

A0-A9 = Dematrixing (active at "1")
X = Not used

A0-A9

Bits from A0 to A9 represents the values of the attenuator Z shown in figure 2 and 3. Below is listed the value of every bits when it is in the active state :

$A0 = 2^{0}$ $A1 = 2^{-1}$ $A2 = 2^{-2}$ $A3 = 2^{-3}$ $A4 = 2^{-4}$
$A5 = 2^{-5}$ $A6 = 2^{-6}$ $A7 = 2^{-7}$ $A8 = 2^{-8}$ $A9 = 2^{-9}$

With the following formula it is possible to calculate the value of the attenuator Z :

$$Z = \sum_{n=0}^{n=9} A^n * 2^n$$

Table 2 : Example Table.

	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	Z
Minimum	0	1	0	0	0	0	0	0	0	0	0.5
Medium	1	0	0	0	0	0	0	0	0	0	1
Maximum	1	1	1	1	1	1	1	1	1	1	2

MV

Bit MV is the mute for the VCR output. To have the mute active it is necessary to put the bit to the level "1". At the switch on the device automatically set bit to "1" putting the output in mute ; so it is necessary to set it to "0" after every, switch on.

REGISTER R3 : (Left channel loudspeaker volume control)

X	X	X	CS5	CS4	CS3	CS2	CS1

MSB LSB

CS1-CS5 = Volume control
X = Not used

REGISTER R4 : (Right channel loudspeaker volume control)

X	X	X	CD5	CD4	CD3	CD2	CD1

MSB LSB

CD1-CD5 = Volume control
X = Not used

In the table below are listed the values of the attenuation in dB depending on the bits set in registers R3 and R4 :

Table 3 : Speaker Volume Table.

Binary Code MSB LSB	Attenuation dB
XXX00000	0
XXX00001	2
XXX00010	4
XXX00011	6
XXX00100	8
XXX00101	10
XXX00110	12
XXX00111	14
XXX01000	16
XXX01001	18
XXX01010	20
XXX01011	22
XXX01100	24
XXX01101	26
XXX01110	28
XXX01111	30
XXX10000	32
XXX10001	34
XXX10010	36
XXX10011	38
XXX10100	40
XXX10101	42
XXX10110	44
XXX10111	46
XXX11000	48
XXX11001	50
XXX11010	52
XXX11011	54
XXX11100	56
XXX11101	58
XXX11110	60
XXX11111	MUTE

REGISTER R6 : (Configuration switch and special effects)

X	S4	PS	ES	S3	S2	S1	S0
MSB							LSB

S0-S4 = Configuration switch

PS = Pseudostereo

ES = Enlarged stereo base

X = Not used

S0-S4

Bits from S0 to S4 are used to select the desired audio condition of TDA8202. The following table shows all the possible conditions :

Table 4 : Configuration Switch.

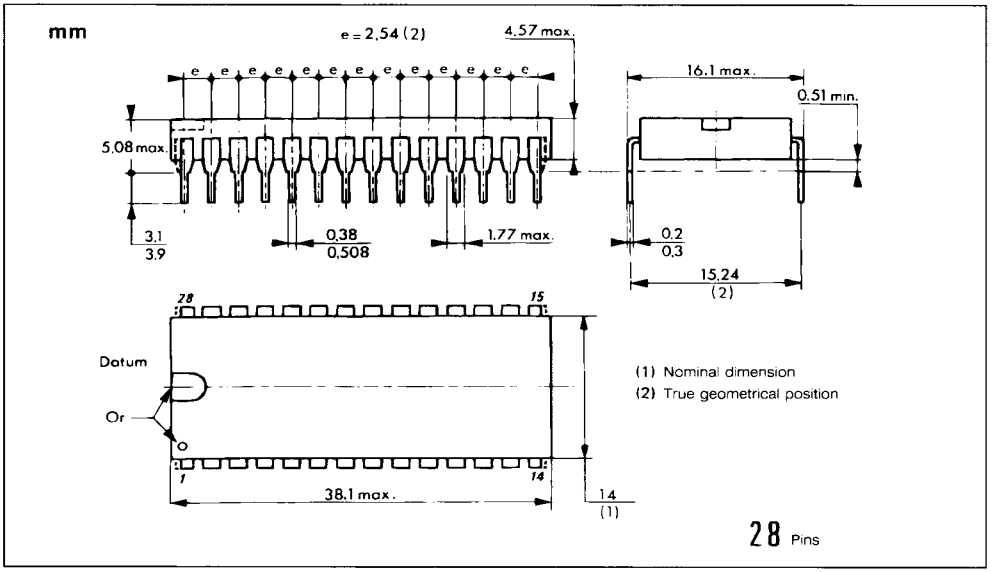
Selection Code S4 S0	AM Input	TV Input		VCR Input		VCR Output		Speaker Output	
		AF1	AF2	L	R	L	R	L	R
00000		$\frac{L+R}{2}$	R	L°	R°	L	R	L°	R°
00001		$\frac{L+R}{2}$	R	1°	2°	L	R	2°	2°
00010		$\frac{L+R}{2}$	R	1°	2°	L	R	1°	1°
00011		$\frac{L+R}{2}$	R			M*	M*	L	R
00100		$\frac{L+R}{2}$	R			L	R	L	R
00101		1	2			1	2	2	2
00110		1	2			1	2	1	1
00111		1	2			1	1	1	1
01000		1	2	L°	R°	1	2	L°	R°
01001		1	2	1°	2°	1	2	2°	2°
01010		1	2	1°	2°	1	2	1°	1°
01011		1	2	1°	2°	2	2	2	2
01100		M		L°	R°	M	M	L°	R°
01101		M		1°	2°	M	M	2°	2°
01110		M		1°	2°	M	M	1°	1°
01111		M				M	M	M	M
11100	AM			L°	R°	AM	AM	L°	R°
11101	AM			1°	2°	AM	AM	2°	2°
11110	AM			1°	2°	AM	AM	1°	1°
11111	AM					AM	AM	AM	AM
10001		$\frac{L+R}{2}$	R	L°	R°	L°	R°	L	R
10010		M		L°	R°	L°	R°	M	M
10011		1	2	L°	R°	L°	R°	1	1
10100		1	2	L°	R°	L°	R°	2	2
10101	AM			L°	R°	L°	R°	AM	AM
10110				L°	R°	L°	R°	L°	R°
10111				1°	2°	1°	2°	1°	1°
11000				1°	2°	1°	2°	2°	2°

Where :

M = monophonic standard TV signal B/G
M* = reconstructed monophonic signal starting from L and R
L = left standard TV B/G stereo signal
R = right standard TV B/G stereo signal
1 = bilingual B/G TV standard 1st language
2 = bilingual B/G TV standard 2nd language
L° = VCR stereo left signal
R° = VCR stereo right signal
1° = bilingual VCR 1st language
2° = bilingual VCR 2nd language
AM = monophonic standard L signal

PACKAGE MECHANICAL DATA

28 PINS – PLASTIC DIP



SGS-THOMSON MICROELECTRONICS