

59E D ■ 0257526 0032226 277 ■ AMD2

查询PAL16L8DCNL供应商

ADV MICRO PLA/PLE/ARRAYS

捷多邦 专业PCB打样工厂, 24小时加

急出货

COM'L: -4/5/7/D/B/B-2/A

MIL: -10/12/B/B-2/A/B-4



**Advanced
Micro
Devices**

PAL16R8 Family

20-Pin TTL Programmable Array Logic

T-46-19-13

DISTINCTIVE CHARACTERISTICS

- As fast as 4.5 ns maximum propagation delay
- Popular 20-pin architectures: 16L8, 16R8, 16R6, 16R4
- Programmable replacement for high-speed TTL logic
- Register preload for testability
- Power-up reset for initialization
- Extensive third-party software and programmer support through FusionPLD partners
- 20-pin DIP and PLCC packages save space
- 28-pin PLCC-4 package provides ultra-clean high-speed signals

GENERAL DESCRIPTION

The PAL16R8 Family (PAL16L8, PAL16R8, PAL16R6, PAL16R4) includes the PAL16R8-5/4 Series which provides the highest speed in the 20-pin TTL PAL device family, making the series ideal for high-performance applications. The PAL16R8 Family is provided with standard 20-pin DIP and PLCC pinouts and a 28-pin PLCC pinout. The 28-pin PLCC pinout contains seven extra ground pins interleaved between the outputs to reduce noise and increase speed.

The family utilizes Advanced Micro Devices' advanced trench-isolated bipolar process and fuse-link technology. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The family allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device

is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

In addition, the PAL device provides the following options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to Vcc or GND.

The entire PAL device family is supported by the FusionPLD partners. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. Once the PAL device is programmed and verified, an additional connection may be opened to prevent pattern readout. This feature secures proprietary circuits.

PRODUCT SELECTOR GUIDE

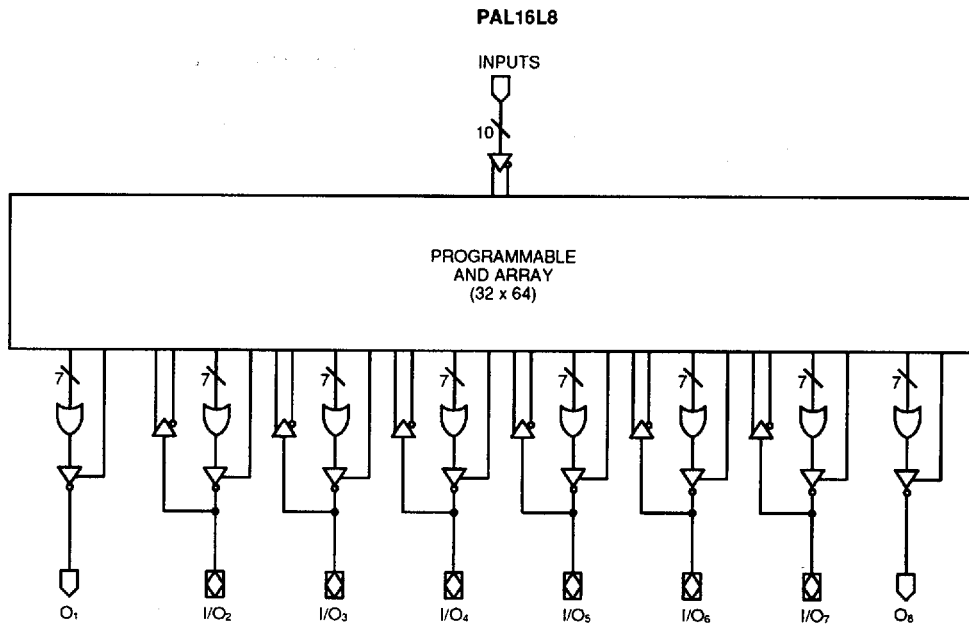
DEVICE	DEDICATED INPUTS	OUTPUTS	PRODUCT TERMS/ OUTPUT	FEEDBACK	ENABLE
PAL16L8	10	6 comb. 2 comb.	7 7	I/O -	prog. prog.
PAL16R8	8	8 reg.	8	reg.	pin
PAL16R6	8	6 reg. 2 comb.	8 7	reg. I/O	pin prog.
PAL16R4	8	4 reg. 4 comb.	8 7	reg. I/O	pin prog.



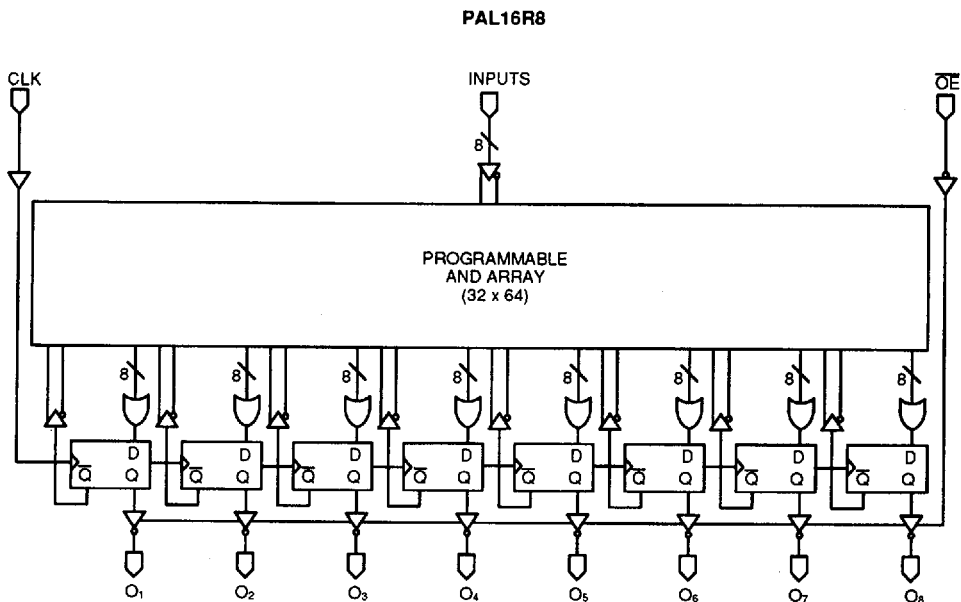


BLOCK DIAGRAMS

ADV MICRO PLA/PLE/ARRAYS



12468-004A

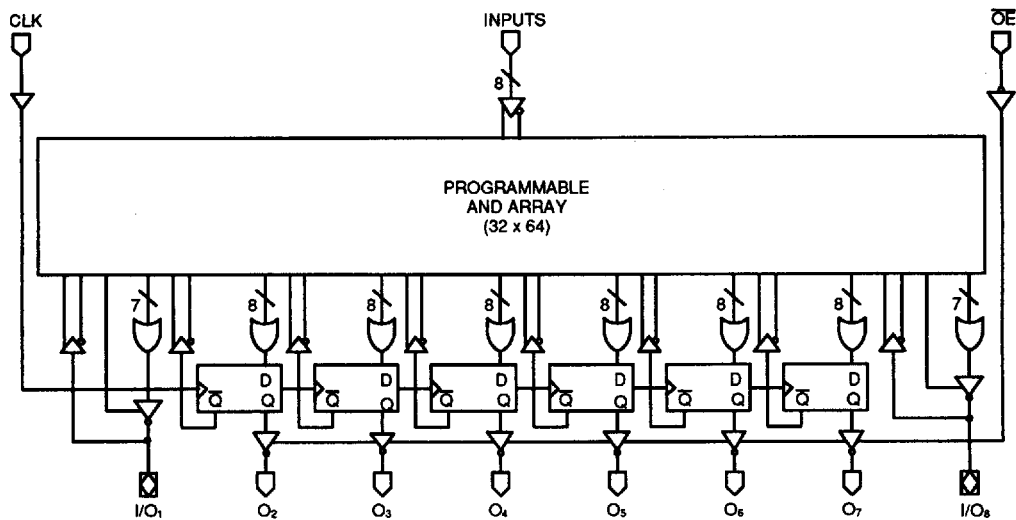


12468-001A

BLOCK DIAGRAMS

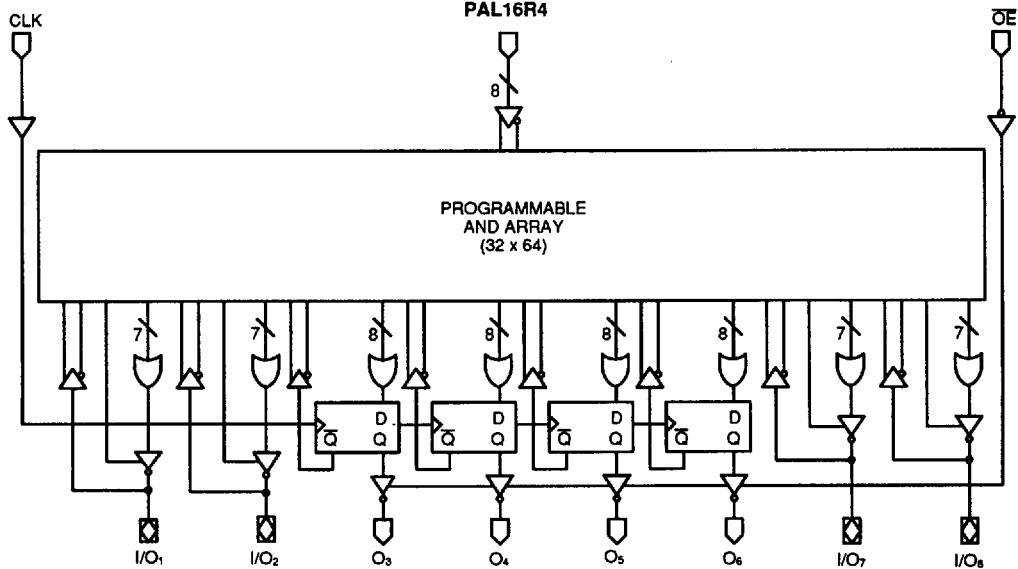
ADV MICRO PLA/PLE/ARRAYS

PAL16R6



12468-002A

PAL16R4



12468-003A

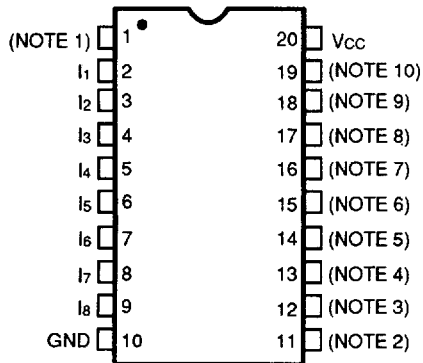


CONNECTION DIAGRAMS

ADV MICRO PLA/PLE/ARRAYS

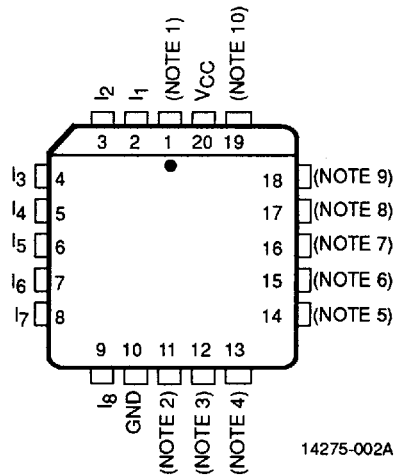
Top View

DIP



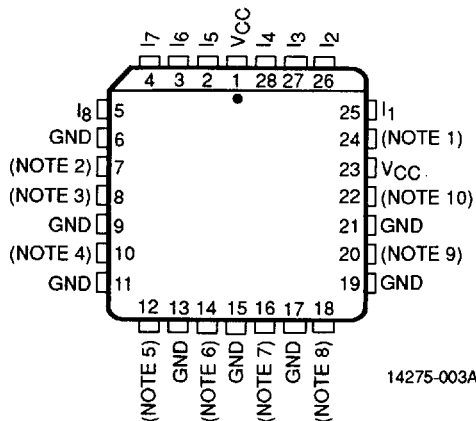
14275-001A

20-Pin PLCC



14275-002A

28-Pin PLCC



14275-003A

PIN DESIGNATIONS

CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
O	Output
OE	Output Enable
Vcc	Supply Voltage

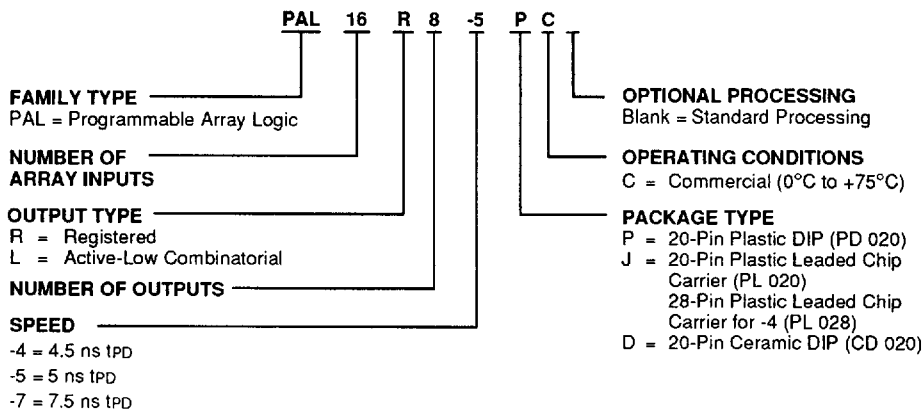
Note:

Pin 1 is marked for orientation.

Note	16L8	16R8	16R6	16R4
1	I ₀	CLK	CLK	CLK
2	I ₉	OE	OE	OE
3	O ₁	O ₁	I/O ₁	I/O ₁
4	I/O ₂	O ₂	O ₂	I/O ₂
5	I/O ₃	O ₃	O ₃	O ₃
6	I/O ₄	O ₄	O ₄	O ₄
7	I/O ₅	O ₅	O ₅	O ₅
8	I/O ₆	O ₆	O ₆	O ₆
9	I/O ₇	O ₇	O ₇	I/O ₇
10	O ₈	O ₈	I/O ₈	I/O ₈

ORDERING INFORMATION**Commercial Products**

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PAL16L8	-5PC, -5JC, -4JC
PAL16R8	
PAL16R6	
PAL16R4	
PAL16L8-7	PC, JC, DC
PAL16R8-7	
PAL16R6-7	
PAL16R4-7	

Valid Combinations

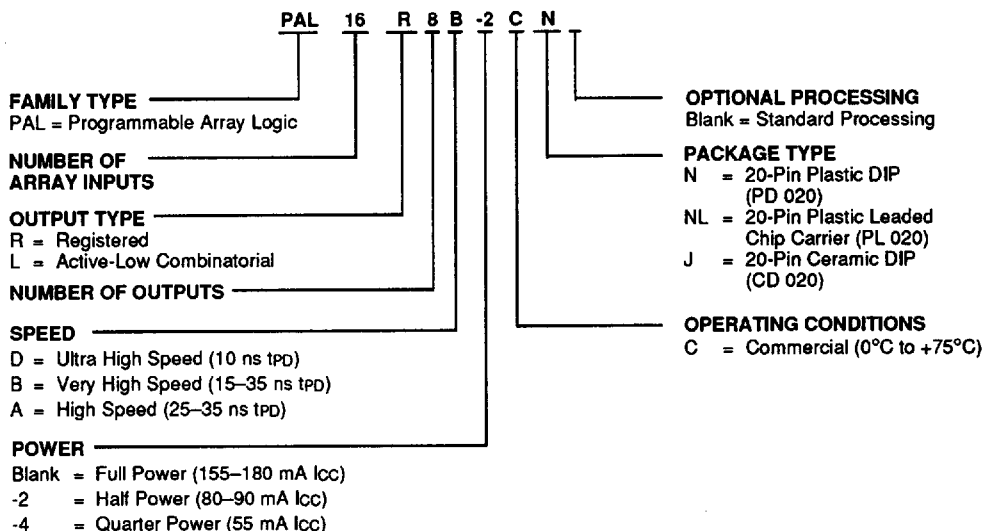
The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.



**ORDERING INFORMATION****Commercial Products (MMI Marking Only)**

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PAL16L8	D, B,	CN, CNL, CJ
PAL16R8	B-2, A,	
PAL16R6	B-4	
PAL16R4		

Valid Combinations

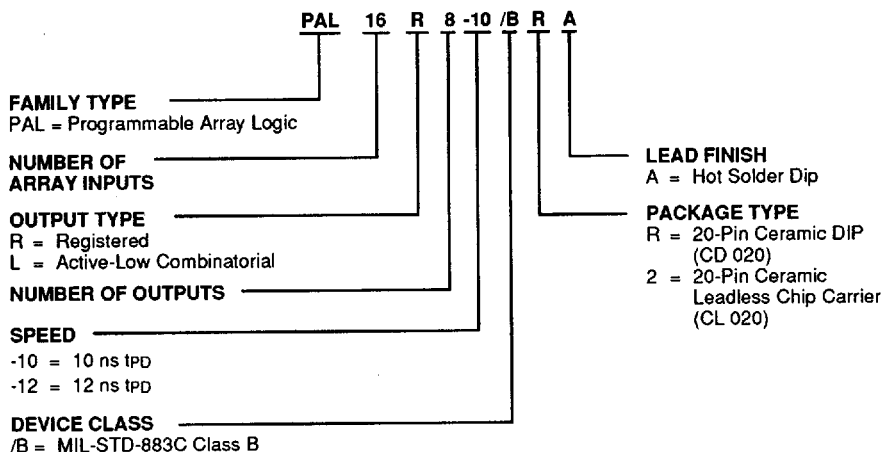
The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with MMI logo.



ORDERING INFORMATION**APL Products**

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PAL16L8	-10, -12	/BRA, /B2A
PAL16R8		
PAL16R6		
PAL16R4		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.





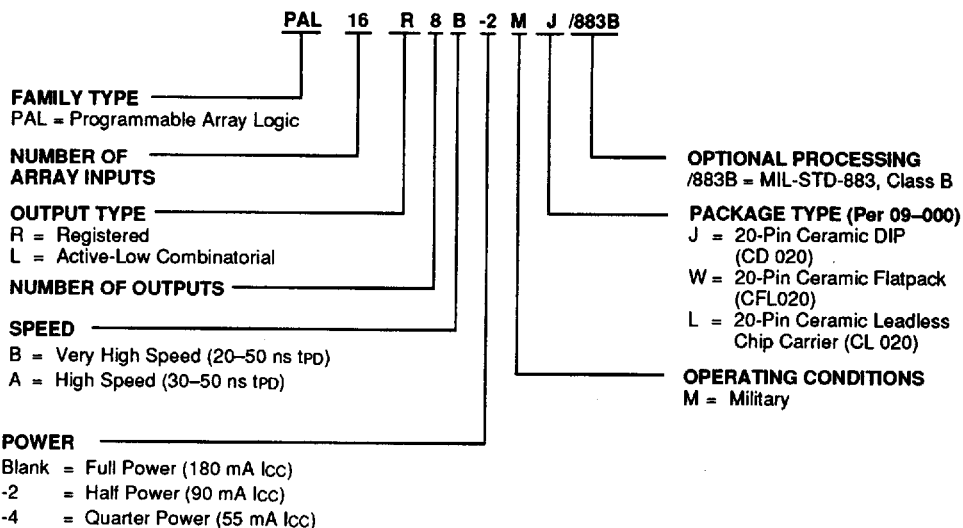
59E D ■ 0257526 0032233 407 ■ AMD2

ORDERING INFORMATION

ADV MICRO PLA/PLE/ARRAYS

APL Products (MMI Marking Only)

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PAL16L8	B, B-2,	MJ/883B,
PAL16R8	A, B-4	MW/883B,
PAL16R6		ML/883B
PAL16R4		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional information on AMD's Standard Military grade products.

Note: Marked with MMI logo.

Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

ADV MICRO PLA/PLE/ARRAYS

FUNCTIONAL DESCRIPTION**Standard 20-pin PAL Family**

The standard bipolar 20-pin PAL family devices have common electrical characteristics and programming procedures. Four different devices are available, including both registered and combinatorial devices. All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Pinouts

The PAL16R8 Family is available in the standard 20-pin DIP and PLCC pinouts and the PAL16R8-4 Series is available in the new 28-pin PLCC pinout. The 28-pin PLCC pinout gives the designer the cleanest possible signal with only 4.5 ns delay.

The PAL16R8-4 pinout has been designed to minimize the noise that can be generated by high-speed signals. Because of its inherently shorter leads, the PLCC package is the best package for use in high-speed designs. The short leads and multiple ground signals reduce the effective lead inductance, minimizing ground bounce. Placing the ground pins between the outputs optimizes the ground bounce protection, and also isolates the outputs from each other, eliminating cross-talk. This pinout can reduce the effective propagation delay by as much as 20% from a standard DIP pinout. Design files for PAL16R8-4 Series devices are written as if the device had a standard 20-pin DIP pinout for most design software packages.

Variable Input/Output Pin Ratio

The registered devices have eight dedicated input lines, and each combinatorial output is an I/O pin. The PAL16L8 has ten dedicated input lines and six of the eight combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to Vcc or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. On combinatorial outputs, a product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin and may be configured as a dedicated input if the output buffer is always disabled. On registered outputs, an input pin controls the enabling of the three-state outputs.

Registers with Feedback

Registered outputs are provided for data storage and synchronization. Registers are composed of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock input.

Register Preload

The register on the PAL16R8 Family can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL16R8 Family will be HIGH due to the active-low outputs. The Vcc rise must be monotonic and the reset delay time is 1000 ns maximum.

Security Fuse

After programming and verification, a PAL16R8 Family design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed.

Quality and Testability

The PAL16R8 Family offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The PAL16R8 Family is fabricated with AMD's advanced trench-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven TiW fuses for reliable operation.



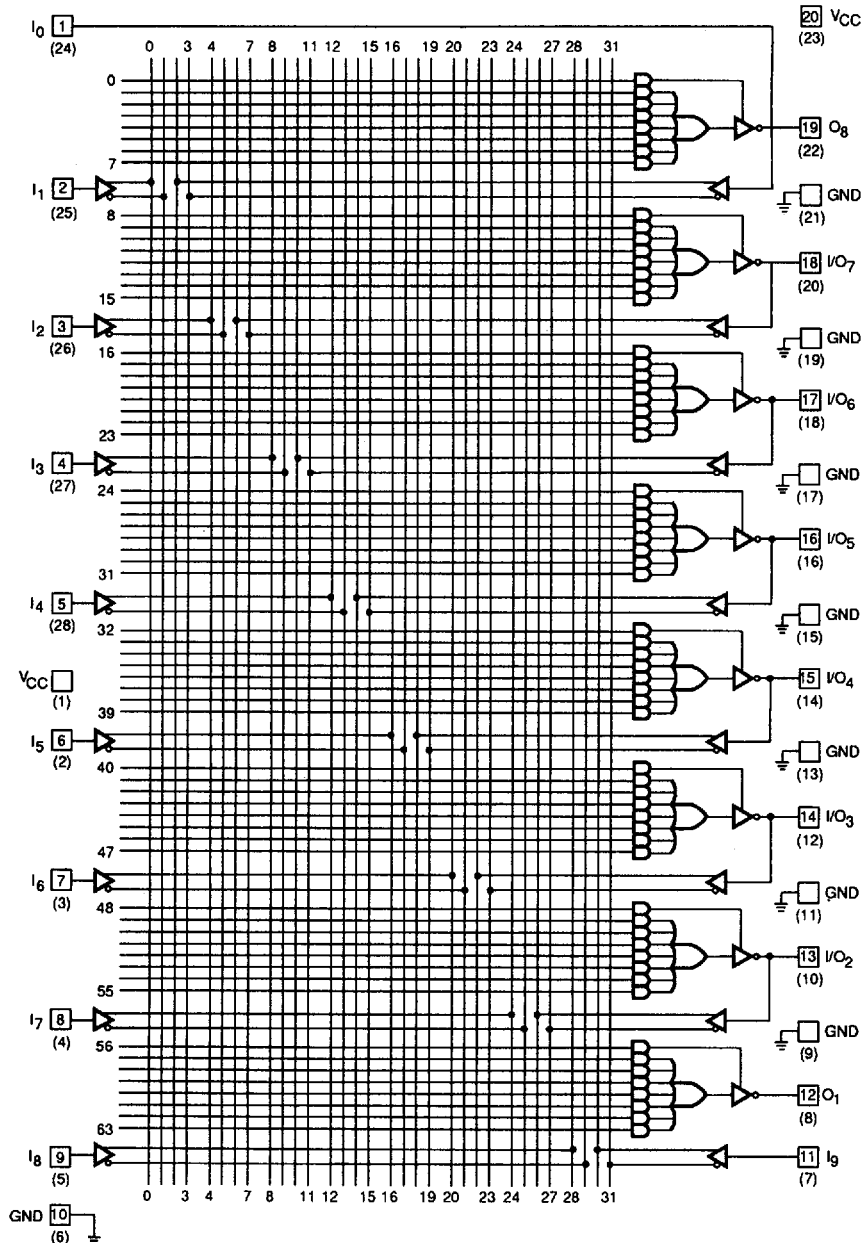


LOGIC DIAGRAM

ADV MICRO PLA/PLE/ARRAYS

DIP and 20-Pin PLCC (28-Pin PLCC) Pinouts

16L8 (-4)

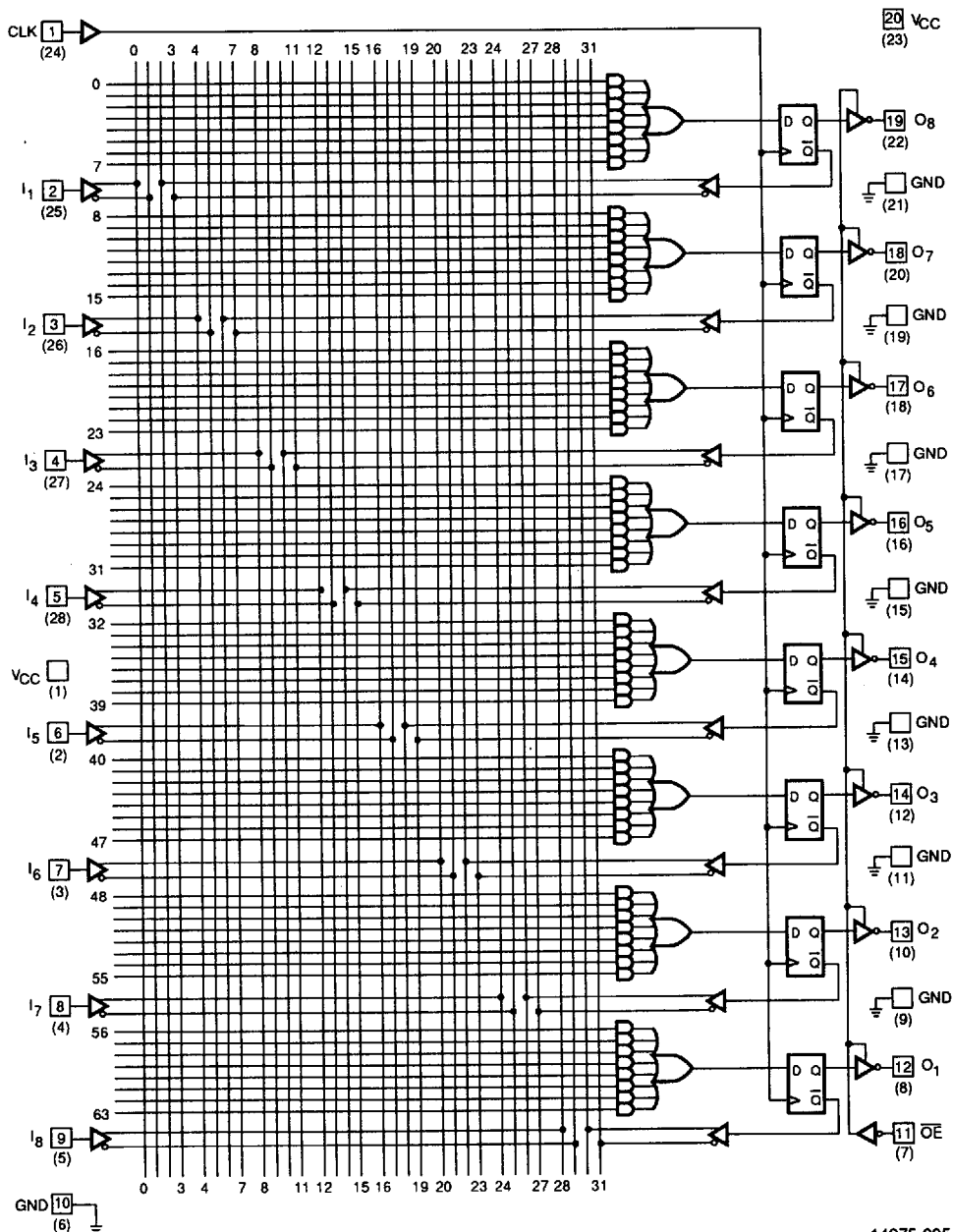


ADV MICRO PLA/PLE/ARRAYS

LOGIC DIAGRAM

DIP and 20-Pin PLCC (28-Pin PLCC) Pinouts

16R8 (-4)



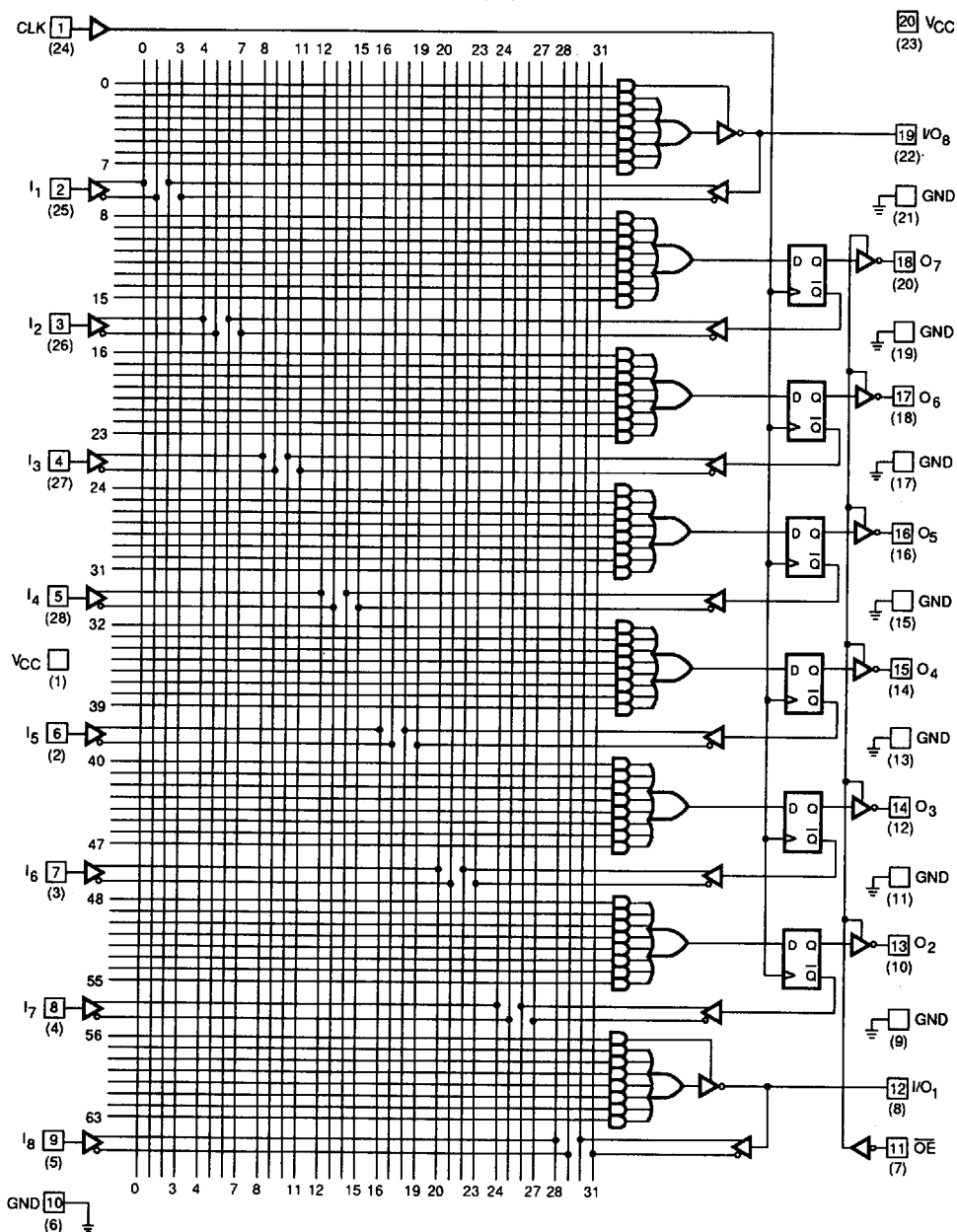


LOGIC DIAGRAM

ADV MICRO PLA/PLE/ARRAYS

DIP and 20-Pin PLCC (28-Pin PLCC) Pinouts

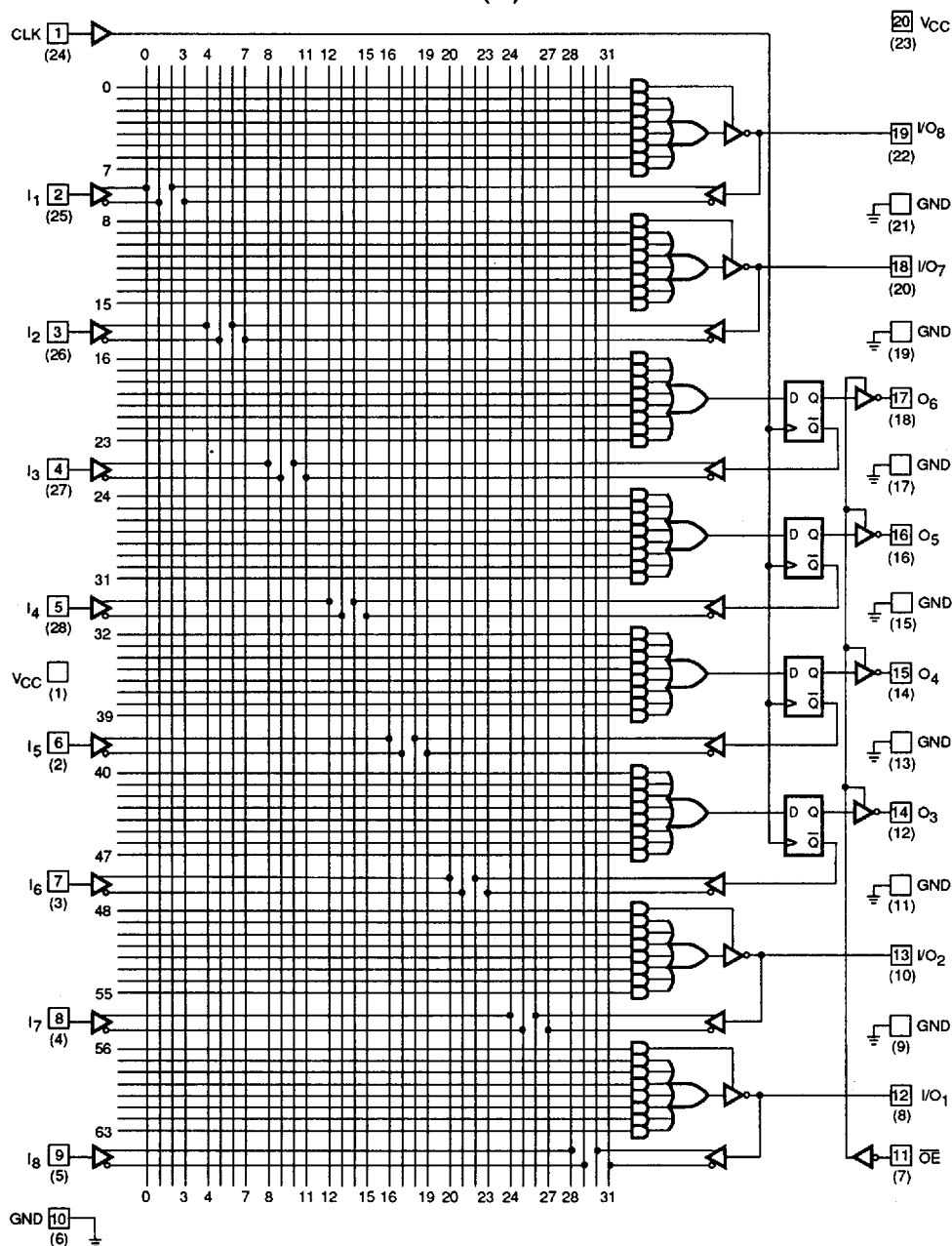
16R6 (-4)



LOGIC DIAGRAM

DIP and 20-Pin PLCC (28-Pin PLCC) Pinouts

16R4 (-4)





ADV MICRO PLA/PLE/ARRAYS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature with Power Applied	-65°C to +150°C
Storage Temperature	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.2 V to $V_{CC} + 0.5$ V
DC Input Current	-30 mA to +5 mA
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC} + 0.5$ V
Static Discharge Voltage	2001 V

OPERATING RANGES

Ambient Temperature (T_A)	0°C to +75°C
Operating in Free Air	
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.2$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min.}$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 24$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min.}$		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	$I_{IN} = -18$ mA, $V_{CC} = \text{Min.}$		-1.2	V
I_{IH}	Input HIGH Current	$V_{IN} = 2.7$ V, $V_{CC} = \text{Max.}$ (Note 2)		25	μ A
I_{IL}	Input LOW Current	$V_{IN} = 0.4$ V, $V_{CC} = \text{Max.}$ (Note 2)		-250	μ A
I_I	Maximum Input Current	$V_{IN} = 5.5$ V, $V_{CC} = \text{Max.}$		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.7$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		100	μ A
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		-100	μ A
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max.}$ (Note 3)	-30	-130	mA
I_{CC}	Supply Current	$V_{IN} = 0$ V, Outputs Open ($I_{OUT} = 0$ mA) $V_{CC} = \text{Max.}$		210	mA

Notes:

- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
- Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT} = 0.5$ V has been chosen to avoid test problems caused by tester ground degradation.



ADV MICRO PLA/PLE/ARRAYS

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C _{IN}	Input Capacitance CLK, \overline{OE} I ₁ –I ₈	V _{IN} = 2.0 V	V _{CC} = 5.0 V T _A = 25°C	8	pF
				5	
C _{OUT}	Output Capacitance	V _{OUT} = 2.0 V	f = 1 MHz	8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-5		-4		Unit	
				Min. (Note 3)	Max.	Min. (Note 3)	Max.		
tPD	Input or Feedback to Combinatorial Output			16L8, 16R8, 16R4	1	5	1	4.5	ns
ts	Setup Time from Input or Feedback to Clock			16R8, 16R6, 16R4	4.5		4.5		ns
tH	Hold Time				0		0		ns
tCO	Clock to Output				1	4.0	1	3.5	ns
tSKEWR	Skew Between Registered Outputs (Note 4)					1		0.5	ns
tWL	Clock Width	LOW			4		4		ns
tWH		HIGH			4		4		ns
fMAX	Maximum Frequency (Note 5)	External Feedback	1/(ts + tco)		117		125		MHz
		Internal Feedback (fCNT)			125		125		MHz
		No Feedback	1/(tWH + tWL)		125		125		MHz
tPZX	OE to Output Enable				1	6.5	1	6.5	ns
tPXZ	OE to Output Disable			1	5	1	5	ns	
tEA	Input to Output Enable Using Product Term Control			16L8, 16R6, 16R4	2	6.5	2	6.5	ns
tER	Input to Output Disable Using Product Term Control				2	5	2	5	ns

Notes:

- See Switching Test Circuit for test conditions.
- Delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are chosen based on two considerations: they must allow for the large number of variables that define "best case" conditions, and they must attempt to anticipate possible future process enhancements that may increase performance. It is possible that such process improvements may someday push the minimum delays beyond what was originally anticipated; therefore minimums should be used with care, and are recommended primarily for simulation.
- Skew testing takes into account pattern and switching direction differences between outputs.
- These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.





ADV MICRO PLA/PLE/ARRAYS _____

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.2 V to +7.0 V
DC Input Current	-30 mA to +5 mA
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC} + 0.5$ V
Static Discharge Voltage	2001 V

OPERATING RANGES**Commercial (C) Devices**

Ambient Temperature (T_A)	0°C to +75°C
Operating in Free Air	
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.2$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min.}$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 24$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min.}$		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	$I_{IN} = -18$ mA, $V_{CC} = \text{Min.}$		-1.2	V
I_{IH}	Input HIGH Current	$V_{IN} = 2.7$ V, $V_{CC} = \text{Max.}$ (Note 2)		25	μ A
I_{IL}	Input LOW Current	$V_{IN} = 0.4$ V, $V_{CC} = \text{Max.}$ (Note 2)		-250	μ A
I_I	Maximum Input Current	$V_{IN} = 5.5$ V, $V_{CC} = \text{Max.}$		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.7$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		100	μ A
I_{OLZ}	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		-100	μ A
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max.}$ (Note 3)	-30	-130	mA
I_{CC}	Supply Current	$V_{IN} = 0$ V, Outputs Open ($I_{OUT} = 0$ mA) $V_{CC} = \text{Max.}$		180	mA

Notes:

- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of I_{IL} and I_{OLZ} (or I_{IH} and I_{OZH}).
- Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT} = 0.5$ V has been chosen to avoid test problems caused by tester ground degradation.



CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0 V	V _{CC} = 5.0 V T _A = 25°C f = 1 MHz	5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 2.0 V		8	

Note:

- These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min. (Note 3)	Max.	Unit	
tPD	Input or Feedback to Combinatorial Output		16L8, 16R6, 16R4	3	7.5	ns	
		1 Output Switching		3	7		
ts	Setup Time from Input or Feedback to Clock			7		ns	
tH	Hold Time			0		ns	
tco	Clock to Output			3	6.5	ns	
tsKEW	Skew Between Registered Outputs (Note 4)				1	ns	
twL	Clock Width	LOW		5		ns	
twH		HIGH		5		ns	
fMAX	Maximum Frequency (Note 5)	External Feedback	1/(ts + tco)	74		MHz	
		Internal Feedback (fCNT)		100		MHz	
		No Feedback	1/(twh + twL)	100		MHz	
tpZX	OE to Output Enable			3	8	ns	
tpXZ	OE to Output Disable			3	8	ns	
teA	Input to Output Enable Using Product Term Control			16L8, 16R6, 16R4	3	10	ns
teR	Input to Output Disable Using Product Term Control				3	10	ns

Notes:

- See Switching Test Circuit for test conditions.
- Output delay minimums are measured under best-case conditions.
- Skew is measured with all outputs switching in the same direction.
- These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.





ADV MICRO PLA/PLE/ARRAYS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.5 V to +5.5 V
DC Output or I/O Pin Voltage	-0.5 V to +5.5 V
Static Discharge Voltage	2001 V

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T _A)	0°C to +75°C
Operating in Free Air	
Supply Voltage (V _{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = -3.2 mA, V _{IN} = V _{IH} or V _{IL} , V _{CC} = Min.	2.4		V
V _{OL}	Output LOW Voltage	I _{OL} = 24 mA, V _{IN} = V _{IH} or V _{IL} , V _{CC} = Min.		0.5	V
V _{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all inputs (Note 1)	2.0		V
V _{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all inputs (Note 1)		0.8	V
V _I	Input Clamp Voltage	I _{IN} = -18 mA, V _{CC} = Min.		-1.5	V
I _{IH}	Input HIGH Current	V _{IN} = 2.4 V, V _{CC} = Max. (Note 2)		25	μA
I _{IL}	Input LOW Current	V _{IN} = 0.4 V, V _{CC} = Max. (Note 2)		-250	μA
I _I	Maximum input Current	V _{IN} = 5.5 V, V _{CC} = Max.		100	μA
I _{ozH}	Off-State Output Leakage Current HIGH	V _{OUT} = 2.4 V, V _{CC} = Max., V _{IN} = V _{IH} or V _{IL} (Note 2)		100	μA
I _{ozL}	Off-State Output Leakage Current LOW	V _{OUT} = 0.4 V, V _{CC} = Max., V _{IN} = V _{IH} or V _{IL} (Note 2)		-100	μA
I _{sc}	Output Short-Circuit Current	V _{OUT} = 0.5 V, V _{CC} = Max. (Note 3)	-30	-130	mA
I _{CC}	Supply Current	V _{IN} = 0 V, Outputs Open (I _{OUT} = 0 mA), V _{CC} = Max.		180	mA

Notes:

- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of I_{IL} and I_{ozL} (or I_{IH} and I_{ozH}).
- Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions			Typ.	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0 V	V _{CC} = 5.0 V T _A = 25°C	CLK, OE	9	pF
				Other Inputs	2	
C _{OUT}	Output Capacitance	V _{OUT} = 2.0 V	f = 1 MHz	Outputs	4	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min. (Note 3)	Max.	Unit	
t _{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4	3	10	ns
t _S	Setup Time from Input or Feedback to Clock			16R8, 16R6, 16R4	10		ns
t _H	Hold Time				0		ns
t _{CO}	Clock to Output				2	7	ns
t _{WL}	Clock Width	LOW			8		ns
t _{WH}		HIGH			8		ns
f _{MAX}	Maximum Frequency (Note 5)	External Feedback	1/(t _S + t _{CO})		58.8		MHz
		Internal Feedback (f _{CNT})			60		MHz
		No Feedback	1/(t _{WH} + t _{WL})		62.5		MHz
t _{PZX}	OE to Output Enable				3	10	ns
t _{PXZ}	OE to Output Disable				3	10	ns
t _{EA}	Input to Output Enable Using Product Term Control			16L8, 16R6, 16R4	1	10	ns
t _{ER}	Input to Output Disable Using Product Term Control			16R4	1	10	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. Calculated from measured f_{MAX} internal.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.





ADV MICRO PLA/PLE/ARRAYS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.5 V to $V_{CC} + 0.5$ V
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC} + 0.5$ V

OPERATING RANGES**Commercial (C) Devices**

Ambient Temperature (T_A)	0°C to +75°C
Operating in Free Air	
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.2$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min.}$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 24$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min.}$		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	$I_{IN} = -18$ mA, $V_{CC} = \text{Min.}$		-1.2	V
I_{IH}	Input HIGH Current	$V_{IN} = 2.4$ V, $V_{CC} = \text{Max.}$ (Note 2)		25	μ A
I_{IL}	Input LOW Current	$V_{IN} = 0.4$ V, $V_{CC} = \text{Max.}$ (Note 2)		-250	μ A
I_I	Maximum Input Current	$V_{IN} = 5.5$ V, $V_{CC} = \text{Max.}$		100	μ A
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.4$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		100	μ A
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		-100	μ A
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max.}$ (Note 3)	-30	-130	mA
I_{CC}	Supply Current	$V_{IN} = 0$ V, Outputs Open ($I_{OUT} = 0$ mA) $V_{CC} = \text{Max.}$		180	mA

Notes:

- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
- Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second.
 $V_{OUT} = 0.5$ V has been chosen to avoid test problems caused by tester ground degradation.



CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0 V	V _{CC} = 5.0 V T _A = 25°C	8	pF
C _{OUT}	Output Capacitance	V _{OUT} = 2.0 V	f = 1 MHz	9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description		Min.	Max.	Unit
t _{PD}	Input or Feedback to Combinatorial Output		16L8, 16R6, 16R4	15	ns
t _S	Setup Time from Input or Feedback to Clock		15		ns
t _H	Hold Time		0		ns
t _{CO}	Clock to Output or Feedback			12	ns
t _{WL}	Clock Width	LOW	16R8, 16R6, 16R4	10	ns
t _{WH}		HIGH		10	ns
f _{MAX}	Maximum Frequency (Note 3)	External Feedback 1/(t _S + t _{CO})		37	MHz
		No Feedback 1/(t _{WH} + t _{WL})		50	MHz
t _{PZX}	OE to Output Enable			15	ns
t _{PXZ}	OE to Output Disable			15	ns
t _{EA}	Input to Output Enable Using Product Term Control		16L8, 16R6, 16R4	15	ns
t _{ER}	Input to Output Disable Using Product Term Control			15	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.





ADV MICRO PLA/PLE/ARRAYS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.5 V to $V_{CC} + 0.5$ V
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC} + 0.5$ V

OPERATING RANGES**Commercial (C) Devices**

Ambient Temperature (T_A)	0°C to +75°C
Operating in Free Air	
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.2$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min.}$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 24$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min.}$		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	$I_{IN} = -18$ mA, $V_{CC} = \text{Min.}$		-1.2	V
I_{IH}	Input HIGH Current	$V_{IN} = 2.7$ V, $V_{CC} = \text{Max.}$ (Note 2)		25	μ A
I_{IL}	Input LOW Current	$V_{IN} = 0.4$ V, $V_{CC} = \text{Max.}$ (Note 2)		-100	μ A
I_I	Maximum Input Current	$V_{IN} = 5.5$ V, $V_{CC} = \text{Max.}$		100	μ A
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.7$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		100	μ A
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		-100	μ A
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max.}$ (Note 3)	-30	-130	mA
I_{CC}	Supply Current	$V_{IN} = 0$ V, Outputs Open ($I_{OUT} = 0$ mA) $V_{CC} = \text{Max.}$		90	mA

Notes:

- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
- Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT} = 0.5$ V has been chosen to avoid test problems caused by tester ground degradation.



ADV MICRO PLA/PLE/ARRAYS

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0 V	V _{CC} = 5.0 V T _A = 25°C	7	pF
C _{OUT}	Output Capacitance	V _{OUT} = 2.0 V	f = 1 MHz	7	

Note:

- These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description		Min.	Max.	Unit
t _{PD}	Input or Feedback to Combinatorial Output		16L8, 16R6, 16R4	25	ns
t _s	Setup Time from Input or Feedback to Clock		25		ns
t _H	Hold Time		0		ns
t _{CO}	Clock to Output			15	ns
t _{WL}	Clock Width	LOW	16R8, 16R6, 16R4	15	ns
t _{WH}		HIGH		15	ns
f _{MAX}	Maximum Frequency (Note 4)	External Feedback 1/(t _s + t _{CO})		25	MHz
		Internal Feedback (f _{CNT})		28.5	MHz
		No Feedback 1/(t _{WH} + t _{WL})		33	MHz
t _{PZX}	OE to Output Enable			20	ns
t _{PXZ}	OE to Output Disable			20	ns
t _{EA}	Input to Output Enable Using Product Term Control		16L8, 16R6, 16R4	25	ns
t _{ER}	Input to Output Disable Using Product Term Control			25	ns

Notes:

- See Switching Test Circuit for test conditions.
- Calculated from measured f_{MAX} internal.
- These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.5 V to $V_{CC} + 0.5$ V
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC} + 0.5$ V

OPERATING RANGES**Commercial (C) Devices**

Ambient Temperature (T_A)	0°C to +75°C
Operating in Free Air	
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.2$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min.}$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 24$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min.}$		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	$I_{IN} = -18$ mA, $V_{CC} = \text{Min.}$		-1.2	V
I_{IH}	Input HIGH Current	$V_{IN} = 2.7$ V, $V_{CC} = \text{Max.}$ (Note 2)		25	μ A
I_{IL}	Input LOW Current	$V_{IN} = 0.4$ V, $V_{CC} = \text{Max.}$ (Note 2)		-250	μ A
I_I	Maximum Input Current	$V_{IN} = 5.5$ V, $V_{CC} = \text{Max.}$		100	μ A
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.7$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		100	μ A
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		-100	μ A
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max.}$ (Note 3)	-30	-130	mA
I_{CC}	Supply Current	16L8	$V_{IN} = 0$ V, Outputs Open ($I_{OUT} = 0$ mA) $V_{CC} = \text{Max.}$	155	mA
		16R8/6/4		180	

Notes:

- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
- Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{CC} = 0.5$ V has been chosen to avoid test problems caused by tester ground degradation.



ADV MICRO PLA/PLE/ARRAYS

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0 V	V _{CC} = 5.0 V T _A = 25°C	7	pF
C _{OUT}	Output Capacitance	V _{OUT} = 2.0 V	f = 1 MHz	7	

Note:

- These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description		Min.	Max.	Unit
t _{PD}	Input or Feedback to Combinatorial Output		16L8, 16R6, 16R4	25	ns
t _S	Setup Time from Input or Feedback to Clock		25		ns
t _H	Hold Time		0		ns
t _{CO}	Clock to Output			15	ns
t _{WL}	Clock Width	LOW	15		ns
t _{WH}		HIGH	15		ns
f _{MAX}	Maximum Frequency (Note 4)	External Feedback	1/(t _S + t _{CO})	25	MHz
		Internal Feedback (f _{CNT})		28.5	MHz
		No Feedback	1/(t _{WH} + t _{WL})	33	MHz
t _{PZX}	OE to Output Enable			20	ns
t _{PXZ}	OE to Output Disable			20	ns
t _{EA}	Input to Output Enable Using Product Term Control		16L8, 16R6, 16R4	25	ns
t _{ER}	Input to Output Disable Using Product Term Control			25	ns

Notes:

- See Switching Test Circuit for test conditions.
- Calculated from measured f_{MAX} internal.
- These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.





ADV MICRO PLA/PLE/ARRAYS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

OPERATING RANGES**Commercial (C) Devices**

Ambient Temperature (T _A)	0°C to +75°C
Operating in Free Air	
Supply Voltage (V _{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = -1 mA V _{IN} = V _{IH} or V _{IL} V _{CC} = Min.	2.4		V
V _{OL}	Output LOW Voltage	I _{OL} = 8 mA V _{IN} = V _{IH} or V _{IL} V _{CC} = Min.		0.5	V
V _{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V _{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V _I	Input Clamp Voltage	I _{IN} = -18 mA, V _{CC} = Min.		-1.5	V
I _{IH}	Input HIGH Current	V _{IN} = 2.4 V, V _{CC} = Max. (Note 2)		25	μA
I _{IL}	Input LOW Current	V _{IN} = 0.4 V, V _{CC} = Max. (Note 2)		-250	μA
I _I	Maximum Input Current	V _{IN} = 5.5 V, V _{CC} = Max.		100	μA
I _{ozH}	Off-State Output Leakage Current HIGH	V _{OUT} = 2.4 V, V _{CC} = Max. V _{IN} = V _{IH} or V _{IL} (Note 2)		100	μA
I _{ozL}	Off-State Output Leakage Current LOW	V _{OUT} = 0.4 V, V _{CC} = Max. V _{IN} = V _{IH} or V _{IL} (Note 2)		-100	μA
I _{sc}	Output Short-Circuit Current	V _{OUT} = 0.5 V, V _{CC} = Max. (Note 3)	-30	-250	mA
I _{CC}	Supply Current	V _{IN} = 0 V, Outputs Open (I _{OUT} = 0 mA) V _{CC} = Max.		55	mA

Notes:

- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of I_{IL} and I_{ozL} (or I_{IH} and I_{ozH}).
- Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V as been chosen to avoid test problems caused by tester ground degradation.



ADV MICRO PLA/PLE/ARRAYS

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description			Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				35	ns
t_s	Setup Time from Input or Feedback to Clock			35		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output or Feedback				25	ns
t_{WL}	Clock Width	LOW		25		ns
t_{WH}		HIGH		25		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_s + t_{CO})$	16		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	20		MHz
t_{PZX}	\overline{OE} to Output Enable				25	ns
t_{PXZ}	\overline{OE} to Output Disable				25	ns
t_{EA}	Input to Output Enable Using Product Term Control				35	ns
t_{ER}	Input to Output Disable Using Product Term Control				35	ns

Notes:

1. See Switching Test Circuit for test conditions.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.





ADV MICRO PLA/PLE/ARRAYS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.2 V to +5.5 V
DC Input Current	-30 mA to +5 mA
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC} + 0.5$ V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military Devices (Note 1)

Ambient Temperature (T_A)	-55°C Min.
Operating in Free Air	
Operating Case (T_C) Temperature	125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at $T_C = +25^\circ\text{C}$, $+125^\circ\text{C}$, and -55°C , per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -2$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min.}$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 12$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min.}$		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	$I_{IN} = -18$ mA, $V_{CC} = \text{Min.}$		-1.2	V
I_{IH}	Input HIGH Current	$V_{IN} = 2.7$ V, $V_{CC} = \text{Max.}$ (Note 4)		25	μA
I_{IL}	Input LOW Current	$V_{IN} = 0.4$ V, $V_{CC} = \text{Max.}$ (Note 4)		-250	μA
I_I	Maximum Input Current	$V_{IN} = 5.5$ V, $V_{CC} = \text{Max.}$		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.7$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 4)		100	μA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 4)		-100	μA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max.}$ (Note 5)	-30	-130	mA
I_{CC}	Supply Current	$V_{IN} = 0$ V, Outputs Open ($I_{OUT} = 0$ mA) $V_{CC} = \text{Max.}$		200	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT} = 0.5$ V has been chosen to avoid test problems caused by tester ground degradation.

ADV MICRO PLA/PLE/ARRAYS

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0 V	10	pF
			5	
C _{OUT}	Output Capacitance	V _{OUT} = 2.0 V	9	

Note:

- These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

SWITCHING CHARACTERISTICS OVER MILITARY Operating Ranges (Note 2)									
Parameter Symbol	Parameter Description		-10		-12		Unit		
			Min. (Note 3)	Max.	Min. (Note 3)	Max.			
t _{PD}	Input or Feedback to Combinatorial Output		16L8, 16R6, 16R4	3	10	3	12	ns	
t _s	Setup Time from Input or Feedback to Clock		16R8, 16R6, 16R4	10		10		ns	
t _h	Hold Time			0		0		ns	
t _{co}	Clock to Output			2	9	3	11	ns	
t _{sKEW}	Skew Between Registered Outputs (Note 4)				1		1	ns	
t _{wL}	Clock Width	LOW		8		8		ns	
t _{wH}		HIGH		8		8		ns	
f _{MAX}	Maximum Frequency (Note 5)	External Feedback		1/(t _s + t _{co})		47.6		MHz	
		Internal Feedback (f _{CNT})		60.6		MHz			
		No Feedback		1/(t _{wH} + t _{wL})		62.5		MHz	
t _{pZX}	OE to Output Enable (Note 5)				1	10	1	12	ns
t _{pXZ}	OE to Output Disable (Note 5)				1	10	1	12	ns
t _{EA}	Input to Output Enable Using Product Term Control (Note 5)		16L8, 16R6, 16R4	1	10	1	12	ns	
t _{ER}	Input to Output Disable Using Product Term Control (Note 5)			1	10	1	12	ns	

Notes:

- See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
- Minimum value for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} parameters should be used for simulation purposes only and are not tested.
- Skew is measured with all outputs switching in the same direction.
- These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.





59E D ■ 0257526 0032255 078 ■ AMD2

ADV MICRO PLA/PLE/ARRAYS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES**Military (M) Devices (Note 1)**

Ambient Temperature (T _A)	-55°C Min.
Operating in Free Air	
Operating Case (T _C) Temperature	125°C Max.
Supply Voltage (V _{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and -55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = -2 mA V _{IN} = V _{IH} or V _{IL} V _{CC} = Min.	2.4		V
V _{OL}	Output LOW Voltage	I _{OL} = 12 mA V _{IN} = V _{IH} or V _{IL} V _{CC} = Min.		0.5	V
V _{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V _{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V _I	Input Clamp Voltage	I _{IN} = -18 mA, V _{CC} = Min.		-1.5	V
I _{IH}	Input HIGH Current	V _{IN} = 2.4 V, V _{CC} = Max. (Note 4)		25	μA
I _{IL}	Input LOW Current	V _{IN} = 0.4 V, V _{CC} = Max. (Note 4)		-250	μA
I _I	Maximum Input Current	V _{IN} = 5.5 V, V _{CC} = Max.		1	mA
I _{OZH}	Off-State Output Leakage Current HIGH	V _{OUT} = 2.4 V, V _{CC} = Max. V _{IN} = V _{IH} or V _{IL} (Note 4)		100	μA
I _{OZL}	Off-State Output Leakage Current LOW	V _{OUT} = 0.4 V, V _{CC} = Max. V _{IN} = V _{IH} or V _{IL} (Note 4)		-100	μA
I _{SC}	Output Short-Circuit Current	V _{OUT} = 0.5 V, V _{CC} = Max. (Note 5)	-30	-130	mA
I _{CC}	Supply Current	V _{IN} = 0 V, Outputs Open (I _{OUT} = 0 mA) V _{CC} = Max.		180	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

ADV MICRO PLA/PLE/ARRAYS

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0 V	V _{CC} = 5.0 V T _A = 25°C f = 1 MHz	9	pF
C _{OUT}	Output Capacitance	V _{OUT} = 2.0 V		10	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min.	Max.	Unit
t _{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4		20 ns
t _S	Setup Time from Input or Feedback to Clock			16R8, 16R6, 16R4	20	ns
t _H	Hold Time				0	ns
t _{CO}	Clock to Output or Feedback					15 ns
t _{WL}	Clock Width	LOW			12	ns
t _{WH}		HIGH			12	ns
f _{MAX}	Maximum Frequency (Note 3)	External Feedback	1/(t _S + t _{CO})		28.5	MHz
		No Feedback	1/(t _{WH} + t _{WL})		41.6	MHz
t _{PZX}	OE to Output Enable (Note 4)					20 ns
t _{PIXZ}	OE to Output Disable (Note 4)					20 ns
t _{EA}	Input to Output Enable Using Product Term Control (Note 4)			16L8, 16R6, 16R4	25	ns
t _{ER}	Input to Output Disable Using Product Term Control (Note 4)				20	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.





ADV MICRO PLA/PLE/ARRAYS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES**Military (M) Devices (Note 1)**

Ambient Temperature (T _A)	-55°C Min.
Operating in Free Air	
Operating Case (T _C) Temperature	125°C Max.
Supply Voltage (V _{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and -55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = -2 mA V _{IN} = V _{IH} or V _{IL} V _{CC} = Min.	2.4		V
V _{OL}	Output LOW Voltage	I _{OL} = 12 mA V _{IN} = V _{IH} or V _{IL} V _{CC} = Min.		0.5	V
V _{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V _{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V _I	Input Clamp Voltage	I _{IN} = -18 mA, V _{CC} = Min.		-1.5	V
I _{IH}	Input HIGH Current	V _{IN} = 2.4 V, V _{CC} = Max. (Note 4)		25	μA
I _{IL}	Input LOW Current	V _{IN} = 0.4 V, V _{CC} = Max. (Note 4)		-250	μA
I _I	Maximum Input Current	V _{IN} = 5.5 V, V _{CC} = Max.		1	mA
I _{ozH}	Off-State Output Leakage Current HIGH	V _{OUT} = 2.4 V, V _{CC} = Max. V _{IN} = V _{IH} or V _{IL} (Note 4)		100	μA
I _{ozL}	Off-State Output Leakage Current LOW	V _{OUT} = 0.4 V, V _{CC} = Max. V _{IN} = V _{IH} or V _{IL} (Note 4)		-100	μA
I _{sc}	Output Short-Circuit Current	V _{OUT} = 0.5 V, V _{CC} = Max. (Note 5)	-30	-130	mA
I _{CC}	Supply Current	V _{IN} = 0 V, Outputs Open (I _{OUT} = 0 mA) V _{CC} = Max.		90	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{ozL} (or I_{IH} and I_{ozH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.



CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0 V	V _{CC} = 5.0 V T _A = 25°C	7	pF
C _{OUT}	Output Capacitance	V _{OUT} = 2.0 V	f = 1 MHz	7	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description		Min.	Max.	Unit
t _{PD}	Input or Feedback to Combinatorial Output		16L8, 16R6, 16R4	30	ns
t _S	Setup Time from Input or Feedback to Clock		30		ns
t _H	Hold Time		0		ns
t _{CO}	Clock to Output or Feedback			20	ns
t _{WL}	Clock Width	LOW	20		ns
t _{WH}		HIGH	20		ns
f _{MAX}	Maximum Frequency (Note 3)	External Feedback	1/(t _S + t _{CO})	20	MHz
		No Feedback	1/(t _{WH} + t _{WL})	25	MHz
t _{PZX}	\overline{OE} to Output Enable (Note 4)			25	ns
t _{PXZ}	\overline{OE} to Output Disable (Note 4)			25	ns
t _{EA}	Input to Output Enable Using Product Term Control (Note 4)		16L8, 16R6, 16R4	30	ns
t _{ER}	Input to Output Disable Using Product Term Control (Note 4)			30	ns

Notes:

- See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
- These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
- These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.





ADV MICRO PLA/PLE/ARRAYS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES**Military (M) Devices (Note 1)**

Ambient Temperature (T_A)	-55°C Min.
Operating in Free Air	
Operating Case (T_C) Temperature	125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at $T_C = +25^\circ\text{C}$, $+125^\circ\text{C}$, and -55°C , per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -2\text{ mA}$ $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min.}$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 12\text{ mA}$ $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min.}$		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	$I_{IN} = -18\text{ mA}$, $V_{CC} = \text{Min.}$		-1.5	V
I_{IH}	Input HIGH Current	$V_{IN} = 2.4\text{ V}$, $V_{CC} = \text{Max.}$ (Note 4)		25	μA
I_{IL}	Input LOW Current	$V_{IN} = 0.4\text{ V}$, $V_{CC} = \text{Max.}$ (Note 4)		-250	μA
I_I	Maximum Input Current	$V_{IN} = 5.5\text{ V}$, $V_{CC} = \text{Max.}$		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.4\text{ V}$, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 4)		100	μA
I_{OLZ}	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4\text{ V}$, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 4)		-100	μA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5\text{ V}$, $V_{CC} = \text{Max.}$ (Note 5)	-30	-130	mA
I_{CC}	Supply Current	$V_{IN} = 0\text{ V}$, Outputs Open ($I_{OUT} = 0\text{ mA}$) $V_{CC} = \text{Max.}$		180	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OLZ} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT} = 0.5\text{ V}$ has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0 V	V _{CC} = 5.0 V T _A = 25°C	7	pF
C _{OUT}	Output Capacitance	V _{OUT} = 2.0 V	f = 1 MHz	7	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min.	Max.	Unit
tPD	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4	30	ns
tS	Setup Time from Input or Feedback to Clock			16R8, 16R6, 16R4	30	ns
tH	Hold Time				0	ns
tCO	Clock to Output or Feedback				20	ns
tWL	Clock Width	LOW			20	ns
tWH		HIGH			20	ns
fMAX	Maximum Frequency (Note 3)	External Feedback	1/(tS + tCO)		20	MHz
		No Feedback	1/(tWH + tWL)		25	MHz
tPZX	OE to Output Enable (Note 4)				25	ns
tPXZ	OE to Output Disable (Note 4)				25	ns
tEA	Input to Output Enable Using Product Term Control (Note 4)			16L8, 16R6, 16R4	30	ns
tER	Input to Output Disable Using Product Term Control (Note 4)				30	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.





59E D ■ 0257526 0032261 371 ■ AMD2

ADV MICRO PLA/PLE/ARRAYS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T _A) Operating in Free Air	-55°C Min.
Operating Case (T _C) Temperature	125°C Max.
Supply Voltage (V _{CC}) with Respect to Ground	+4.50 V to +5.50 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and -55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = -1 mA V _{IN} = V _{IH} or V _{IL} V _{CC} = Min.	2.4		V
V _{OL}	Output LOW Voltage	I _{OL} = 4 mA V _{IN} = V _{IH} or V _{IL} V _{CC} = Min.		0.5	V
V _{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all inputs (Note 3)	2.0		V
V _{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all inputs (Note 3)		0.8	V
V _I	Input Clamp Voltage	I _{IN} = -18 mA, V _{CC} = Min.		-1.5	V
I _{IH}	Input HIGH Current	V _{IN} = 2.4 V, V _{CC} = Max. (Note 4)		25	μA
I _{IL}	Input LOW Current	V _{IN} = 0.4 V, V _{CC} = Max. (Note 4)		-250	μA
I _I	Maximum Input Current	V _{IN} = 5.5 V, V _{CC} = Max.		1	mA
I _{OZH}	Off-State Output Leakage Current HIGH	V _{OUT} = 2.4 V, V _{CC} = Max. V _{IN} = V _{IH} or V _{IL} (Note 4)		100	μA
I _{OZL}	Off-State Output Leakage Current LOW	V _{OUT} = 0.4 V, V _{CC} = Max. V _{IN} = V _{IH} or V _{IL} (Note 4)		-100	μA
I _{SC}	Output Short-Circuit Current	V _{OUT} = 0.5 V, V _{CC} = Max. (Note 5)	-30	-250	mA
I _{CC}	Supply Current	V _{IN} = 0 V, Outputs Open (I _{OUT} = 0 mA) V _{CC} = Max.		55	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
tPD	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4		50	ns
ts	Setup Time from Input or Feedback to Clock			16R8, 16R6, 16R4	50		ns
tH	Hold Time				0		ns
tCO	Clock to Output or Feedback					25	ns
twL	Clock Width	LOW			25		ns
twH		HIGH			25		ns
fMAX	Maximum Frequency (Note 2)	External Feedback	1/(ts + tco)		13.3		MHz
		No Feedback	1/(twH + twL)		20		MHz
tpZX	OE to Output Enable (Note 3)					25	ns
tpXZ	OE to Output Disable (Note 3)				25	ns	
tEA	Input to Output Enable Using Product Term Control (Note 3)			16L8, 16R6, 16R4		45	ns
tER	Input to Output Disable Using Product Term Control (Note 3)					45	ns

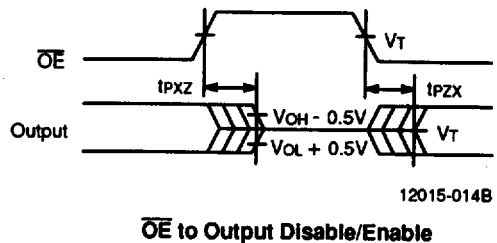
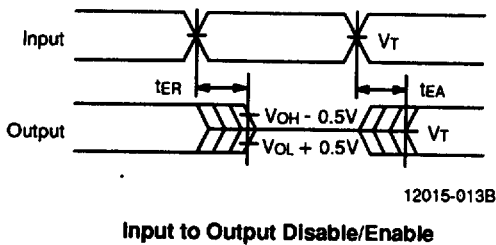
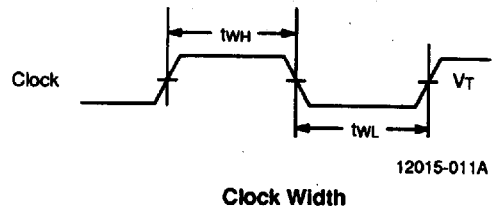
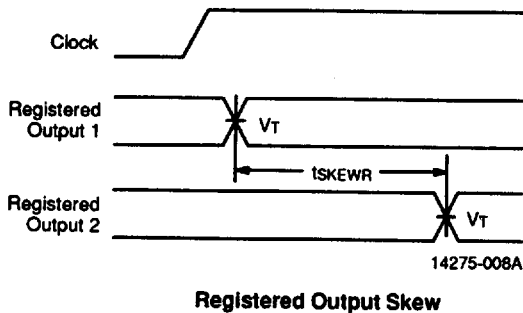
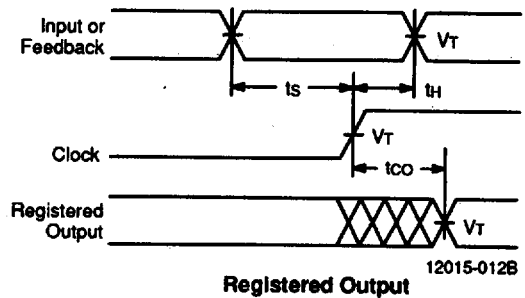
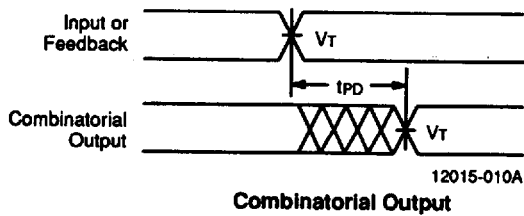
Notes:

1. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.





SWITCHING WAVEFORMS



Notes:

1. $V_T = 1.5 \text{ V}$
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–3 ns typical.

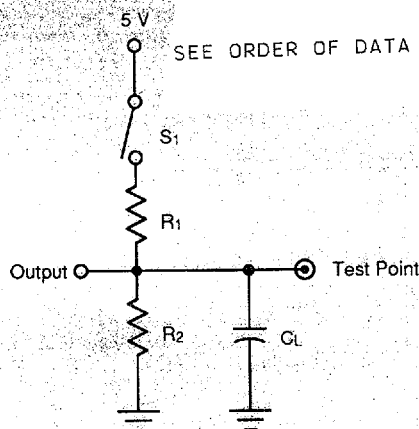


KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing; State Unknown
	Does Not Apply	Center Line is High Impedance 'Off' State

KS000010-PAL

SWITCHING TEST CIRCUIT



NOTICE

SEE ORDER OF DATA FOR ERRATA INFORMATION

12350-019A

Specification	S ₁	C _L	Commercial		Measured Output Value
			R ₁	R ₂	
t _{PD} , t _{CO}	Closed	50 pF	200 Ω	200 Ω	1.5 V
t _{PZX} , t _{EA}	Z → H: Open Z → L: Closed				1.5 V
t _{PXZ} , t _{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V _{OH} - 0.5 V L → Z: V _{OL} + 0.5 V

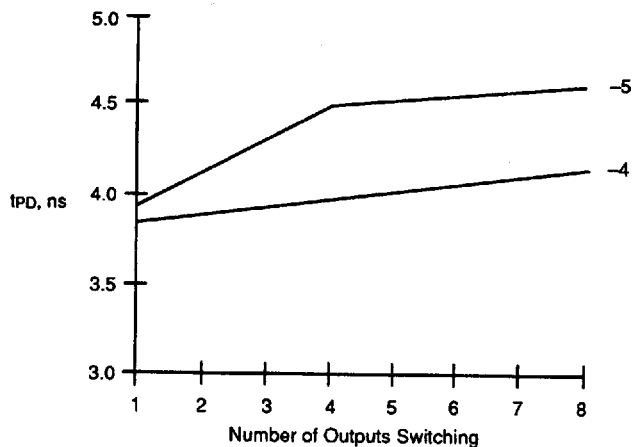


59E D ■ 0257526 0032265 T17 ■ AMD2

ADV MICRO PLA/PLE/ARRAYS

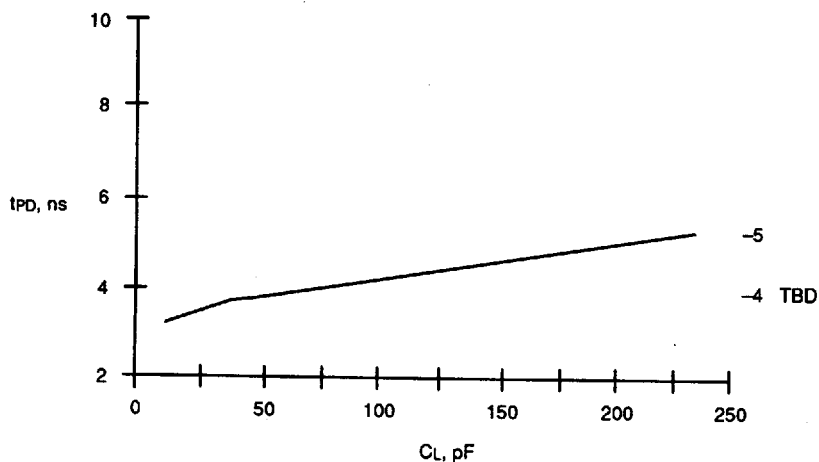
MEASURED SWITCHING CHARACTERISTICS for the PAL16R8-4/5

V_{CC} = 4.75 V, T_A = 75°C (Note 1)



t_{PD} vs. Number of Outputs Switching

14275-010A



t_{PD} vs. Load Capacitance

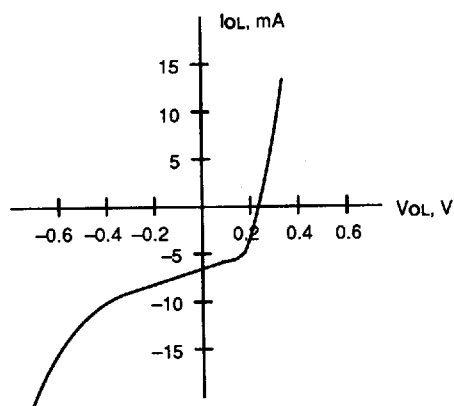
V_{CC} = 5.25 V, T_A = 25°C

14275-011A

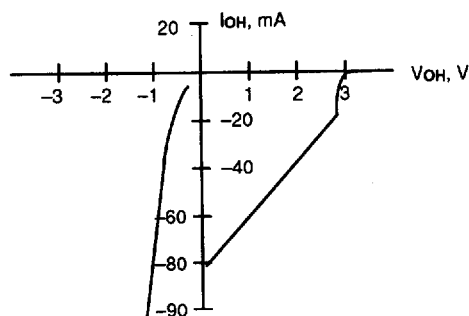
Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where t_{PD} may be affected.

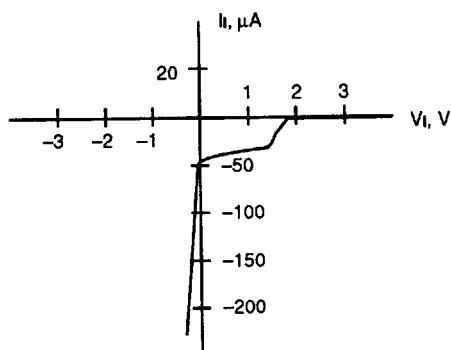
ADV MICRO PLA/PLE/ARRAYS

CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS for the PAL16R8-4/5 $V_{CC} = 5.0 \text{ V}$, $T_A = 25^\circ\text{C}$ **Output, LOW**

10240-003B

**Output, HIGH**

10240-004B

**Input**

10240-005A



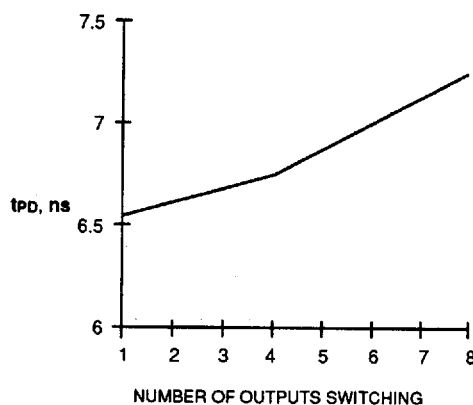


59E D ■ 0257526 0032267 89T ■ AMD2

ADV MICRO PLA/PLE/ARRAYS

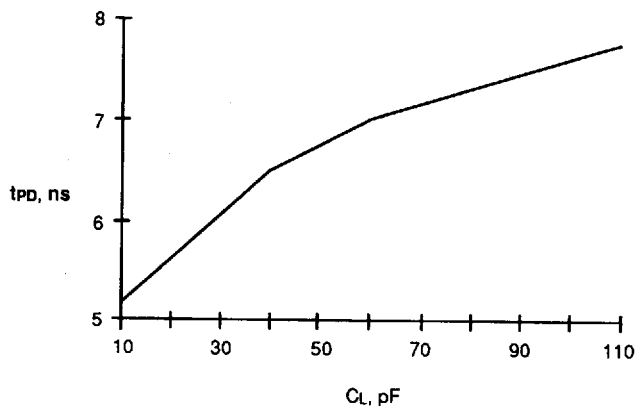
MEASURED SWITCHING CHARACTERISTICS for the PAL16R8-7

V_{CC} = 4.75 V, T_A = 75°C (Note 1)



t_{PD} vs. Number of Outputs Switching

10240-001A



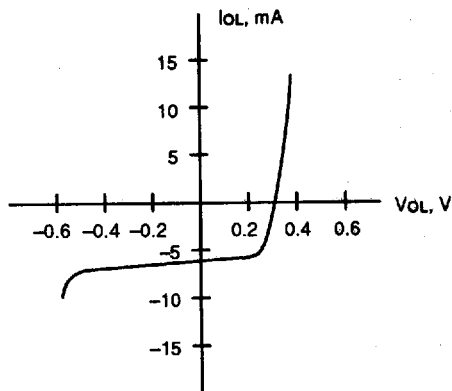
t_{PD} vs. Load Capacitance

10240-002A

Note:

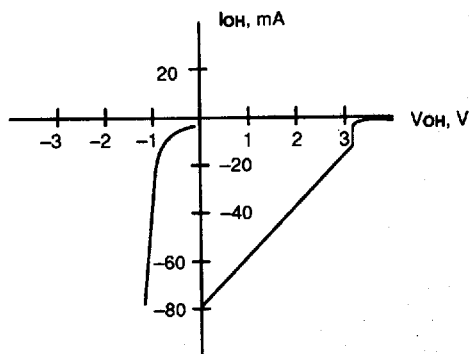
1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where t_{PD} may be affected.



CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS for the PAL16R8-7 $V_{CC} = 5.0 \text{ V}$, $T_A = 25^\circ\text{C}$ 

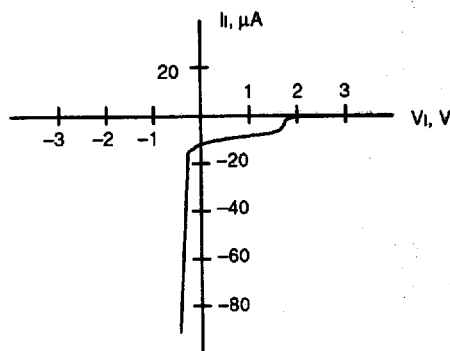
Output, LOW

10240-003A



Output, HIGH

10240-004A



Input

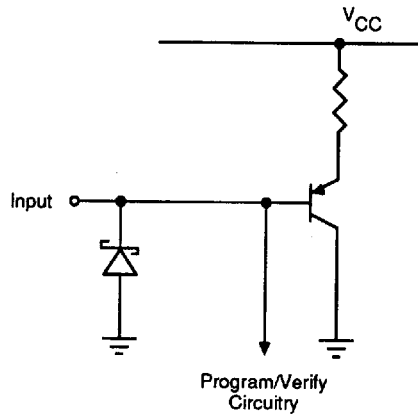
10240-005A



INPUT/OUTPUT EQUIVALENT SCHEMATICS

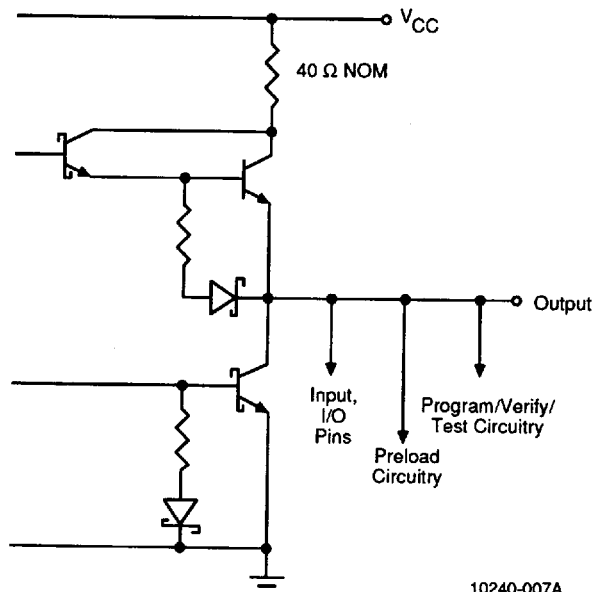
ADV MICRO PLA/PLE/ARRAYS

Typical Input



10240-006A

Typical Output



10240-007A

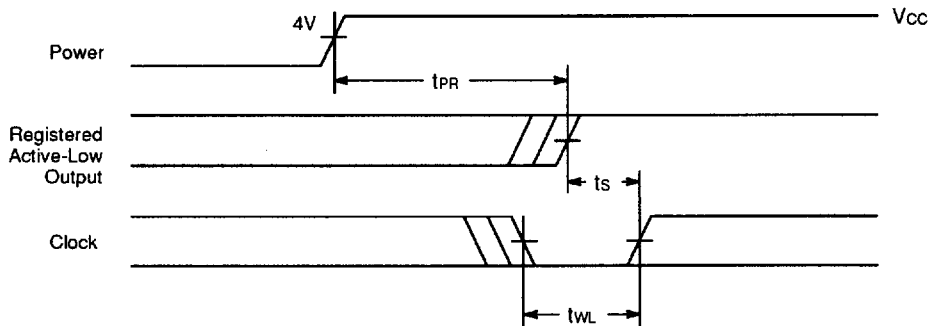
POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will be HIGH due to the inverting output buffer. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC}

can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_s	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



12350-024A

Power-Up Reset Waveform